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Time Service Facility FPGA PSM specification

1 Introduction

This document WINNF-TS-3004-App03 is the FPGA PSM specification of WInnForum Time Service Facility V1.1.0.

It derives from Time Service Facility PIM Specification [Ref1] in accordance with Principles for WInnForum Facility Standards [Ref2].

It addresses the FPGA programming paradigm, applying the mapping rules of the FPGA section of WInnForum Facilities PSMs Mapping Rules [Ref3] and specifically reporting any deviation to those rules.

The following figure positions the interfaces addressed by the FPGA PSM specification:

As depicted, the FPGA PSM specification addresses the FPGA functional interfaces of time services, positioned, within an FPGA node, between the FPGA applicative modules of radio applications and FPGA façades of time service instances.

The FPGA PSM specification considers RTL (Register-Transfer Level) [Ref4] interfaces, specifying RTL signals and the associated chronogram, independently from the used programming language (e.g., VHDL or Verilog).

It also provides normative source files applicable in case of VHDL programming.

1.1 Reference definitions

The Time Service Facility FPGA PSM specification applies the following definitions from Time Service Facility PIM Specification [Ref1]:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Used definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time service concepts</td>
<td>time service, Time Service Facility</td>
</tr>
</tbody>
</table>

Table 1 Definitions from Time Service Facility PIM Specification
The Time Service Facility FPGA PSM specification applies the following definitions from Principles for WInnForum Facility Standards [Ref2]:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Used definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base concepts</td>
<td>radio application</td>
</tr>
<tr>
<td>Architecture concepts</td>
<td>facade</td>
</tr>
<tr>
<td>WInnForum facilities</td>
<td>facility, PIM specification, PSM specification</td>
</tr>
<tr>
<td>Primitives</td>
<td>primitive, parameter, exception, type</td>
</tr>
</tbody>
</table>

Table 2 Definitions from Principles for WInnForum Facility Standards

The Time Service Facility FPGA PSM specification applies the following definitions from WInnForum Facilities PSMs Mapping Rules [Ref3]:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Used definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specification purpose</td>
<td>FPGA PSM specification, FPGA functional interfaces</td>
</tr>
<tr>
<td>Software architecture</td>
<td>FPGA node, FPGA façade, FPGA applicative module</td>
</tr>
<tr>
<td>RTL signals origin</td>
<td>origin, caller, callee</td>
</tr>
<tr>
<td>Base RTL signals</td>
<td>primitive prefix, structural RTL signals, semantics RTL signals, parameters RTL signals, exception RTL signals</td>
</tr>
</tbody>
</table>

Table 3 Definitions from WInnForum Facilities PSMs Mapping Rules

The term “unspecified” indicates an aspect explicitly left to implementer’s decisions.

1.2 Conformance

1.2.1 Radio platform items

An FPGA façade of a time service implementation is conformant with the Time Service Facility FPGA PSM specification if it provides an FPGA implementation of related primitives.

An FPGA time service is defined as a time service implementation with all of its FPGA façades being conformant with the FPGA PSM specification.

1.2.2 Radio application items

An FPGA applicative module of a radio application is conformant with the Time Service Facility FPGA PSM specification if it can use FPGA façades conformant with the FPGA PSM specification without using any non-standard primitive for the time service.

1.3 Document structure

Section 2 specifies the normative content for the FPGA functional interfaces.

Section 3 specifies the normative content for FPGA constants.

Section 4 specifies the normative files to be used for VHDL programming.
2 FPGA functional interfaces

This normative section specifies the FPGA functional interfaces for time service, according to the FPGA section of WInnForum Facilities PSMs Mapping Rules [Ref3].

2.1 Specification approach

2.1.1 Base RTL signals

The following base RTL signals from the FPGA section of WInnForum Facilities PSMs Mapping Rules [Ref3] are used:

<table>
<thead>
<tr>
<th>Base RTL signal</th>
<th>Used definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Structural RTL signals</td>
<td>CLK, RST</td>
</tr>
<tr>
<td>Semantics RTL signals</td>
<td>EN, RDY</td>
</tr>
<tr>
<td>Parameters RTL signals</td>
<td>EN_IN, DATA_IN, EN_OUT, DATA_OUT</td>
</tr>
<tr>
<td>Exception RTL signals</td>
<td>IRQ</td>
</tr>
</tbody>
</table>

Table 4 Base RTL signals from WInnForum Facilities PSMs Mapping Rules

For each base RTL signal, the complete RTL signal name, its origin (using the concept of caller and callee) and its format are specified.

2.1.2 Primitive prefixes

The primitive prefixes for time service follow the related indications of WInnForum Facilities PSMs Mapping Rules [Ref3].

A primitive prefix concatenates:

- The TSF field, for time service,
- The <instNum> field, optionally numbering instances of a time service in case there are more than one (starting count from 1),
- The <PRIM_NAME> field, identifying the primitive using a screaming snake case transcription of the PIM specification name.
2.2 Interfaces specification

2.2.1 TimeService::TerminalTime::TerminalTimeAccess

2.2.1.1 getTerminalTime()

The RTL signals for `getTerminalTime()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>CL</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_OUT</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_OUT.terminal_time</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
</tbody>
</table>

Table 5 RTL signals for `getTerminalTime()`

The dynamic behavior for `getTerminalTime()` is specified by the following chronogram:

![Figure 2 Dynamic behavior for getTerminalTime()](image)

2.2.1.2 getTerminalTimeRateUncertainty()

The RTL signals for `getTerminalTimeRateUncertainty()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>CL</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_OUT</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_OUT.terminal_time_rate_uncertainty</td>
<td>FPGA app module</td>
<td>32-bit vector -- signed</td>
</tr>
</tbody>
</table>

Table 6 RTL signals for `getTerminalTimeRateUncertainty()`
The dynamic behavior for \texttt{getTerminalTimeRateUncertainty()} is specified by the following chronogram:

![Dynamic behavior for getTerminalTimeRateUncertainty()](image)

Figure 3  Dynamic behavior for \texttt{getTerminalTimeRateUncertainty()}

### 2.2.2 \texttt{TimeService::SystemTime::SystemTimeAccess}

#### 2.2.2.1 getCurrentTAI()

The RTL signals for \texttt{getCurrentTAI()} are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSF_(&lt;\text{instNum}&gt;_)GET_CURRENT_TAI_ +</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_OUT</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_OUT.current_tai</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_OUT.time_stamp</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_OUT.time_uncertainty</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
</tbody>
</table>

Table 7  RTL signals for \texttt{getCurrentTAI()}

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The dynamic behavior for **getCurrentTAI()** is specified by the following chronogram:

![Figure 4 Dynamic behavior for getCurrentTAI()](image)

### 2.2.2.2 getCurrentUTC()

The RTL signals for **getCurrentUTC()** are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSF_{&lt;instNum&gt;}<em>GET_CURRENT.UTC</em> +</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_OUT</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_OUT.current_utc</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_OUT.time_stamp</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_OUT.time_uncertainty</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
</tbody>
</table>

Table 8 RTL signals for **getCurrentUTC()**
The dynamic behavior for `getCurrentUTC()` is specified by the following chronogram:

![Figure 5 Dynamic behavior for getCurrentUTC()](image)

2.2.2.3 `getLastUpdateTAI()`

The RTL signals for `getLastUpdateTAI()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>TSF_{&lt;instNum&gt;_}GET_LAST_UPDATE_TAI_+</code></td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td><code>CLK</code></td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td><code>RST</code></td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td><code>EN_IN</code></td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td><code>EN_OUT</code></td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td><code>DATA_OUT.last_update_tai</code></td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td><code>DATA_OUT.time_stamp</code></td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td><code>DATA_OUT.time_uncertainty</code></td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
</tbody>
</table>

Table 9  RTL signals for `getLastUpdateTAI()`
The dynamic behavior for \textit{getLastUpdateTAI()} is specified by the following chronogram:

![Chronogram for getLastUpdateTAI()](image)

**Figure 6** Dynamic behavior for \textit{getLastUpdateTAI()}

### 2.2.2.4 \texttt{getLastUpdateUTC()}

The RTL signals for \textit{getLastUpdateUTC()} are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSF_(&lt;instNum&gt;__)\texttt{GET_LAST_UPDATE_UTC_} +</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_OUT</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_OUT.last_update_utc</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_OUT.time_stamp</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_OUT.time_uncertainty</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
</tbody>
</table>

**Table 10** RTL signals for \textit{getLastUpdateUTC()}

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The dynamic behavior for `getLastUpdateUTC()` is specified by the following chronogram:

![Figure 7 Dynamic behavior for getLastUpdateUTC()](image)

### 2.2.3 `TimeService::SystemTime::StandardTimeProvision`

#### 2.2.3.1 `provideTAI()`

The RTL signals for `provideTAI()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSF_{&lt;instNum&gt;}<em>PROVIDE_TAI</em>+</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.provided_tai</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_IN.time_stamp</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_IN.time_uncertainty</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_IN.source_id</td>
<td>FPGA app module</td>
<td>8-bit vector</td>
</tr>
<tr>
<td>IRQ_FUTURE_TIME_STAMP (optional)</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

*Table 11 RTL signals for `provideTAI()`*
The dynamic behavior for `provideTAI()` is specified by the following chronogram:

![Chronogram of provideTAI()](image_url)

**Figure 8 Dynamic behavior for provideTAI()**

### 2.2.3.2 `provideUTC()`

The RTL signals for `provideUTC()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>TSF_{&lt;instNum&gt;}_PROVIDE_UTC_</code> +</td>
<td><strong>FPGA façade</strong></td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td><strong>FPGA façade</strong></td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td><strong>FPGA façade</strong></td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td><strong>FPGA façade</strong></td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.provided_utc</td>
<td><strong>FPGA app module</strong></td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_IN.time_stamp</td>
<td><strong>FPGA app module</strong></td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_IN.time_uncertainty</td>
<td><strong>FPGA app module</strong></td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_IN.source_id</td>
<td><strong>FPGA app module</strong></td>
<td>8-bit vector</td>
</tr>
<tr>
<td><strong>IRQ_FUTURE_TIME_STAMP</strong> (optional)</td>
<td><strong>FPGA app module</strong></td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

**Table 12 RTL signals for provideUTC()**
The dynamic behavior for `provideUTC()` is specified by the following chronogram:

![Dynamic behavior for provideUTC()](image)

**Figure 9** Dynamic behavior for `provideUTC()`

### 2.2.4 TimeService::StandardTimes::ReferencesNotification

#### 2.2.4.1 notifyStandardTimeReference()

The RTL signals for `notifyStandardTimeReference()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>TSF_{&lt;instNum&gt;_}NOTIFY_STANDARD_TIME_REFERENCE_</code> +</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td><code>DATA_IN.reference_tai</code></td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td><code>DATA_IN.reference_utc</code></td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td><code>DATA_IN.time_stamp</code></td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td><code>DATA_IN.time_uncertainty</code></td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td><code>DATA_IN.source_id</code></td>
<td>FPGA app module</td>
<td>8-bit vector</td>
</tr>
</tbody>
</table>

**Table 13** RTL signals for `notifyStandardTimeReference()`
The `int` type for `SourceId` in the *PIM specification* (not a valid IDL type) maps to an 8-bit vector.

The dynamic behavior for `notifyStandardTimeReference()` is specified by the following chronogram:

![Dynamic behavior for notifyStandardTimeReference()](image)

**Figure 10** Dynamic behavior for `notifyStandardTimeReference()`

### 2.2.5 TimeService::SpecificTimes::SpecificTimeHandling

#### 2.2.5.1 setSpecificTime()

The RTL signals for `setSpecificTime()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>TSF_{&lt;instNum&gt;_}SET_SPECIFIC_TIME_ +</code></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td><code>DATA_IN.specific_time_id</code></td>
<td>FPGA app module</td>
<td>16-bit vector</td>
</tr>
<tr>
<td><code>DATA_IN.specific_time</code></td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td><code>DATA_IN.time_stamp</code></td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td><code>DATA_IN.time_uncertainty</code></td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td><code>IRQ_FUTURE_TIME_STAMP</code> (optional)</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td><code>IRQ_INVALID_SPECIFIC_TIME_ID</code> (optional)</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

| **Table 14** RTL signals for `setSpecificTime()` |

---

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The `int` type for `specificTimeId` in the PIM specification (not a valid IDL type) maps to a 16-bit vector.

The dynamic behavior for `setSpecificTime()` is specified by the following chronogram:

![Figure 11 Dynamic behavior for setSpecificTime()](image)

2.2.5.2 `getSpecificTime()`

The RTL signals for `getSpecificTime()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>TSF_{&lt;instNum&gt;}_GET_SPECIFIC_TIME_</code></td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RST</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_OUT</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.specific_time_id</td>
<td>FPGA app module</td>
<td>16-bit vector</td>
</tr>
<tr>
<td>DATA_OUT.specific_time</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_OUT.time_stamp</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_OUT.time_uncertainty</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>IRQ_INVALID_SPECIFIC_TIME_ID</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

Table 15  RTL signals for `getSpecificTime()`
The dynamic behavior for `getSpecificTime()` is specified by the following chronogram:

![Chronogram](image)

**Figure 12** Dynamic behavior for `getSpecificTime()`

### 2.2.6 TimeService::SpecificTimes::SettingsNotification

#### 2.2.6.1 notifySpecificTimeSetting()

The RTL signals for `notifySpecificTimeSetting()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSF_(&lt;instNum&gt;<em>&lt;instNum&gt;</em>&lt;instNum&gt;<em>NOTIFY_SPECIFIC_TIME_SETTING</em> +</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.specific_time_id</td>
<td>FPGA app module</td>
<td>16-bit vector</td>
</tr>
<tr>
<td>DATA_IN.specific_time</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_IN.time_stamp</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_IN.time_uncertainty</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
</tbody>
</table>

**Table 16** RTL signals for `notifySpecificTimeSetting()`
The dynamic behavior for `notifySpecificTimeSetting()` is specified by the following chronogram:

![Figure 13 Dynamic behavior for notifySpecificTimeSetting()](image-url)

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3 FPGA PSM constants

This normative section specifies FPGA PSM constants.

3.1 PIM version

In accordance with the FPGA section of *WInnForum Facilities PSMs Mapping Rules* [Ref3], the `TSF_PIM_VERSION` constant is equal to `0x010100`. 
4 VHDL programming

This section specifies additional normative concepts supported by FPGA time services programmed using VHDL [Ref5], essentially through specification of VHDL packages to be used by conformant FPGA façades and FPGA applicative modules (see section 1.2).

The supported VHDL versions are vhdl-93 and all subsequent versions.

The specified VHDL packages have been successfully compiled using:
- Modelsim 10.4a,

4.1 VHDL library

The specified packages need to be compiled in tsf_api library.
4.2 pkg_tsf_api_types.vhd

The `pkg_tsf_api_types.vhd` file is defined as the standard VHDL package for the types of the FPGA PSM specification.

Specific types are introduced for `sourceId` and `specificTimeId` parameters, specified as `int` (not a valid IDL type) by Time Service Facility PIM Specification [Ref1].

The content of `pkg_tsf_api_types.vhd` is specified as:

```vhdl
library ieee;
use ieee.std_logic_1164.all;

package pkg_tsf_api_types is

  -- Constant reflecting version of the PIM Specification
  constant C_TSF_PIM_VERSION : std_logic_vector( 23 downto 0):= X"010100";

  -- SourceId_type (int in the [PIM], no dedicated type)
  subtype SourceId_type is std_logic_vector(7 downto 0);

  -- SpecificTimeId_type (int in the [PIM], no dedicated type)
  subtype SpecificTimeId_type is std_logic_vector(15 downto 0);

  -- TimeValue ([PIM] §3.4.1)
  -- struct TimeValue {
  --   long seconds,             // in seconds
  --   long nanoseconds};        // in nanoseconds (<1.000.000.000)
  --  const TimeValue UndefinedTime = {0xFFFFFFFF, 0xFFFFFFFF};
  type TimeValue_type is record
    seconds : std_logic_vector(31 downto 0);
    nanoseconds : std_logic_vector(31 downto 0);
  end record TimeValue_type;
  constant UndefinedTime : TimeValue_type := (
    seconds => X"FFFFFFFF",
    nanoseconds => X"FFFFFFFF"
  );

  -- TimeUncertainty ([PIM] §3.4.2)
  -- typedef long TimeUncertainty;
  subtype TimeUncertainty_type is std_logic_vector(31 downto 0);
  constant Beyond2SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFF0";
  constant Beyond4SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFF1";
  constant Beyond8SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFF2";
  constant Beyond16SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFF3";
  constant Beyond32SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFF4";
  constant Beyond64SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFF5";
  constant Beyond128SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFF6";
  constant Beyond256SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFF7";
  constant Beyond512SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFF8";
  constant Beyond1024SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFF9";
  constant Beyond2048SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFFA";
  constant Beyond4096SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFFB";
  constant Beyond8192SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFFC";
  constant Beyond16384SecTimeUncertainty : TimeUncertainty_type := X"FFFFFFFFD";
  constant UnknownTimeUncertainty : TimeUncertainty_type := X"FFFFFFFFE";
  constant UndefinedTimeUncertainty : TimeUncertainty_type := X"FFFFFFFF";

  -- RateUncertainty ([PIM] §3.4.3)
  -- typedef long RateUncertainty;
  subtype RateUncertainty_type is std_logic_vector(31 downto 0);

end package pkg_tsf_api_types;
```
constant UnknownRateUncertainty : RateUncertainty_type := X"FFFFFFFF";
end package pkg_tsf_api_types;
4.3  pkg_tsf_primitives_parameters.vhd

The file **pkg_tsf_primitives_parameters.vhd** is defined as the standard VHDL package for parameters of the FPGA PSM specification primitives.

For primitives with optional implementation of exceptions specified by the PIM specification, the corresponding dedicated 1-bit RTL signal is not specified in the VDHL file.

The content of **pkg_tsf_primitives_parameters.vhd** is specified as:

```vhdl
library ieee;
use ieee.std_logic_1164.all;

library tsf_api;
use tsf_api.pkg_tsf_api_types.all;

package pkg_tsf_primitives_parameters is

  -- TimeService::TerminalTime::TerminalTimeAccess ([PIM] §3.1.2)
  -- getTerminalTime ([PIM] §3.1.2.1.2)
  type getTerminalTime_outputType is record
    terminal_time : TimeValue_type;
  end record;
  -- PIM Exceptions: none

  -- getTerminalTimeUncertainty ([PIM] § 3.1.2.2.2)
  type getTerminalTimeUncertainty_outputType is record
    terminalTimeRateUncertainty : RateUncertainty_type;
  end record;
  -- PIM Exceptions: none

  -- TimeService::SystemTime::SystemTimeAccess([PIM] §3.1.3)
  -- getCurrentTAI ([PIM] §3.1.3.1.2)
  type getCurrentTAI_outputType is record
    currentTAI      : TimeValue_type;
    timeStamp       : TimeValue_type;
    timeUncertainty : TimeUncertainty_type;
  end record;
  -- PIM Exceptions: none

  -- getCurrentUTC ([PIM] §3.1.3.2.2)
  type getCurrentUTC_outputType is record
    currentUTC      : TimeValue_type;
    timeStamp       : TimeValue_type;
    timeUncertainty : TimeUncertainty_type;
  end record;
  -- PIM Exceptions: none

  -- getLastUpdateTAI ([PIM] §3.1.3.3.2)
  type getLastUpdateTAI_outputType is record
    lastUpdateTAI   : TimeValue_type;
    timeStamp       : TimeValue_type;
    timeUncertainty : TimeUncertainty_type;
  end record;
  -- PIM Exceptions: none

  -- getLastUpdateUTC ([PIM] §3.1.3.4.2)
  type getLastUpdateUTC_outputType is record
    lastUpdateUTC   : TimeValue_type;
    timeStamp       : TimeValue_type;
    timeUncertainty : TimeUncertainty_type;
end package pkg_tsf_primitives_parameters;
```
end record;
-- PIM Exceptions: none

-- TimeService::SystemTime::StandardTimeProvision ([PIM] §3.1.4)
-- provideTAI ([PIM] §3.1.4.1.2)
type provideTAI_inputType is record
  providedTAI : TimeValue_type;
  timeStamp : TimeValue_type;
  timeUncertainty : TimeUncertainty_type;
  sourceId : SourceId_type;
end record;
-- PIM Exceptions: none

-- TimeService::SystemTime::StandardTimeProvision ([PIM] §3.1.4)
-- provideUTC ([PIM] §3.1.4.2.2)
type provideUTC_inputType is record
  providedUTC : TimeValue_type;
  timeStamp : TimeValue_type;
  timeUncertainty : TimeUncertainty_type;
  sourceId : SourceId_type;
end record;
-- PIM Exceptions: FutureTimeStamp

-- TimeService::SystemTime::StandardTimeProvision ([PIM] §3.1.4)
-- notifyStandardTimeReference ([PIM] §3.1.5.1.2)
type notifyStandardTimeReference_inputType is record
  referenceTAI : TimeValue_type;
  referenceUTC : TimeValue_type;
  timeStamp : TimeValue_type;
  timeUncertainty : TimeUncertainty_type;
  sourceId : SourceId_type;
end record;
-- PIM Exceptions: none

-- TimeService::SpecificTimes::SpecificTimeHandling ([PIM] §3.1.6)
-- setSpecificTime ([PIM] §3.1.6.1.2)
type setSpecificTime_inputType is record
  specificTimeId : SpecificTimeId_type;
  specificTime : TimeValue_type;
  timeStamp : TimeValue_type;
  timeUncertainty : TimeUncertainty_type;
end record;
-- PIM Exceptions: FutureTimeStamp | InvalidSpecificTimeId

-- TimeService::SpecificTimes::SpecificTimeHandling ([PIM] §3.1.6)
-- getSpecificTime ([PIM] §3.1.6.2.2)
type getSpecificTime_inputType is record
  specificTimeId : SpecificTimeId_type;
end record;
type getSpecificTime_outputType is record
  specificTime : TimeValue_type;
  timeStamp : TimeValue_type;
  timeUncertainty : TimeUncertainty_type;
end record;
-- PIM Exceptions: InvalidSpecificTimeId

-- TimeService::SpecificTimes::SettingsNotification ([PIM] §3.1.7)
-- notifySpecificTimeSetting ([PIM] §3.1.7.1.2)
type notifySpecificTimeSetting_type is record
  specificTimeId : SpecificTimeId_type;
  specificTime : TimeValue_type;
  timeStamp : TimeValue_type;
  timeUncertainty : TimeUncertainty_type;
end record;
-- PIM Exceptions: none

end package pkg_tsf_primitives_parameters;
5 References

5.1 Referenced documents

   https://sds.wirelessinnovation.org/specifications-and-recommendations
   https://winnf.memberclicks.net/assets/work_products/Specifications/WINNF-TS-3004-V1.1.1.pdf

   https://sds.wirelessinnovation.org/specifications-and-recommendations

   https://sds.wirelessinnovation.org/specifications-and-recommendations
   https://winnf.memberclicks.net/assets/work_products/Reports/WINNF-TR-2008-V1.0.1.pdf

   https://en.wikipedia.org/wiki/Register-transfer_level


The URLs above were successfully accessed at release date.