Transceiver Facility FPGA PSM Specification

Document WINNF-TS-0008-App03

Version V2.1.1

22 January 2022
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<td>RTL signals for <code>scheduleRelativeBurst()</code></td>
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<td>11</td>
<td>RTL signals for <code>scheduleAbsoluteBurst()</code></td>
<td>8</td>
</tr>
<tr>
<td>12</td>
<td>RTL signals for <code>scheduleStrobedBurst()</code></td>
<td>9</td>
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<td>10</td>
</tr>
<tr>
<td>15</td>
<td>RTL signals for <code>pushRxBlock()</code></td>
<td>11</td>
</tr>
<tr>
<td>16</td>
<td>RTL signals for <code>pushTxBlock()</code></td>
<td>12</td>
</tr>
<tr>
<td>17</td>
<td>RTL signals for <code>setTuning()</code></td>
<td>13</td>
</tr>
<tr>
<td>18</td>
<td>RTL signals for <code>retune()</code></td>
<td>14</td>
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<tr>
<td>19</td>
<td>RTL signals for <code>notifyEvent()</code></td>
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<td>RTL signals for <code>lockGain()</code></td>
<td>17</td>
</tr>
<tr>
<td>23</td>
<td>RTL signals for <code>unlockGain()</code></td>
<td>18</td>
</tr>
<tr>
<td>24</td>
<td>RTL signals for <code>getCurrentTime()</code></td>
<td>18</td>
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<tr>
<td>25</td>
<td>RTL signals for <code>getLastStartTime()</code></td>
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<td>RTL signals for <code>triggerStrobe()</code></td>
<td>20</td>
</tr>
</tbody>
</table>
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Transceiver Facility FPGA PSM Specification

1 Introduction

This document WINNF-TS-0008-App03 is the FPGA PSM specification of Transceiver Facility V2.1.0.

It derives from Transceiver Facility PIM Specification [Ref1] in accordance with Principles for WinnForum Facility Standards [Ref2].

It addresses the FPGA programming paradigm, applying the mapping rules of the FPGA section of WinnForum Facilities PSMs Mapping Rules [Ref3] and specifically reporting any deviation to those rules.

The following figure positions the interfaces addressed by the FPGA PSM specification:

![Figure 1 - Positioning of FPGA PSM interfaces](image)

As depicted, the FPGA PSM specification addresses the FPGA functional interfaces of transceivers, positioned, within an FPGA node, between the FPGA applicative modules of radio applications and FPGA façades of transceiver instances.

The FPGA PSM specification considers RTL (Register-Transfer Level) [Ref4] interfaces, specifying RTL signals and the associated chronogram, independently from the used programming language (e.g., VHDL or Verilog).

It also provides normative source files applicable in case of VHDL programming.

1.1 Reference definitions

The Transceiver Facility FPGA PSM specification applies the following definitions from Transceiver Facility PIM Specification [Ref1]:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Used definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transceiver concepts</td>
<td>transceiver, Transceiver Facility, Tx channel, Rx channel</td>
</tr>
</tbody>
</table>

Table 1 Definitions from Transceiver Facility PIM Specification
The *Transceiver Facility FPGA PSM specification* applies the following definitions from *Principles for WInnForum Facility Standards* [Ref2]:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Used definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Base concepts</td>
<td>radio application</td>
</tr>
<tr>
<td>Architecture concepts</td>
<td>Façade</td>
</tr>
<tr>
<td>WInnForum facilities</td>
<td>facility, PIM specification, PSM specification</td>
</tr>
<tr>
<td>Services</td>
<td>Service</td>
</tr>
<tr>
<td>Primitives</td>
<td>primitive, parameter, exception, type</td>
</tr>
</tbody>
</table>

**Table 2 Definitions from Principles for WInnForum Facility Standards**

The *Transceiver Facility FPGA PSM specification* applies the following definitions from *WInnForum Facilities PSMs Mapping Rules* [Ref3]:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Used definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interfaces</td>
<td>FPGA PSM specification, FPGA functional interfaces</td>
</tr>
<tr>
<td>Software architecture</td>
<td>FPGA node, FPGA façade, FPGA applicative module</td>
</tr>
<tr>
<td>RTL signals origin</td>
<td>origin, caller, callee</td>
</tr>
<tr>
<td>Base RTL signals</td>
<td>primitive prefix, structural RTL signals, semantics RTL signals, parameters RTL signals, exception RTL signals</td>
</tr>
</tbody>
</table>

**Table 3 Definitions from WInnForum Facilities PSMs Mapping Rules**

The term “unspecified” indicates an aspect explicitly left to implementer’s decisions.

### 1.2 Conformance

#### 1.2.1 Radio platform items

An *FPGA façade* of a *transceiver* implementation is **conformant with** the Transceiver Facility *FPGA PSM specification* if it provides an FPGA implementation of related *primitives*.

An *FPGA transceiver* is **defined as** a *transceiver* implementation with all of its *FPGA façades* being conformant with the *FPGA PSM specification*.

#### 1.2.2 Radio application items

An *FPGA applicative module* of a *radio application* is **conformant with** the Transceiver Facility *FPGA PSM specification* if it can use *FPGA façades* conformant with the *FPGA PSM specification* without using any non-standard *primitive* for the *transceiver*.

### 1.3 Document structure

Section 2 specifies the normative content for the *FPGA functional interfaces*.

Section 3 specifies the normative content for FPGA constants.

Section 4 specifies the normative files to be used for VHDL programming.
2 FPGA functional interfaces

This normative section specifies the FPGA functional interfaces for transceiver, according to the FPGA section of WInnForum Facilities PSMs Mapping Rules [Ref3].

2.1 Specification approach

2.1.1 Base RTL signals

The following base RTL signals from the FPGA section of WInnForum Facilities PSMs Mapping Rules [Ref3] are used:

<table>
<thead>
<tr>
<th>Base RTL signal</th>
<th>Used definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Structural RTL signals</td>
<td>CLK, RST</td>
</tr>
<tr>
<td>Semantics RTL signals</td>
<td>EN, RDY</td>
</tr>
<tr>
<td>Parameters RTL signals</td>
<td>EN_IN, DATA_IN, EN_OUT, DATA_OUT</td>
</tr>
<tr>
<td>Exception RTL signals</td>
<td>IRQ</td>
</tr>
</tbody>
</table>

Table 4 Base RTL signals from WInnForum Facilities PSMs Mapping Rules

For each base RTL signal, the complete RTL signal name, its origin (using the concept of caller and callee) and its format are specified.

2.1.2 Primitive prefixes

The primitive prefixes for transceiver follow the related indications of WInnForum Facilities PSMs Mapping Rules, with the transceiver-specific addition of <CHAN> field.

A primitive prefix concatenates:

- The XCVR field, for transceiver,
- The <instNum> field, optionally numbering instances of a transceiver in case there are more than one (starting count from 1),
- The <CHAN> field indicating if an RTL signal is attached to Tx channels or Rx channels with, for SamplesTransmission and SamplesReception, the Tx channel or Rx channel number,
- The <PRIM_NAME> field, identifying the primitive using a screaming snake case transcription of the PIM specification name.
The value of `<CHAN>` is specified by the following table:

<table>
<thead>
<tr>
<th><code>&lt;CHAN&gt;</code> value</th>
<th>Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>For Services attached to Tx channels. Including <strong>SamplesTransmission</strong> if only one Tx channel is used.</td>
</tr>
<tr>
<td>RX</td>
<td>The Services attached to Rx channels. Including <strong>SamplesReception</strong> if only one Rx channel is used.</td>
</tr>
<tr>
<td>TX&lt;channelNumber&gt;</td>
<td>For <strong>SamplesTransmission</strong> if several Tx channels are used, starting at 1.</td>
</tr>
<tr>
<td>RX&lt;channelNumber&gt;</td>
<td>For <strong>SamplesReception</strong> if several Rx channels are used, starting at 1.</td>
</tr>
</tbody>
</table>

Table 5 Possible values for `<CHAN>`

### 2.1.3 Stream-oriented design

A stream-oriented design, keeping the notion of baseband samples block and completely suppressing the notion of baseband samples packet, is introduced for **SamplesReception** (see section 2.2.8) and **SamplesTransmission** (see section 2.2.9) Services.

The PIM primitives `pushTxPacket()` and `pushRxPacket()` are replaced by the substitute primitives `pushTxBlock()` and `pushRxBlock()`, which are then mapped to an FPGA interface:

- One-by-one transfers of baseband samples are realized over the length of the block,
- The main parameter becomes **in BasebandBlock sequence<BasebandSamples>**,
- Parameter **endOfBlock** is suppressed.

The `RxPacketsLengthControl` service is not mapped, implying:

- Operation `setRxPacketsLength()` is not mapped,
- Type `PacketsLength` is not mapped.

### 2.2 Interfaces specification

#### 2.2.1 Transceiver::Management::Reset

2.2.1.1 reset()

The RTL signals for `reset()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>XCVR_{&lt;instNum&gt;_}_&lt;CHAN&gt;_RESET_+</code></td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_OUT</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

Table 6 RTL signals for `reset()`
The dynamic behavior for \texttt{reset()} is specified by the following chronogram:

![Chronogram](image)

\textbf{Figure 2 Dynamic behavior for \texttt{reset()}}

\subsection{Transceiver::Management::RadioSilence}

\subsubsection{startRadioSilence()}

The RTL signals for \texttt{startRadioSilence()} are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{XCVR}<em>{&lt;\texttt{instNum}&gt;}</em>{&lt;\texttt{CHAN}&gt;}_\texttt{START_RADIO_SILENCE}+</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>\texttt{CLK}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>\texttt{RST}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>\texttt{EN}</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\textbf{Table 7 RTL signals for \texttt{startRadioSilence()}}

The dynamic behavior for \texttt{startRadioSilence()} is specified by the following chronogram:

![Chronogram](image)

\textbf{Figure 3 Dynamic behavior for \texttt{startRadioSilence()}}

\subsubsection{stopRadioSilence()}

The RTL signals for \texttt{stopRadioSilence()} are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{XCVR}<em>{&lt;\texttt{instNum}&gt;}</em>{&lt;\texttt{CHAN}&gt;}_\texttt{STOP_RADIO_SILENCE}+</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>\texttt{CLK}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>\texttt{RST}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>\texttt{EN}</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\textbf{Table 8 RTL signals for \texttt{stopRadioSilence()}}
The dynamic behavior for `stopRadioSilence()` is specified by the following chronogram:

![Figure 4 Dynamic behavior for stopRadioSilence()](image)

### 2.2.3 Transceiver::BurstControl::DirectCreation

#### 2.2.3.1 startBurst()

The RTL signals for `startBurst()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCVR_{&lt;instNum&gt;_}&lt;CHAN&gt;<em>START_BURST</em>+</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.requested_length</td>
<td>FPGA app module</td>
<td>32-bit vector</td>
</tr>
<tr>
<td>START_BURST_RDY</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

![Table 9 RTL signals for startBurst()](image)

The dynamic behavior for `startBurst()` is specified by the following chronogram:

![Figure 5 Dynamic behavior for startBurst()](image)
2.2.4 Transceiver::BurstControl::RelativeCreation

2.2.4.1 scheduleRelativeBurst()

The RTL signals for `scheduleRelativeBurst()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>XCVR_{&lt;instNum&gt;_}_&lt;CHAN&gt;_SCHEDULE_RELATIVE_BURST_+</code></td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.requested_alternate</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.requested_delay</td>
<td>FPGA app module</td>
<td>32-bit or 64-bit vector</td>
</tr>
<tr>
<td>DATA_IN.requested_length</td>
<td>FPGA app module</td>
<td>32-bit vector</td>
</tr>
<tr>
<td>RDY</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

Table 10 RTL signals for `scheduleRelativeBurst()`

The dynamic behavior for `scheduleRelativeBurst()` is specified by the following chronogram:

![Figure 6 Dynamic behavior for scheduleRelativeBurst()](image)

Figure 6 Dynamic behavior for `scheduleRelativeBurst()`
2.2.5 *Transceiver::BurstControl::AbsoluteCreation*

2.2.5.1 *scheduleAbsoluteBurst()*

The RTL signals for *scheduleAbsoluteBurst()* are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.requested_start_time</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
<tr>
<td>DATA_IN.requested_length</td>
<td>FPGA app module</td>
<td>32-bit vector</td>
</tr>
<tr>
<td>RDY</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

Table 11 RTL signals for *scheduleAbsoluteBurst()*

The dynamic behavior for *scheduleAbsoluteBurst()* is specified by the following chronogram:

![Figure 7 Dynamic behavior for scheduleAbsoluteBurst()](image)
2.2.6  Transceiver::BurstControl::StrobedCreation

2.2.6.1  scheduleStrobedBurst()

The RTL signals for `scheduleStrobedBurst()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>XCVR_{&lt;instNum&gt;_}&lt;CHAN&gt;_SCHEDULE_STROBED_BURST</code></td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.requested_strobe_source</td>
<td>FPGA app module</td>
<td>16-bit vector</td>
</tr>
<tr>
<td>DATA_IN.requested_delay</td>
<td>FPGA app module</td>
<td>32-bit or 64-bit vector</td>
</tr>
<tr>
<td>DATA_IN.requested_length</td>
<td>FPGA app module</td>
<td>32-bit vector</td>
</tr>
<tr>
<td>RDY</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

Table 12  RTL signals for `scheduleStrobedBurst()`

The dynamic behavior for `scheduleStrobedBurst()` is specified by the following chronogram:

![Figure 8  Dynamic behavior for scheduleStrobedBurst()](image)
2.2.7 Transceiver::BurstControl::Termination

2.2.7.1 setBlockLength()

The RTL signals for `setBlockLength()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>XCVR_{&lt;instNum&gt;_}_&lt;CHAN&gt;_SET_BLOCK_LENGTH</code> +</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.requested_length</td>
<td>FPGA app module</td>
<td>32-bit vector</td>
</tr>
</tbody>
</table>

Table 13 RTL signals for `setBlockLength()`

The dynamic behavior for `setBlockLength()` is specified by the following chronogram:

![Figure 9 Dynamic behavior for setBlockLength()](image)

2.2.7.2 stopBurst()

The RTL signals for `stopBurst()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>XCVR_{&lt;instNum&gt;_}_&lt;CHAN&gt;_STOP_BURST</code> +</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

Table 14 RTL signals for `stopBurst()`

The dynamic behavior for `stopBurst()` is specified by the following chronogram:

![Figure 10 Dynamic behavior for stopBurst()](image)
2.2.8 Transceiver::BasebandSignal::SamplesReception

2.2.8.1 pushRxPacket()/pushRxBlock()

The stream-oriented design explained in section 2.1.3 is applied, with the PIM primitive `pushRxPacket()` being replaced by `pushRxBlock()`, with a sequence of baseband samples as the only in parameter, no out parameter.

No flow control mechanism is required for reception.

The transmission of meta-data, as specified by value of `RX_META_DATA`, is directly using transmission of data of type `rx_meta_data_type`.

The RTL signals for `pushRxBlock()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>XCVR_{&lt;instNum&gt;_&gt;&lt;CHAN&gt;_PUSH_RX_BLOCK_+</code></td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>BASEBAND_SAMPLE_FIRST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>BASEBAND_SAMPLE_LAST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>BASEBAND_SAMPLE_EN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>BASEBAND_SAMPLE_DATA</td>
<td>FPGA façade</td>
<td>Two 16-bit or 32-bit vectors</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.rx_meta_data</td>
<td>FPGA app module</td>
<td>User-defined</td>
</tr>
</tbody>
</table>

Table 15 RTL signals for `pushRxBlock()`

The dynamic behavior for `pushRxBlock()` is specified by the following chronogram:

Figure 11 Dynamic behavior for `pushRxBlock()`
2.2.9 Transceiver::BasebandSignal::SamplesTransmission

2.2.9.1 pushTxPacket()/pushTxBlock()

The stream-oriented design explained in section 2.1.3 is applied, with the PIM primitive `pushTxPacket()` being replaced by `pushTxBlock()`, with a sequence of baseband samples as the only in parameter, no out parameter.

Flow control signaling is added to ensure transmission integrity.

The transmission of meta-data, as specified by value of `TX_META_DATA`, is directly using transmission of data of type `tx_metadata_type`.

The RTL signals for `pushTxBlock()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>BASEBAND_SAMPLE_FIRST</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>BASEBAND_SAMPLE_LAST</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>BASEBAND_SAMPLE_EN</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>BASEBAND_SAMPLE_RDY</td>
<td>FPGA app module</td>
<td>2 16-bit or 32-bit vectors</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN</td>
<td>FPGA app module</td>
<td>User-defined</td>
</tr>
</tbody>
</table>

Table 16 RTL signals for `pushTxBlock()`
The dynamic behavior for `pushTxBlock()` is specified by the following chronogram:

![Figure 12 Dynamic behavior for pushTxBlock()](image)

### 2.2.10 Transceiver::BasebandSignal::RxPacketsLengthControl

Not mapped.

### 2.2.11 Transceiver::Tuning::InitialTuning

#### 2.2.11.1 setTuning()

The RTL signals for `setTuning()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>XCVR_{&lt;instNum&gt;_}_&lt;CHAN&gt;_SET_TUNING</code> +</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA app module</td>
<td>16-bit vector</td>
</tr>
<tr>
<td><code>DATA_IN.requested_preset</code></td>
<td>FPGA app module</td>
<td>32-bit or 64-bit vector</td>
</tr>
<tr>
<td><code>DATA_IN.requested_frequency</code></td>
<td>FPGA app module</td>
<td>16-bit vector – signed</td>
</tr>
<tr>
<td><code>DATA_IN.requested_gain</code></td>
<td>FPGA app module</td>
<td>16-bit vector</td>
</tr>
<tr>
<td><code>DATA_IN.requested_burst_number</code></td>
<td>FPGA app module</td>
<td>16-bit vector</td>
</tr>
<tr>
<td>RDY</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

Table 17 RTL signals for `setTuning()`
The dynamic behavior for `setTuning()` is specified by the following chronogram:

![Chronogram for setTuning()](image)

**Figure 13  Dynamic behavior for setTuning()**

### 2.2.12 Transceiver::Tuning::Retuning

#### 2.2.12.1 retune()

The RTL signals for `retune()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>XCVR_{&lt;instNum&gt;}_&lt;CHAN&gt;_RETUNE_</code> +</td>
<td><strong>FPGA façade</strong></td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td><strong>FPGA façade</strong></td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td><strong>FPGA app module</strong></td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td><strong>FPGA app module</strong></td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.requested_frequency</td>
<td><strong>FPGA app module</strong></td>
<td>32-bit or 64-bit vector</td>
</tr>
<tr>
<td>DATA_IN.requested_gain</td>
<td><strong>FPGA app module</strong></td>
<td>16-bit vector</td>
</tr>
<tr>
<td>DATA_IN.requested_delay</td>
<td><strong>FPGA app module</strong></td>
<td>32-bit or 64-bit vector</td>
</tr>
</tbody>
</table>

**Table 18  RTL signals for retune()**
The dynamic behavior for `retune()` is specified by the following chronogram:

![Chronogram for retune()](image1)

**Figure 14** Dynamic behavior for `retune()`

### 2.2.13 Transceiver::Notifications::Events

#### 2.2.13.1 notifyEvent()

The RTL signals for `notifyEvent()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>XCVR_{&lt;instNum&gt;_}_&lt;CHAN&gt;_NOTIFY_EVENT_ +</code></td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.notified_event</td>
<td>FPGA façade</td>
<td>3-bit vector</td>
</tr>
</tbody>
</table>

*Table 19* RTL signals for `notifyEvent()`

The dynamic behavior for `notifyEvent()` is specified by the following chronogram:

![Chronogram for notifyEvent()](image2)

**Figure 15** Dynamic behavior for `notifyEvent()`
2.2.14 Transceiver::Notifications::Errors

2.2.14.1 notifyError()

The RTL signals for notifyError() are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCVR_{&lt;instNum&gt;<em>}</em>&lt;CHAN&gt;<em>NOTIFY_ERROR</em>+</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.notified_error</td>
<td>FPGA façade</td>
<td>4-bit vector</td>
</tr>
</tbody>
</table>

Table 20 RTL signals for notifyError()

The dynamic behavior for notifyError() is specified by the following chronogram:

![Figure 16 Dynamic behavior for notifyError()](image)

2.2.15 Transceiver::GainControl::GainChanges

2.2.15.1 indicateGain()

The RTL signals for indicateGain() are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCVR_{&lt;instNum&gt;<em>}</em>&lt;CHAN&gt;<em>INDICATE_GAIN</em>+</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_IN.new_gain</td>
<td>FPGA façade</td>
<td>16-bit vector -- signed</td>
</tr>
<tr>
<td>DATA_IN.first_valid_sample</td>
<td>FPGA façade</td>
<td>32-bit vector</td>
</tr>
</tbody>
</table>

Table 21 RTL signals for indicateGain()
The dynamic behavior for *indicateGain()* is specified by the following chronogram:

![Figure 17 Dynamic behavior for indicateGain()](image)

### 2.2.16 Transceiver::GainControl::GainLocking

2.2.16.1 lockGain()

The RTL signals for *lockGain()* are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCVR_{&lt;instNum&gt;<em>}</em>&lt;CHAN&gt;<em>LOCK_GAIN</em>+</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RST</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

Table 22 RTL signals for *lockGain()*

The dynamic behavior for *lockGain()* is specified by the following chronogram:

![Figure 18 Dynamic behavior for lockGain()](image)
2.2.16.2 unlockGain()

The RTL signals for *unlockGain()* are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCVR_{&lt;instNum&gt;_} &lt;CHAN&gt;<em>UNLOCK_GAIN</em>+</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

Table 23  RTL signals for *unlockGain()*

The dynamic behavior for *unlockGain()* is specified by the following chronogram:

![Dynamic behavior for unlockGain()](image)

**Figure 19** Dynamic behavior for *unlockGain()*

2.2.17 Transceiver::TransceiverTime::TimeAccess

2.2.17.1 getCurrentTime()

The RTL signals for *getCurrentTime()* are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCVR_{&lt;instNum&gt;_} &lt;CHAN&gt;<em>GET_CURRENT_TIME</em>+</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_IN</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>EN_OUT</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>DATA_OUT.current_time</td>
<td>FPGA app module</td>
<td>Two 32-bit vectors</td>
</tr>
</tbody>
</table>

Table 24  RTL signals for *getCurrentTime()*
The dynamic behavior for `getCurrentTime()` is specified by the following chronogram:

![Figure 20 Dynamic behavior for `getCurrentTime()`](image)

### 2.2.17.2 `getLastStartTime()`

The RTL signals for `getLastStartTime()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>XCVR_{&lt;instNum&gt;_&lt;_CHAN&gt;_GET_LAST_START_TIME_+_</code></td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RST</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN_IN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN_OUT</td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>DATA_OUT.last_start_time</code></td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
<tr>
<td><code>DATA_OUT.last_burst_number</code></td>
<td></td>
<td>Two 32-bit vectors</td>
</tr>
</tbody>
</table>

**Table 25 RTL signals for `getLastStartTime()`**

The dynamic behavior for `getLastStartTime()` is specified by the following chronogram:

![Figure 21 Dynamic behavior for `getLastStartTime()`](image)
2.2.18 Transceiver::Strobing::ApplicationStrobe

2.2.18.1 triggerStrobe()

The RTL signals for `triggerStrobe()` are specified by the following table:

<table>
<thead>
<tr>
<th>RTL signal name</th>
<th>Origin</th>
<th>Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>XCVR_{&lt;instNum&gt;<em>}&lt;CHAN&gt; TRIGGER_STROBE</em>+</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>CLK</td>
<td>FPGA façade</td>
<td>1-bit signal</td>
</tr>
<tr>
<td>RST</td>
<td>FPGA app module</td>
<td>1-bit signal</td>
</tr>
</tbody>
</table>

Table 26 RTL signals for `triggerStrobe()`

The dynamic behavior for `triggerStrobe()` is specified by the following chronogram:

Figure 22 Dynamic behavior for `triggerStrobe()`
3  FPGA PSM constants

This normative section specifies FPGA PSM constants.

3.1  PIM version

In accordance with the FPGA section of *WInnForum Facilities PSMs Mapping Rules* [Ref3], the `XCVR_PIM_VERSION` constant is equal to `0x020100`. 
4 VHDL programming

This section specifies additional normative concepts supported by FPGA transceivers programmed using VHDL [Ref5], essentially through specification of VHDL packages to be used by conformant FPGA façades and FPGA applicative modules (see section 1.2).

The supported VHDL versions are vhdl-93 and all subsequent versions.

The specified VHDL packages have been successfully compiled using:

- Modelsim 10.4a,

4.1 VHDL library

The specified packages need to be compiled in xcvr_api library.

4.2 pkg_xcvr_interface_declaration_properties.vhd

The pkg_xcvr_interface_declaration_properties.vhd file is defined as the standard VHDL package for handling of interface declaration properties.

The content of pkg_xcvr_interface_declaration_properties.vhd is specified as:

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

-- Interface declaration properties ([PIM] §4.5)
package pkg_xcvr_interface_declaration_properties is

  -- 1) Variable types properties (CARRIER_FREQ_TYPE, CARRIER_FREQ_TYPE, CARRIER_FREQ_TYPE)
  -- Enumerated values constants
  -- int16
  constant C_INT16 : std_logic_vector( 1 downto 0) := "00";
  -- int32
  constant C_INT32 : std_logic_vector( 1 downto 0) := "01";
  -- int64
  constant C_INT64 : std_logic_vector( 1 downto 0) := "10";
  -- float32: not mapped
```

-- Setting of enumerated values
-- enum CARRIER_FREQ_TYPE {int32, int64};
constant C_CARRIER_FREQ_TYPE : std_logic_vector( 1 downto 0) := <C_INT32|C_INT64>; -- USER SELECTION REQUIRED

-- enum DELAY_TYPE {int32, int64};
constant C_DELAY_TYPE : std_logic_vector( 1 downto 0) := <C_INT32|C_INT64>; -- USER SELECTION REQUIRED

-- enum IQ_TYPE {int16, int32, float32};
constant C_IQ_TYPE : std_logic_vector( 1 downto 0) := <C_INT16|C_INT32>; -- USER SELECTION REQUIRED

-- Setting of enumerated values
-- enum CARRIER_FREQ_TYPE {int32, int64};
constant C_CARRIER_FREQ_VECTOR_SIZE : natural;

-- enum DELAY_TYPE {int32, int64};
constant C_DELAY_VECTOR_SIZE : natural;

-- enum IQ_TYPE {int16, int32, float32};
constant C_IQ_VECTOR_SIZE : natural;
-- float32: not mapped

-- 2) Optional meta-data properties
-- boolean TX_META_DATA
constant C_TX_META_DATA : std_logic := '<1|0>'; -- USER SELECTION REQUIRED
-- boolean RX_META_DATA
constant C_RX_META_DATA : std_logic := '<1|0>'; -- USER SELECTION REQUIRED

end package pkg_xcvr_interface_declaration_properties;

package body pkg_xcvr_interface_declaration_properties is
  function set_carrier_freq_vector_size(constant_type : in std_logic_vector(1 downto 0)) return natural is
    begin
      if (constant_type = C_INT32) then
        return 32;
      elsif (constant_type = C_INT64) then
        return 64;
      else
        assert false report "<C_INT32|C_INT64>" severity error;
        return 32;
      end if;
    end set_carrier_freq_vector_size;

  function set_delay_vector_size(constant_type : in std_logic_vector(1 downto 0)) return natural is
    begin
      if (constant_type = C_INT32) then
        return 32;
      elsif (constant_type = C_INT64) then
        return 64;
      else
        assert false report "<C_INT32|C_INT64>" severity error;
        return 32;
      end if;
    end set_delay_vector_size;
function set_iq_vector_size(constant_type : in std_logic_vector(1 downto 0)) return natural is
  begin
    if (constant_type = C_INT16) then
      return 16;
    elsif (constant_type = C_INT32) then
      return 32;
    else
      assert false report "<C_INT16|C_INT32>" severity error;
      return 16;
    end if;
  end set_iq_vector_size;

-- Resulting vector sizes computations
-- enum CARRIER_FREQ_TYPE {int32, int64};
constant C_CARRIER_FREQ_VECTOR_SIZE : natural :=
  set_carrier_freq_vector_size( C_CARRIER_FREQ_TYPE);

-- enum DELAY_TYPE {int32, int64};
constant C_DELAY_VECTOR_SIZE : natural :=
  set_delay_vector_size( C_DELAY_TYPE);

-- enum IQ_TYPE {int16, int32, float32};
constant C_IQ_VECTOR_SIZE : natural :=
  set_iq_vector_size( C_IQ_TYPE);
-- float32: not mapped
end package body pkg_xcvr_interface_declaration_properties;

The user has to adapt pkg_xcvr_interface_declaration_properties.vhd in selecting the property value in lines commented with "-- USER SELECTION REQUIRED".
4.3 pkg_xcvr_api_types.vhd

The pkg_xcvr_api_types.vhd file is defined as the standard VHDL package for the types of the FPGA PSM specification.

The content of pkg_xcvr_api_types.vhd is specified as:

```vhdl
library ieee;
use ieee.std_logic_1164.all;

library xcvr_api;
use xcvr_api.pkg_xcvr_interface_declaration_properties.all;

package pkg_xcvr_api_types is

  -- Constant reflecting value of XCVR_PIM_VERSION property
  constant C_XCVR_PIM_VERSION : std_logic_vector( 23 downto 0):= X"020100";

  -- BasebandPacket ([PIM] §3.4.2) : the FPGA PSM does not use the concept of
  -- packets for baseband samples exchange; each baseband sample is
  -- transferred
  -- individually within the digital stream
  -- BlockLength ([PIM] §3.4.3)
  -- typedef unsigned long BlockLength;
  subtype block_length_type is std_logic_vector( 31 downto 0);
  constant C_UNDEFINED_BLOCK_LENGTH : block_length_type := (others => '1');

  -- IQ ([PIM] §3.4.11)
  -- typedef <short|long|float> IQ
  subtype iq_type is std_logic_vector( C_IQ_VECTOR_SIZE-1 downto 0);

  -- BasebandSample ([PIM] §3.4.4)
  -- struct BasebandSample {IQ valueI, IQ valueQ};
  type baseband_sample_type is record
    valueI : iq_type;
    valueQ : iq_type;
  end record;

  -- BurstNumber ([PIM] §3.3.5)
  -- typedef unsigned long BurstNumber;
  subtype burst_number_type is std_logic_vector( 15 downto 0);

  -- CarrierFreq ([PIM] §3.4.6), in Hz
  -- typedef <unsigned long|unsigned long long> CarrierFreq
  subtype carrier_freq_type is std_logic_vector( C_CARRIER_FREQ_VECTOR_SIZE-1
downto 0);

  -- const CarrierFreq UndefinedCarrierFreq = <0xFFFFFFFF | 0xFFFFFFFF>
  constant C_UNDEFINED_CARRIER_FREQ : carrier_freq_type := (others => '1');

  -- Delay ([PIM] §3.4.7), in ns
  -- typedef <unsigned long|unsigned long long> Delay
  subtype delay_type is std_logic_vector( C_DELAY_VECTOR_SIZE-1 downto 0);

  -- const Delay UndefinedDelay = <0xFFFFFFFF | 0xFFFFFFFF>
  constant C_UNDEFINED_DELAY : delay_type := (others => '1');

end package pkg_xcvr_api_types;
```

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-- Error ([PIM] §3.4.8)
-- enum Error { errorDelayedTuning, ... 
subtype error_type is std_logic_vector( 3 downto 0);
constant C_DELAYED_TUNING_ERROR : error_type := X"0";
constant C_TUNING_TIMEOUT_ERROR : error_type := X"1";
constant C_FIRST_SAMPLE_TIMEOUT_ERROR : error_type := X"2";
constant C_TRANSMISSION_UNDERFLOW_ERROR : error_type := X"3";
constant C_RECEPTION_OVERFLOW_ERROR : error_type := X"4";
constant C_SHORTER_TRANMITTED_BLOCK_ERROR : error_type := X"5";
constant C_LONGER_TRANMITTED_BLOCK_ERROR : error_type := X"6";
constant C_UNDEFINED_GAIN : gain_type := (others => '1');
-- MetaData ([PIM] §3.4.12): specified by pkg_xcvr_metadata_types.vhd
-- PacketLength ([PIM] §3.4.13): not mapped
-- SampleNumber ([PIM] §3.4.14)
-- typedef unsigned long SampleNumber;
subtype sample_number_type is std_logic_vector( 31 downto 0);
-- StrobeSource ([PIM] §3.4.15)
-- enum StrobeSource ( ApplicationStrobe,... 
subtype strobe_source_type is std_logic_vector( 3 downto 0);
constant C_APPLICATION_STROBE : strobe_source_type := X"0";
constant C_TIME_REF_PPS : strobe_source_type := X"1";
constant C_GNSS_PPS : strobe_source_type := X"2";
constant C_USER_STROBE_1 : strobe_source_type := X"3";
constant C_USER_STROBE_2 : strobe_source_type := X"4";
constant C_USER_STROBE_3 : strobe_source_type := X"5";
constant C_USER_STROBE_4 : strobe_source_type := X"6";
-- TimeSpec ([PIM] §3.4.16)
-- struct TimeSpec ( unsigned long seconds, unsigned long nanoseconds);
type time_spec_type is record
  seconds  : std_logic_vector( 31 downto 0);  -- in seconds
  nanoseconds : std_logic_vector( 31 downto 0);  -- in ns (<1.000.000.000)
end record;
-- const TimeSpec UndefinedTimeSpec = (0xFFFFFFFF, 0xFFFFFFFF);
constant C_UNDEFINED_TIME_SPEC : time_spec_type := (others => (others => '1'));
4.4 pkg_xcvr_metadata_types.vhd

The file `pkg_xcvr_metadata_types.vhd` is defined as the standard VHDL package used to declare meta-data types.

It is applicable if `TX_META_DATA` or `RX_META_DATA` is equal to `TRUE`.

The content of `pkg_xcvr_metadata_types.vhd` is specified as:

```vhdl
library ieee;
use ieee.std_logic_1164.all;

library xcvr_api;
use xcvr_api.pkg_xcvr_interface_declaration_properties.all;
use xcvr_api.pkg_xcvr_api_types.all;

package pkg_xcvr_metadata_types is

  -- MetaData ([PIM] §3.4.12)
  -- typedef struct TxMetaData (keep if C_TX_META_DATA = '1')
  type tx_metadata_type is record
    <user-defined>;   -- USER-DEFINED FIELDS
  end record;

  -- typedef struct RxMetaData (keep if C_RX_META_DATA = '1')
  type rx_metadata_type is record
    <user-defined>;   -- USER-DEFINED FIELDS
  end record;

end package pkg_xcvr_metadata_types;
```

The user has to adapt `pkg_xcvr_metadata_types.vhd` to declare the fields composing `tx_metadata_type` and/or `rx_metadata_typelines` using the lines identified with the comment "-- USER-DEFINED FIELDS".
4.5 pkg_xcvr_primitives_parameters.vhd

The file **pkg_xcvr_primitives_parameters.vhd** is defined as the standard VHDL package for the parameters of the FPGA PSM specification primitives.

For primitives with optional implementation of exceptions specified by the PIM specification, the corresponding dedicated 1-bit RTL signal is not specified in the VDHL file.

The content of **pkg_xcvr_primitives_parameters.vhd** is specified as:

```vhdl
library ieee;
use ieee.std_logic_1164.all;

library xcvr_api;
use xcvr_api.pkg_xcvr_api_types.all;
use xcvr_api.pkg_xcvr_metadata_types.all;

package pkg_xcvr_primitives_parameters is

-- Management::Reset ([PIM] §2.4.1.1)
-- reset() has no parameters
-- PIM Exceptions: none

-- Management::RadioSilence ([PIM] §2.4.1.2)
-- startRadioSilence() and stopRadioSilence() have no parameters
-- PIM Exceptions: none

-- BurstControl::DirectCreation ([PIM] §2.4.2.1)
-- startBurst()
type start_burst_in is record
  requested_length: block_length_type;
end record;
-- PIM Exceptions: MinBlockLength, MaxBlockLength

-- BurstControl::RelativeCreation ([PIM] §2.4.2.2)
-- scheduleRelativeBurst()
type schedule_relative_burst_in_type is record
  requested_alternate : std_logic;
  requested_delay : delay_type;
  requested_length : block_length_type;
end record;
-- PIM Exceptions: NoAlternateReferencing, MinFromPrevious, MaxFromPrevious,
-- MinBlocklength, MaxBlockLength, RelativeMILT

-- BurstControl::AbsoluteCreation ([PIM] §2.4.2.3)
-- scheduleAbsoluteBurst()
type schedule_absolute_burst_in_type is record
  requested_start_time : time_spec_type;
  requested_length : block_length_type;
end record;
-- PIM Exceptions: MaxNanoseconds, MinBlockLength, MaxBlockLength,
-- AbsoluteMILT
```


-- BurstControl::StrobedCreation ([PIM] §2.4.2.4)
-- scheduleStrobedBurst()
type schedule_strobed_burst_in_type is record
  requested_strobe_source : strobe_source_type;
  requested_delay : delay_type;
  requested_length : block_length_type;
end record;
-- PIM Exceptions: StrobeSource, MinFromStrobe, MaxFromStrobe,
-- MinBlockLength, MaxBlockLength

-- BurstControl::Termination ([PIM] §2.4.2.5)
-- setBlockLength()
type set_block_length_in_type is record
  requested_length : block_length_type;
end record;
-- PIM Exceptions: NoOngoingProcessing, MinBlockLength, MaxBlockLength

-- stopBurst() has no parameter
-- PIM Exceptions: NoOngoingProcessing

-- BasebandSignal::SamplesReception ([PIM] §2.4.3.1)
-- pushRxBlock(), replacing pushRxPacket()
type push_rx_block_in_sample_type is record
  rx_baseband_sample : baseband_sample_type;
end record;
type push_rx_block_in_metadata_type is record
  rx_meta_data : rx_metadata_type;
end record;
-- PIM Exceptions: none

-- BasebandSignal::SamplesTransmission ([PIM] §2.4.3.2)
-- pushTxBlock(), replacing pushTxPacket()
type push_tx_block_in_sample_type is record
  tx_baseband_sample : baseband_sample_type;
end record;
type push_tx_block_in_metadata_type is record
  tx_meta_data : tx_metadata_type;
end record;
-- PIM Exceptions: MaxTxPacketsLength, TxPacketsMILT

-- BasebandSignal::RxPacketsLengthControl ([PIM] §2.4.3.3): not mapped
-- setRxPacketsLength(): not mapped

-- Tuning::InitialTuning ([PIM] §2.4.4.1)
-- setTuning()
type set_tuning_in_type is record
  requested_preset : tuning_preset_type;
  requested_frequency : carrier_freq_type;
  requested_gain : gain_type;
  requested_burst_number : burst_number_type;
end record;
-- PIM Exceptions: MaxTuningPreset, MinCarrierFreq, MaxCarrierFreq,
-- MinGain, MaxGain, TuningMILT
package pkg_xcvr_primitives_parameters;

-- Tuning::Retuning ([PIM] §2.4.4.2)
-- retune()
type retune_in_type is record
    requested_frequency : carrier_freq_type;
    requested_gain : gain_type;
    requested_delay : delay_type;
end record;
-- PIM Exceptions: NoOngoingProcessing, MinCarrierFreq, MaxCarrierFreq,
-- MinGain, MaxGain, MinFromOnGoing, MaxFromOnGoing, RetuningMILT

-- Notifications::Events ([PIM] §2.4.5.1)
-- notifyEvent()

-- notify_event_in_type is record
    notified_event : event_type;
end record;
-- PIM Exceptions: none

-- Notifications::Errors ([PIM] §2.4.5.2)
-- notifyError()

-- notify_error_in_type is record
    notified_error : error_type;
end record;
-- PIM Exceptions: none

-- GainControl::GainChanges ([PIM] §2.4.6.1)
-- indicateGain()

-- indicate_gain_in_type is record
    new_gain : gain_type;
    first_valid_sample : sample_number_type;
end record;
-- PIM Exceptions: none

-- GainControl::GainLocking ([PIM] §2.4.6.2)
-- lockGain() and unlockgain() have no parameter
-- PIM Exceptions: NoOngoingProcessingException

-- TransceiverTime::TimeAccess ([PIM] §2.4.7.1)
-- getCurrentTime()

-- get_current_time_out_type is record
    current_time : time_spec_type;
end record;
-- PIM Exceptions: none

-- getLastStartTime()

-- get_last_start_time_out_type is record
    last_start_time : time_spec_type;
    last_burst_number : burst_number_type;
end record;
-- PIM Exceptions: none

-- Strobing::ApplicationStrobe ([PIM] §2.4.8.1)
-- triggerStrobe() has no parameter
-- PIM Exceptions: none

end package pkg_xcvr_primitives_parameters;
5 References

5.1 Referenced documents

  https://sds.wirelessinnovation.org/specifications-and-recommendations
  https://winnf.memberclicks.net/assets/work_products/Specifications/WINNF-TS-0008-V2.1.1.pdf

  https://sds.wirelessinnovation.org/specifications-and-recommendations

  https://sds.wirelessinnovation.org/specifications-and-recommendations
  https://winnf.memberclicks.net/assets/work_products/Reports/WINNF-TR-2008-V1.0.1.pdf

  URL: https://en.wikipedia.org/wiki/Register-transfer_level

  URL: http://ieeexplore.ieee.org/document/1003477/

The URLs above were successfully accessed at release date.
END OF THE DOCUMENT