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Editors:

David K. Murotake, Ph.D.
Chair, R&D Working Group
dmurotak@scatechnica.com

Lee Pucker
Co-Chair, R&D Working Group
Lee_Pucker@spectrumsignal.com

Earl W. McCune Jr., Ph.D.
Chair, RF Enablers Study Group
Earl.McCune@tropian.com

Jeffrey H. Reed, Ph.D.
Chair, Smart Antennas and Adaptive Processing Study Group
reedjh@vt.edu

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1 Purpose of this Document

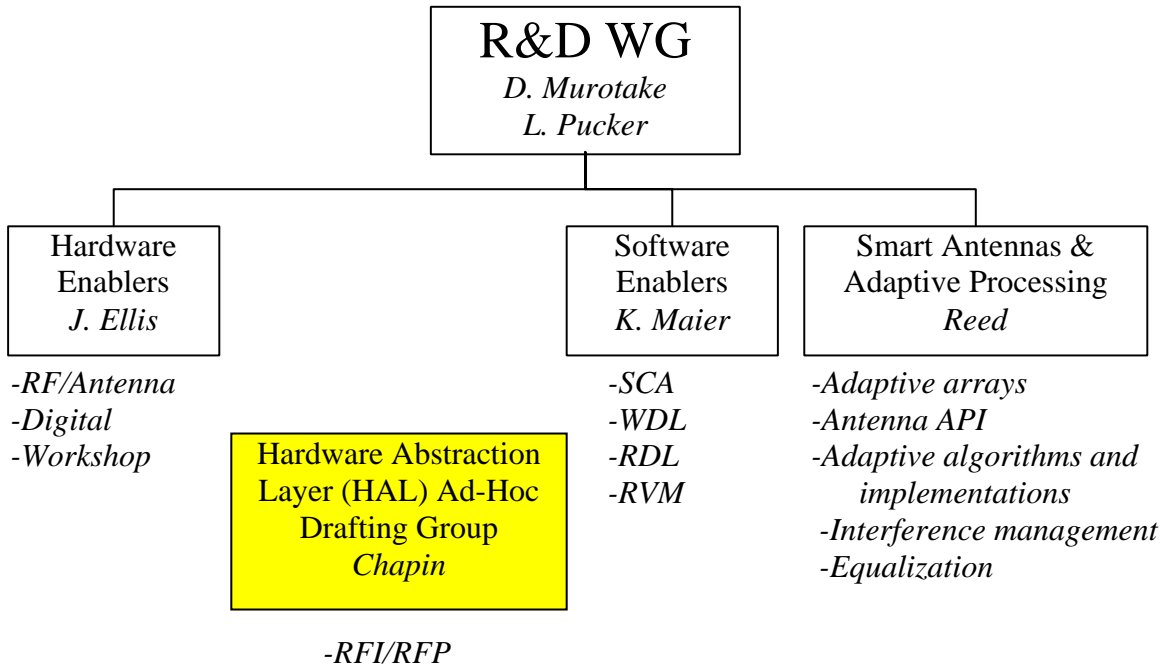
The R&D WG will survey the state-of-the-art in new technology (technology enablers for software defined radio (SDR). These enabling technologies include:

- Hardware technology including RF enablers and digital enablers.
- Software technology (software radio definition languages (RDL) and tools; radio virtual machines (RVM); and new software communications architecture (SCA).
- Systems technology (smart antennas and adaptive processing, scalable systems, advanced terminal management and security technology, and test bed architectures.

This document provides:

- An introduction to the charter and organization of the R&D Working Group.
- Overview of enabling technologies.
- Expert lists and bibliographies for each enabling technology.

2 Introduction to the R&D Working Group



(Above) R&D Working Group organization including HAL Ad-hoc Drafting Group. Source: SDR Forum

Following recommendation by the 2001 Roadmap Task Group, the Research and Development Working Group was established in February 2002 at the 27th General Meeting. The WG is chaired by David Murotake (CEO, SCA Technica, Inc.) and co-chaired by Lee Pucker (CTO, Spectrum Signal Processing, Inc.). The working group is organized into three permanent study groups (Hardware Enablers, Software Enablers, Smart Antennas and Adaptive Processing), and a cross-disciplinary ad-hoc drafting group for a SDRF Recommendation on Hardware Abstraction Layer (HAL-DG). At the

November 2002 General Meeting, it is planned to elevate the HAL-DG to a Technical Committee level drafting group.

2.1 Working Group Charter

- Conduct research into technical activities and publications throughout the world as related to Software Defined Radio. This is to identify technologies which can either fulfil the needs of the marketplace, or enable new products, services, and applications.
- Develop briefings, working papers, bibliographies and expert lists for use by the Forum membership on the conducted research.
- Exchange guest speakers, as necessary, with other organizations as a means of reinforcing and proliferating SDR concepts.
- Facilitate Forum members collaborating on advanced technology demonstrations at select venues including the annual SDRF Technical Conference and Exposition.
- Support development of a web-accessible test bed for use in applied research in software defined radio.
- Conduct requests for participation, requests for information, and draft SDRF recommendations as appropriate.

2.2 2002 Work Plan

The R&D Working Group plans to conduct the following work during 2002. Much of this work will be performed by correspondence using email circulation via the R&D Working Group reflector (researchdevelopment@sdrforum.org), and through bi-weekly teleconferences.

- 1) The R&D WG will solicit additional members by means of a broadly issued Call for Participation in one or more venues to include the IEEE Spectrum.
- 2) The R&D WG will survey the state-of-the-art in:
 - Hardware technology (RF enablers, digital enablers)
 - Software technology (SDR definition tools, Radio virtual machines)
 - Systems technology (smart antennas and adaptive processing, scalable systems, advanced terminal management and security technology, and test bed architecture).

As part of the survey, a list of experts and a bibliography will be developed. In future versions of the report, the lists and bibliography will be updated, and the bibliography annotated for further convenience of our members. Additional nominations for addition to the bibliography and experts list are welcome, and should be submitted to Dave\Murotake (dmurotak@scatechnica.com).

- 3) HAL Ad-Hoc Drafting Group –As part of its mission to promote the development and use of software radio technology, the SDR Forum intends to create a set of standards that improve the portability of waveform software. A key area for standardization is the hardware abstraction layer (HAL). The HAL enables software to exploit the diverse signal processing hardware of SDR platforms in a portable fashion. The HAL drafting group (HAL-DG) has been formed to identify candidate HAL technologies and drive the standardization process. A Request For Information (RFI) is planned in early 2003, a Request For Proposals (RFP) in the middle of 2003, and a standard or standards will be recommended to the SDRF in early 2004. John Chapin (CTO, Vanu Inc.) has been voted Chair of the ad-hoc group. Voted co-chairs are Jonathan Ellis (CEO, PredaComm Inc.) and Alden Fuchs (Senior Systems Engineer, Mercury Computer Systems, Inc.)

The HAL-DG will draft a standard or standards potentially covering the following areas.

1. Technologies that reduce the porting cost of enabling signal processing subsystem software to execute on diverse processing hardware.
2. Technologies that improve the efficiency with which portable signal processing subsystem software executes on diverse processing hardware.
3. Technologies that reduce the porting cost of enabling application software to interact with diverse signal processing subsystems.

Technologies of particular interest include, but are not limited to, languages, APIs, compilers, development environments, automatic code generation, and virtual machines.

The responsibility for Area 3 is shared with the System Interface Working Group of the SDRF. In their documents, this technology area is called the “Modem API.”

The HAL-DG will first issue a Request for Information (RFI), which should receive broad dissemination. The draft RFI will be developed and reviewed by correspondence, prepared as input submissions, reviewed/commented by the Technical Committee at a future General Meeting, and posted as input documents for review by the SDRF membership for purposes of coordination and integration of review comments.

Responses to the RFI will be reported to the Technical Committee. After inputs from the RFI have been received, one or more Requests for Comment (RFC) will be drafted by the ad hoc drafting group, and reviewed by an Architecture Review Board to be established by the SDRF Technical Committee. Upon approval by the Architecture Review Board, the RFP will be reviewed/commented by the Technical Committee at a future General Meeting, and posted as input documents for review by the SDRF membership for purposes of coordination and integration of review comments.

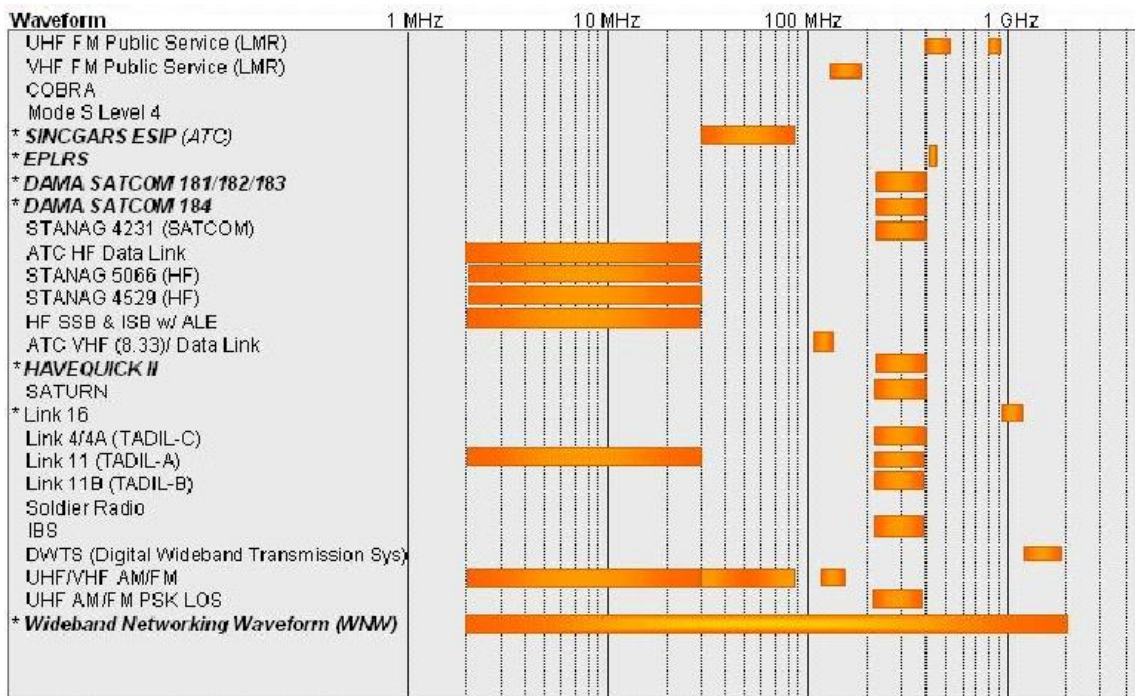
- 4) During the 2003 work period, the R&D Working Group plans to analyze the potential impacts of the new technologies to SDR hardware, software, and systems, and draft

one or more SDRF Recommendations on radio virtual machines, SDR definition languages, adaptive systems, and other areas as appropriate.

- 5) The R&D WG members will support the planning and review of the November SDRF Technical Conference by coordinating with conference planners, encouraging our peers in the submission of papers, assisting in the peer review of submitted papers, and assisting in chairing of sessions as needed.
- 6) The R&D WG will develop and maintain an internal website which includes informal discussion boards and posting area for working papers, for the purposes of informal peer review and comment. The website is initially hosted by Virginia Tech.

3 Hardware Enablers

3.1 Radio Frequency (RF) Enablers



* - indicates Cluster 1 Core Waveforms *ITALICS* - indicates JTRS ORD Key Performance Waveforms
 (Above) Unlike consumer and commercial SDR, government SDR applications may require radios and antenna systems that tune over three or more decades (2 MHz – 2 GHz). (Source: US Government)

In many applications (such as software reconfigurable, multi-mode home networking devices or single-band (e.g. 1900 MHz) mobile terminals), operation within a limited range of frequencies are acceptable, and conventional RF chipsets and antennas may be employed with SDR sets. By contrast, other applications require multi-band operation over multiple decades. By example, the family of Joint Tactical Radio Systems (JTRS) radio networks and terminals are required to operate over 2 MHz – 2 GHz, with future frequency extensions down to 1.6 MHz and up to 6 GHz and beyond. An internationally multi-band, multi-mode 2G/3G mobile terminal may be required to operate between in

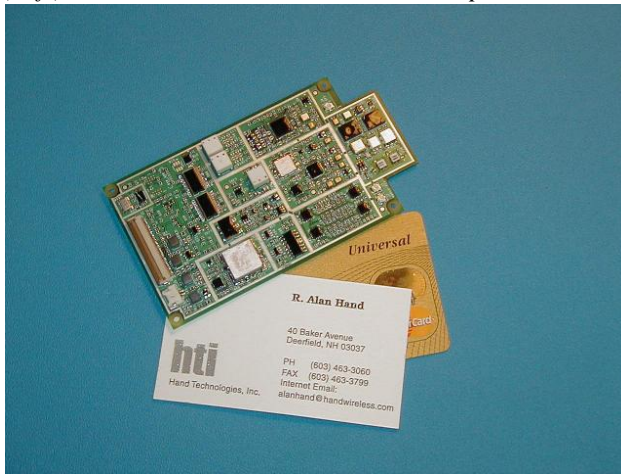
several bands including 800 MHz, 900 MHz, 1900 MHz, 2.3 GHz, etc. For these multi-band, multi-mode (MB/MM) government and commercial SDR applications, novel RF chipsets, power amplifiers and antennas are required.

During the next few years, another enabling technology which is critical to the MB/MM SDR is the RF micro-electrical machine (RF MEMS). These tiny devices will permit practical multi-decade antennas and small, low-power RF receivers and synthesizers.

Another enabling technology, key to commercial infrastructure and special government radio applications, is cryogenically cooled multi-band RF receivers and transmitters.

3.1.1 Multi-band/multi-mode RF chipsets

(Left) Advancements in miniaturized RF chipsets enable design of mobile terminals capable of meeting government and commercial SDR requirements, supporting multiple cellular and PCS modes. (Source: HTI, Inc.)



Highly miniaturized MB/MM RF chipsets have been developed, and are expected to enter production in 2003. Further technological advances are expected as RF MEMS technology is incorporated, leading to order-of-magnitude reductions in size, weight, power consumptions and cost of MB/MM chipsets. Research is ongoing on novel methods of RF signal

processing which may further result in order-of-magnitude improvements in size, weight and power. Finally, superconducting RF technology helps achieve required performance for both commercial infrastructure and government MB/MM front ends. These technologies are entering the SDR mainstream today and should be common by 2005.

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Experts List

Transceivers/Modulation/Low Level RF

Asad Abidi, UCLA. <http://www.icsl.ucla.edu/aagroup/>. abidi@icsl.ucla.edu
 Mark Cummings, enVia. markcummings@envia.com. +1 (408) 777-4802
 Alan Hand, HTI, alanhand@handwireless.com, +1 (603) 463-3060
 Tom Lee, Stanford. tomlee@smirc.stanford.edu. +1 (650) 725-3709
 Nathan Silberman, RFCo. nsilberman@rfco.net . +1 (408) 351-4235

Linear Power Amplifiers

John Sevic, Cal-Eastern Labs John.Sevic@cel.com

Superconducting RF Systems

Jack Rosa, Hypres. jrosa@hypres.com. +1 (914) 592-1190 x7888

3.1.2 Wideband and ultra-wideband (UWB) antenna elements

Left: A simple 800 MHz – 1.9 GHz meander line antenna (MLA) prototype is shown. MLA technology can support efficient single antenna elements which can be tuned over several decades while maintaining a high Q factor. (Source: SkyCross)

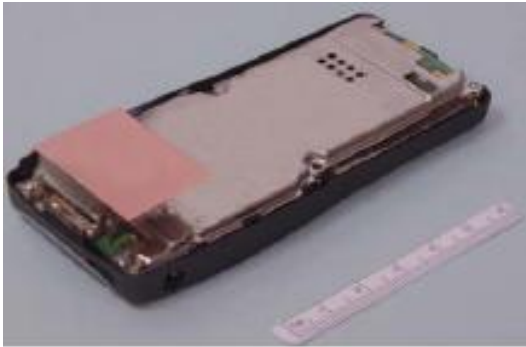


Photo taken in a test configuration

Novel antenna element technologies have emerged which enable design and production of wideband (WB) and ultra-wideband (UWB) antennas for SDR. Examples include ultra-wideband "resistive" antennas, as well as the "meander line" antennas (MLA). In those designs in which switches are employed, replacement of pin diodes, fat FETs, vacuum tube relays (VTR) and other bulky, costly switch devices with micro electro-mechanical systems (MEMS) will further enable order of

magnitude size and cost reductions of WB and UWB antennas. Additionally, advances in modeling and simulation methods enable accurate simulation of these new antenna element types.

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www.timedomain.com/Files/PDF/news/AntennaSchantz.pdf

Experts List.

- Roland Gilbert, BAE Systems. roland.a.gilbert@baesystems.com. +1 (603) 885-5861.
 Sergey Makarov, Center for Wireless Information Studies, Worcester Polytechnic University. makarov@wpi.edu . +1 (508) 831-5017
 Mike Thursby, SkyCross. thursbym@skycross.com . +1 (321) 308-6617

3.1.3 RF MEMS

These highly miniaturized devices can be used as miniature switches (replacing costly, bulky pin diodes, super-wide field-effect transistors (FET) and vacuum tube relays (VTR) in antennas. They can also be used as high-performance miniature inductors, capacitors, filters, T/R switches and diplexers in RF front ends. Use of RF MEMS can reduce the size, weight and power consumption of RF systems by an order of magnitude. First production deployment of RF MEMS is expected in cell phones by 2003, and should be mainstream by 2005.

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Experts.

J.T. Aberle, Etenna Corporation. <http://www.etenna.com/>. +1 (240) 456-4100.

F. Musalem, MEMSCAP. <http://www.memscap.com/index.html>. +1 (877) MEMSCAP

William H. Weedon, Applied Radar. whw@appliedradar.com. +1 (401) 295-0062

Professor R.B. Yates (R.Yates@mems.org.uk)

3.2 Digital Enablers

3.2.1 Processing Devices

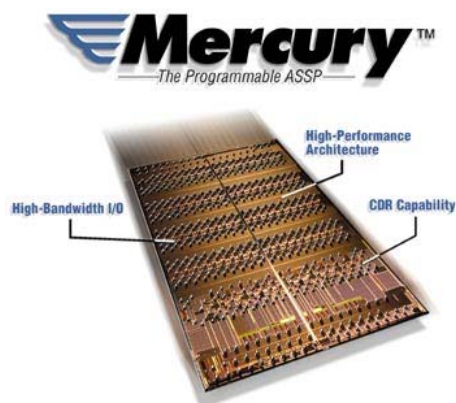
3.2.1.1 Field Programmable Gate Arrays

Above: The “Virtex II Pro” XC2VP7 device comes in numerous die sizes including the 23x23x1 mm FG456 flat pack. This miniscule package contains eight embedded serial transceivers, one PPC 405 32-bit RISC CPU and approximately 700K reconfigurable gates. This small package fits well in PC card packages, and contains 248 user available I/O pins. (Figure: Xilinx)

Pkg	Pitch (mm)	Size (mm)				Rocket I/O Transceiver Blocks	PowerPC Processor Blocks	Logic Cells ⁽¹⁾	CLB (1 = 4 slices = max 128 bits)	
			XC2VP2	XC2VP4	XC2VP7				Slices	Max Distr RAM (Kb)
FG256	1.00	17 x 17	140	140						
FG456	1.00	23 x 23	156	248	248					
FF672	1.00	27 x 27	204	348	396					
FF896	1.00	31 x 31			396					

Device	Rocket I/O Transceiver Blocks	PowerPC Processor Blocks	Logic Cells ⁽¹⁾	Slices	Max Distr RAM (Kb)
XC2VP2	4	0	3,168	1,408	44
XC2VP4	4	1	6,768	3,008	94
XC2VP7	8	1	11,088	4,928	154

(Left) The “Mercury” programmable logic device offers high density, reconfigurable system-on-chip functionality and competes with the Virtex II architecture. (Figure: Altera).



Several advanced FPGA families provide “system-on-chip” capabilities. The Xilinx Virtex II Pro and Altera Mercury are current examples of this class. The tables above show representative data for a one inch square Xilinx XC2P7 “platform” FPGA which contains about 700,000 logic gates in addition to 8 LVDS transceiver blocks and one PowerPC 405 core. A number of optimized IP cores have been developed for wireless processing. Xilinx and Altera have both worked closely with The Mathworks to offer co-design libraries specifically targeted at optimized core implementations in

combination with SimuLink. Specialized reconfigurable devices for SDR have been under development by Quicksilver and others. The R&D Working Group is sponsoring a Reconfigurable Devices Workshop in early 2003. The Workshop is being organized by Jonathan Ellis (CEO, Predacomm).

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Experts:

- Chris Dick, Xilinx. chris.dick@xilinx.com. +1 (408) 558-2709.
- Jonathan Ellis, Predacomm. jonathan_ellis@predacomm.com. +1 (512) 587-6001.
- Ben Esposito, Altera. bene@altera.com. +1 (407) 681-9300.
- John Watson, QuickSilver. john.watson@qstech.com. +1 (408) 574-3300.

3.2.1.2 General Purpose Processing

The "big news" during 2002 was undoubtedly the announcement by Intel CTO Pat Gelsinger at Intel Developer Forum (IDF, 2/28/02, San Francisco) that Intel was initiating a large-scale R&D initiative called "Radio Free Intel", the company's new, ambitious R&D efforts into the radio-frequency (RF), software-defined radio, and related wireless sectors. The initiative will incorporate SDR support into "every Intel CPU" as a baseline product by the end of the decade. Gelsinger said Intel Labs demonstrated a "complete radio technology" on a single chip at 10-GHz--based on traditional silicon. "We are talking about silicon, not silicon-germanium or gallium-arsenide," he said.

Progress has been made on other fronts, notably GPP cores by MIPS, ARM, and PowerPC become increasingly available in mainstream FPGAs, and currently dominate the embedded GPP marketplace (including SDR).

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3.2.2 Communications Fabrics

Switched fabrics employing crossbar ASICs, such as RACEway and SkyChannel, are an excellent means of overcoming the I/O bottlenecks suffered by "normal" I/O busses such as PCI. The latest generation of switched fabrics such as Infiniband and RapidIO employ gigabit serial physical layers, offering excellent I/O performance and network topologies while dramatically reducing the size, cost, power consumption, and (most importantly) the number of wires and pins necessary to implement the fabrics. Crossbar switched fabrics can now be implemented inside large FPGAs, overcoming I/O bottlenecks in high-speed wireless processing. Crossbar switch, I/O transceiver cores and "smart"

endpoint cores are available, and the latest “platform” FPGA’s such as the “Virtex II/Pro” and “Mercury” also provide embedded I/O transceivers.

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Experts List:

Craig Lund, Mercury Computer Systems Inc. clund@mc.com . +1 (978) 256-0052
 Eitan Medina, Galileo. eitan@galileo.co.il. +972-8-924-7555 Ext 317.
 David Murotake, SCA Technica. dmurotak@scatechnica.com. +1 (603) 321-6536.

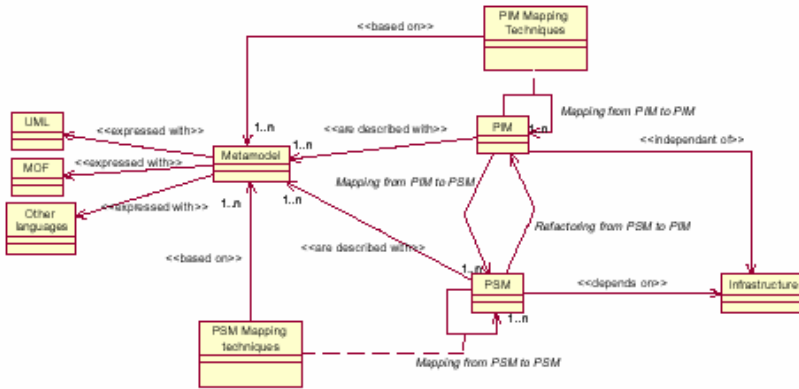
4 Software Enablers

4.1 Software Communications Architecture (SCA)

A new version of the SCA is under development by the Object Management Group (OMG) Software Radio Domain Special Interest Group (SR-DSIG) (<http://swradio.omg.org/>). This new SCA is being developed using the OMG Model Driven Architecture (MDA). The new Platform Independent Model (PIM) uses the JTRS SCA 2.2 as a Platform Specific Model (PSM) starting point, and extends the current SCA behavioral models. The new PIM, and the Minimum version which will follow, will probably be mapped to J2ME and other platforms. The activity is being led by the OMG SR-DSIG Co-Chairs, Jerry Bickle (Raytheon), Jeff Smith (Mercury Computer Systems) and Mike McClemens (Mitre).

One of the major benefits of a platform independent model (PIM) standard is the ability to port the PIM to different platform specific models (PSM) using CE, .NET, CORBA, or Java. A second major benefit is the ability to certify compliance of various PSM’s. Since the PIM maps to PSM’s using basic OMG technologies such as the UML and XML, and since these technologies are capable of formal methods of proof, *it is possible to formally prove compliance of a PSM/PIM pair as long as the mappings themselves are done with formal methods in mind.*

Left: Platform independent models (PIM) are mapped to platform specific models (PSM) using core OMG



technologies such as UML and XML. The SCA PIM is likely to be mapped to Java platforms for consumer and commercial SDR applications. (Figure: OMG)

A SCA Reference Implementation (SCARI) has also been developed by the Canadian

Communications Research Center (CRC) under contract to the SDR Forum and the Canadian defense establishment. The project is led by Steve Bernier. The CRC SCA Reference Implementation uses Java and complies with the Joint Tactical Radio System (JTRS) SCA 2.2.

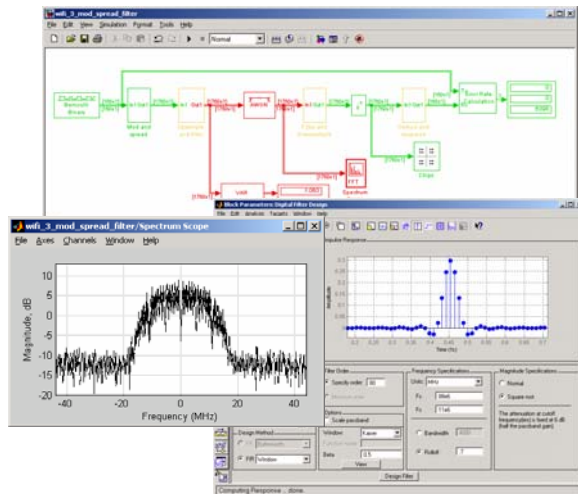
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Experts List:

- Steve Bernier, CRC. +1 613-991-6343. steve.bernier@crc.ca
- Jerry Bickle, Raytheon. Gerald_L_Bickle@Raytheon.com
- Mike McClimens, Mitre. mikemc@mitre.org
- Jeff Smith, Mercury Computer Systems Inc. jessmith@mc.com

4.2 Waveform Development Environment (WDE)



Left: SIMULINK is used to model wireless systems such as IEEE 802.11 WLAN and Bluetooth. Different radio designs, waveforms, propagation effects and interference management systems can be evaluated with SIMULINK. SIMULINK has optimized target platform implementations for Xilinx and Altera FPGAs as well as TI DSPs. SIMULINK is used as a component of Foresight’s WDE. (Figure: MathWorks)

Impressive milestones have been reached in the SDR tools area, such as waveform development systems. Some of these tool sets employ “mainstream” simulation environments such as MATLAB and SIMULINK. Because of the platform

specific optimization of IP cores and DSP algorithms, under some circumstances SIMULINK generated code on DSPs and FPGAs may perform BETTER than when hand-coded. Related fields include Radio Definition Language (RDL) and Radio Virtual Machines (RVM).

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Experts List:

Anne Mascarin, Mathworks. +1 (508) 647-7598 (annem@mathworks.com).
 Stuart McGarrity, Mathworks. (stuartm@mathworks.com).
 E.D. Willink, Racal, Ed.Willink@rrl.co.uk
 Maurice Schiff, Elanix. maury@elanix.com
 Deborah Wilson, Foresight Systems. +1 (714) 704-1670, wilson@foresight-systems.com

4.3 Radio Description Languages

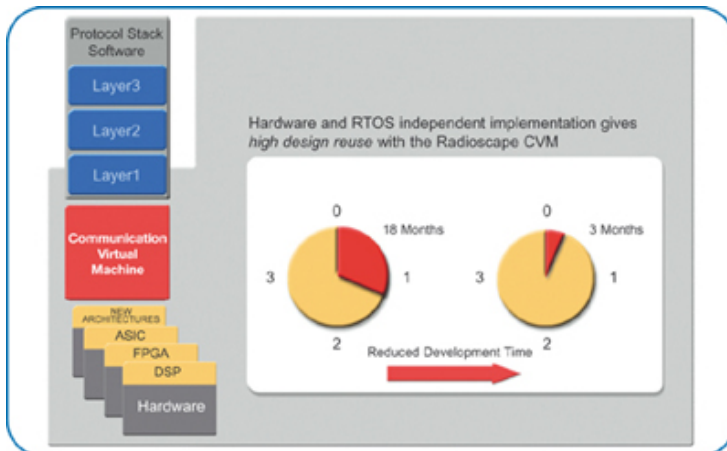
The Radio Definition Language (RDL) is a higher order language originally developed by Vanu used to "construct" a radio functional model using RDL "building blocks". RDL is used to configure a flexible modem, describe the desired signal processing graph, and give parameters for each processing stage. It does NOT include implementations of signal processing stages, nor is it a waveform specification language.

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Experts:

John Chapin, Vanu. 617-864-1711, jchapin@vanu.com. <http://www.vanu.com/>
 Jeff Reed, Virginia Tech. +1 (540) 231-2972. reedjh@vt.edu

4.4 Radio Virtual Machines

Left: The RVM is a hardware abstraction which can significantly accelerate time to market. It brokers parallelism in multi-core, multi-processor, and accelerated designs. It allows the interoperability of multi-vendor, real-time intellectual property at both 'whole-stack' level and 'stack-component' model. Figure source: Radioscape.

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Experts:

Dan Chester, RadioScape. +44 (0)20-7224-1586 (in UK), dan.chester@radioscape.com
 Mike Gudaitis, L-3 Communications, +1 (315) 339-6184 mike.gudaitis@L-3com.com
 Joe Mitola III, DARPA, jmitola@darpa.mil

5 Adaptive Processing and Smart Antennas

For years, wireless infrastructure leaders have planned to deploy SDR technology in base stations concurrently with their deployment of software defined adaptive processing, interference cancellation and smart antennas. This is because the digital signal processing

hardware and algorithms needed to implement adaptive algorithms are complementary to the methods needed to implement SDR receivers, synthesizers and modems. Also, joint implementation of SDR modems with adaptive processing is generally synergistic, offering higher performance at lower cost than individual methods implemented alone.

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5.11 Experts

5.11.1 Industry Leaders

Michael Wengler, Qualcomm Inc., mwengler@qualcomm.com

Brian G. Agee, Protean Radio Networks, bgagee@proteanradio.net

Paul Petrus, ArrayComm, Inc., petrus@arraycomm.com

Marty J. Feuerstein, Metawave Communications, martyf@metawave.com

J. C. Liberti, Telcordia Technologies, liberti@bellcore.com

Mamoru Sawahashi, NTT DoCoMo, Inc., sawahasi@mlab.yrp.nttdocomo.co.jp

5.11.2 Narrow-Band Cellular

G. E. Bottomley, Ericsson, bottoml@rtp.ericsson.se

K. J. Molnar, Ericsson, molnar@rtp.ericsson.se

S. Chennakeshu, Ericsson

J. J. Shynk, University of California, Santa Barbara

5.11.3 General Array Processing

J. M. Mendel, University of Southern California, Los Angeles, mendel@sipi.usc.edu
 Jack H. Winters, Jack Winters Communications LLC. jack@jackwinters.com
 Mati Wax, U.S. Wireless, mati@uswcorp.com
 Harry L. Van Trees, George Mason University, hlv@gmu.edu
 Arogyaswami J. Paulraj, Stanford. +1 (650) 725-8307. apaulraj@stanford.edu
 James Hicks, MPRG, VA Tech, jahicks@vt.edu

5.11.4 Array Processing for CDMA

Seungwon Choi, Hanyang University, choi@dsplab.hanyang.ac.kr
 Hyuck M. Kwon, Wichita State University, hyuck.kwon@wichita.edu
 Ayman F. Naguib, Morphics Technology, Inc., naguib@morphics.com

5.11.5 STC and MIMO

Vahid Tarokh, Harvard Univeristy, vahid@mit.edu
 Nambi Seshadri, Broadcom Corp., nimbi@broadcom.com
 Hamid Jafarkhani, University of California, hamidj@uci.edu
 Ran Gozali, Raphael, rgozali@vt.edu
 S. N. Diggavi, AT&T Shannon Laboratory, suhas@research.att.com
 N. Al-Dhahir, AT&T Shannon Laboratory, naofal@research.att.com

5.11.6 Diversity Reception

Chinthananda Tellambura, Monash University, chintha@dgs.monash.edu.au
 Annamalai Annamalai, MPRG, VA Tech, annamala@vt.edu
 Rodney G. Vaughan, New Zealand Institute for Industrial Research, r.vaughan@irl.cri.nz

5.11.7 Radio Resource Management

R. D. Yates, WINLAB Rutgers University, ryates@winlab.rutgers.edu
 David N. C. Tse, University of California Berkeley, dtse@eecs.berkeley.edu

5.11.8 Propagation

Marcus Bronzel, Technical Univ. of Dresden, bronzel@ifn.et.tu-dresden.de
 Richard Ertle, 3Com, Richard.B.Ertel@L-3Com.com
 Jeffrey H. Reed, MPRG, VA Tech, reedjh@vt.edu

5.11.9 AOA/TOA Estimation

Martin Haardt, Ilmenau University of Technology, Martin.Haardt@tu-ilmenau.de
 A. Lee Swindlehurst, Brigham Young University, swindle@ee.byu.edu
 Ryuji Kohno, Yokohama National University, kohno@kohnolab.dnj.ynu.ac.jp