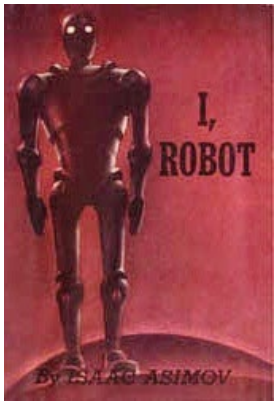
Exciting Next Generation Software Radios

Tom Rondeau
DARPA/MTO

Wireless Innovation Forum, 2018
Melbourne, FL

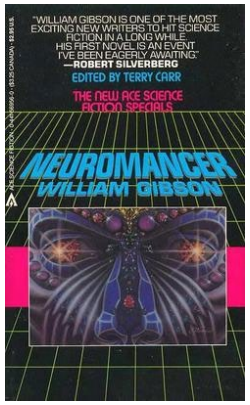
11/15/2018

Science fiction and the electromagnetic spectrum



https://en.wikipedia.org/wiki/I,_Robot

http://www.imdb.com/title/tt0079945/



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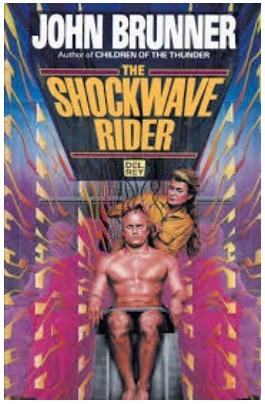

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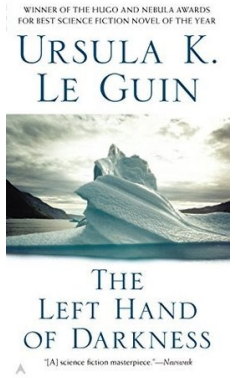

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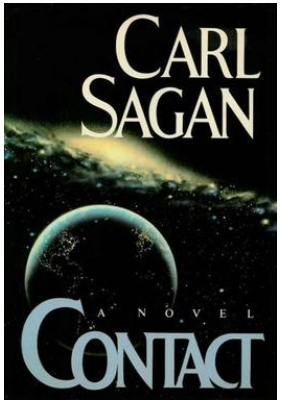


https://upload.wikimedia.org/wikipedia/en/5/55/Contact_Sagan.jpg

It’s a great time to love science fiction – and radio

https://upload.wikimedia.org/wikipedia/en/d/d4/Rogue_One%2C_A_Star_Wars_Story_poster.png

https://motherboard-images.vice.com/content-images/contentimage/no-id/1482962292713131.png

Defeating the Empire relied on an antenna alignment!

Plot points are even revolving around electronic warfare

http://nerdist.com/wp-content/uploads/2016/05/startrekbeyondposter-4.jpg

https://www.youtube.com/watch?v=AmWLaFQNwVE

57.7 MHz!
"Very high frequency!"

Another look at the law of Star Trek films

imdb.com

Star Trek I
The Motion Picture

imdb.com

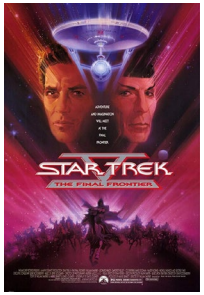
Star Trek II
The Wrath of Khan

imdb.com

Star Trek III
The Search for Spock

imdb.com

Star Trek IV
The Voyage Home



imdb.com

Star Trek V
The Final Frontier

imdb.com

Star Trek VI
The Undiscovered Country

Cellular Technologies

1G (1979)
Proved the commercial viability

2G (1991)
Voice and SMS – indicated need for data

3G (1998)
Proved market for data

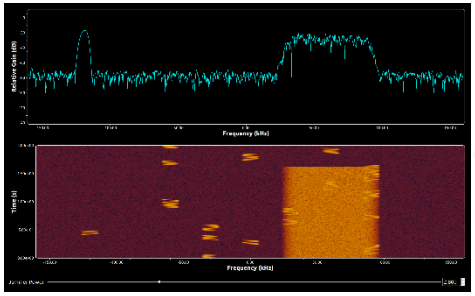
4G (2008)
Data done right – how to get data everywhere?

5G (2019)
High BW, low latency – New (IoT) markets?

6G (2028?)
Solving the problems of 5G?

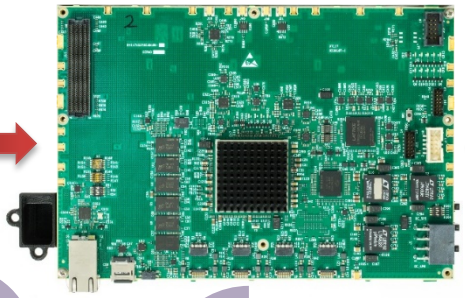
What do we need for RF convergence?

Spectrum



Access to unprecedented amount of spectrum and instantaneous bandwidth

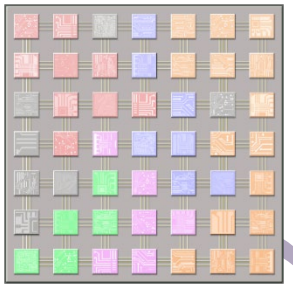
Receiver/Exciter



Flexible, reconfigurable hardware enabling multiple missions from same hardware

- Comms
- Radar
- EW
- SIGINT

Processor



More bandwidth needs more processing and/or smarter math

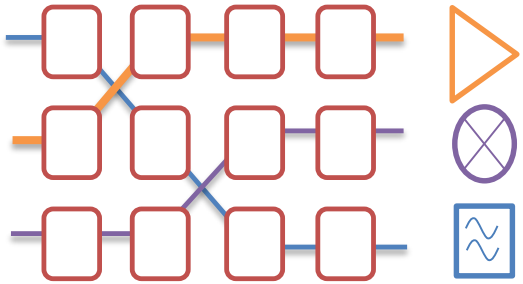
Apps, Development

C/C++
TensorFlow
GNU Radio
Python
Etc.

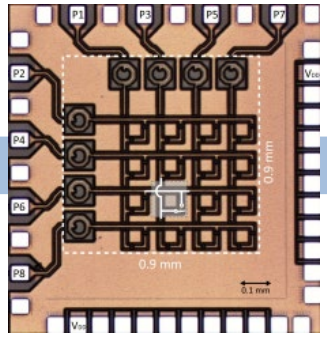
Development tools to quickly produce new applications and approaches to spectrum use

The DARPA RF-FPGA program

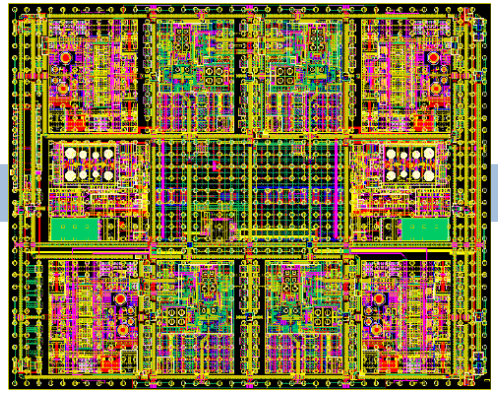
Can we create an FPGA-like fabric of switches and programmable RF components?



Concept

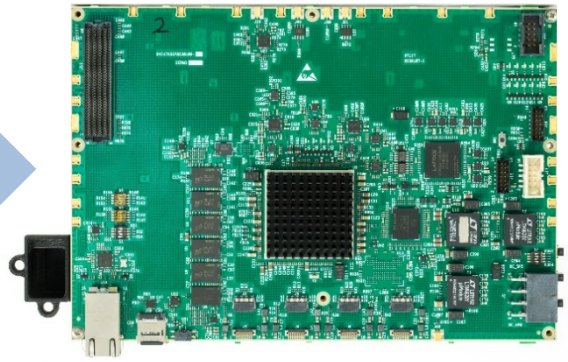


Proof of Concept



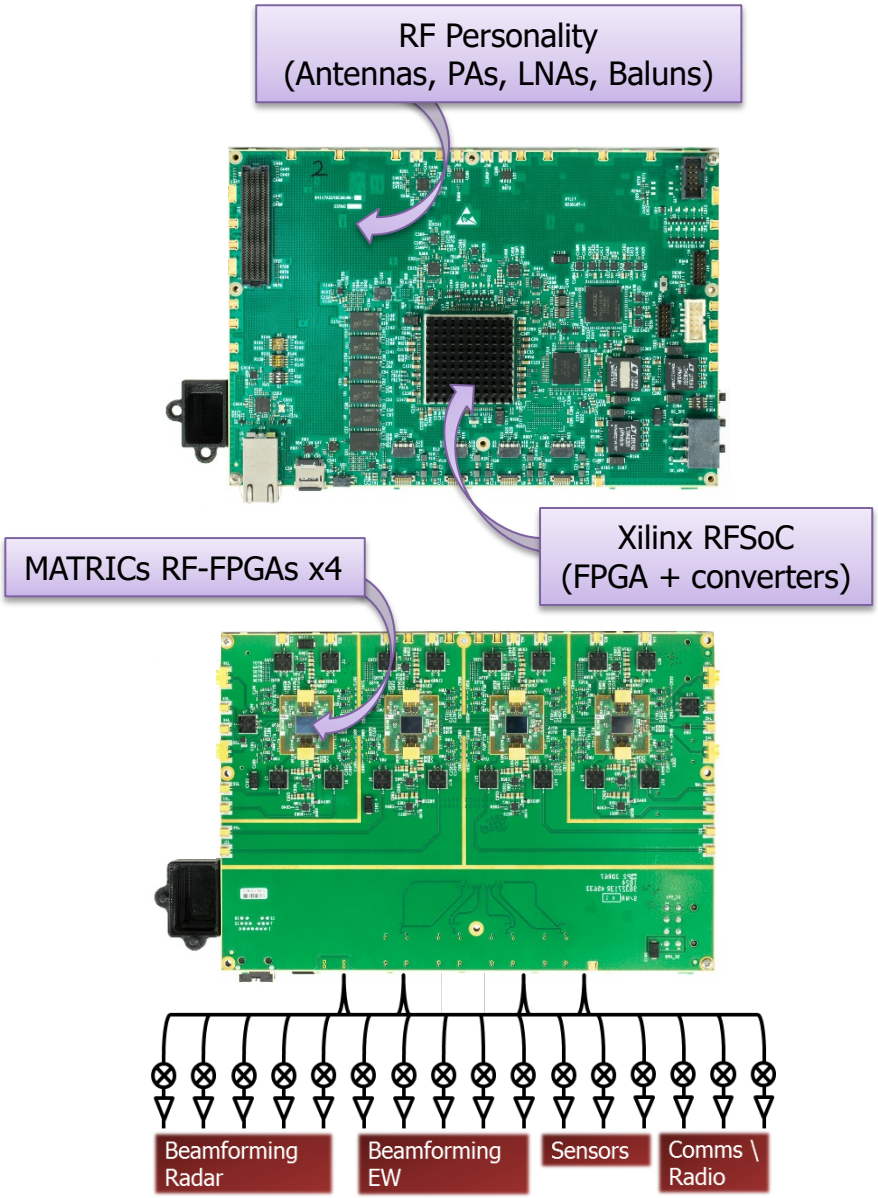
Prototype

Demonstration



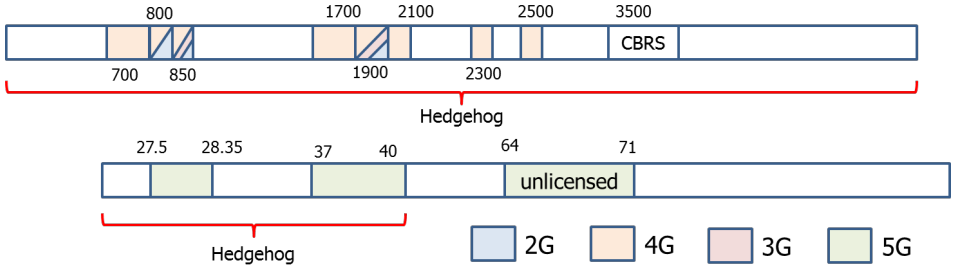
Integrated System

Hedgehog: multifunction, multichannel RF Convergence device

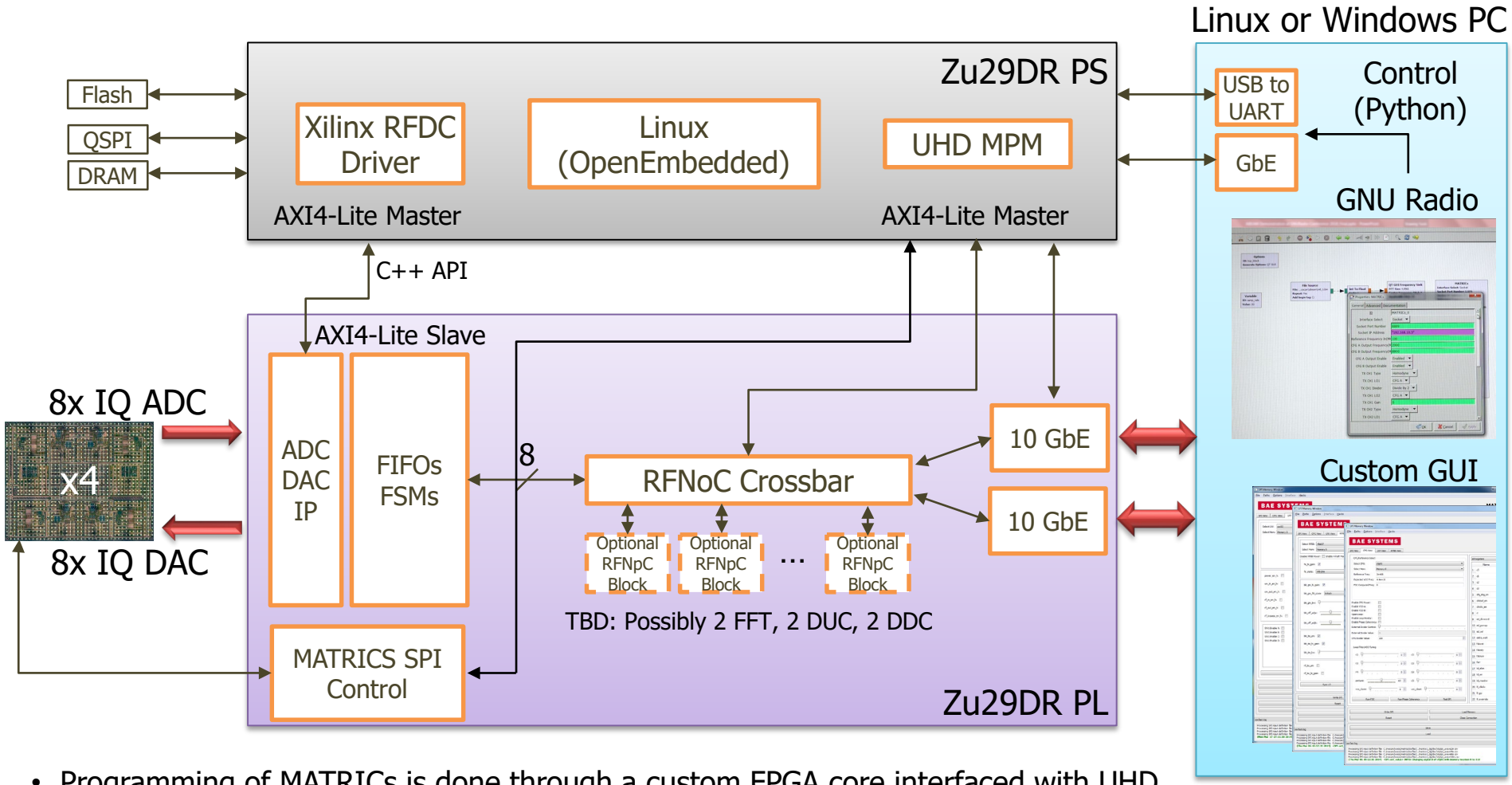


Parameter	Specification
Freq. Range	DC – 40 GHz
IBW	10 MHz - 2 GHz
Channels	8 Tx, 8 Rx
Integrated processing	GPP and FPGA Over 280 Gbps I/O
Converters	16 x 14 bit DACs 16 x 12 bit ADCs Integrated with processor

Covering all the G's



Programming on Hedgehog

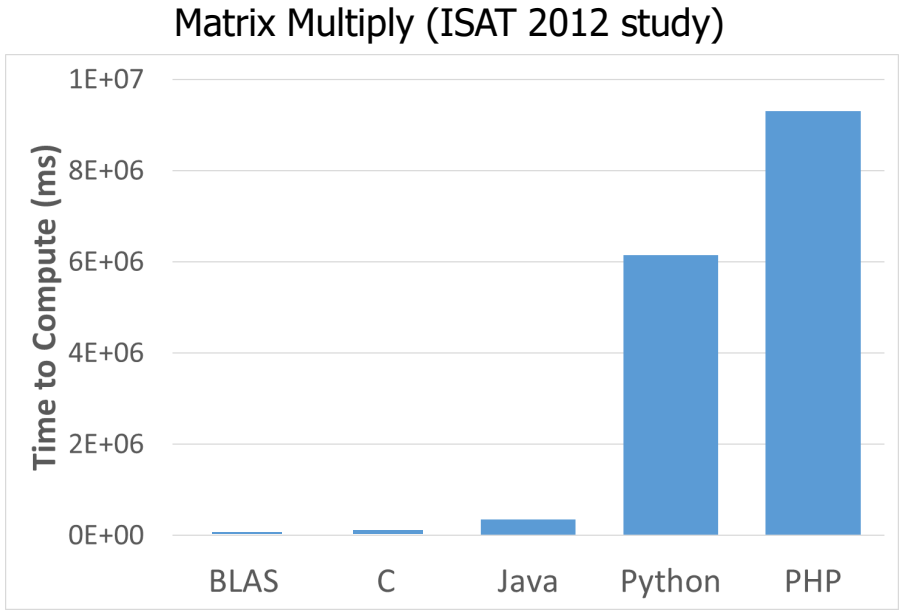


- Programming of MATRICs is done through a custom FPGA core interfaced with UHD
- Programming of the ADCs/DACs is done through a Xilinx Driver with a C/C++ API
- Tools will be available under the open-source GNU General Public License version 3 (GPLv3)
  - Gov't users may have early access to alpha/beta versions

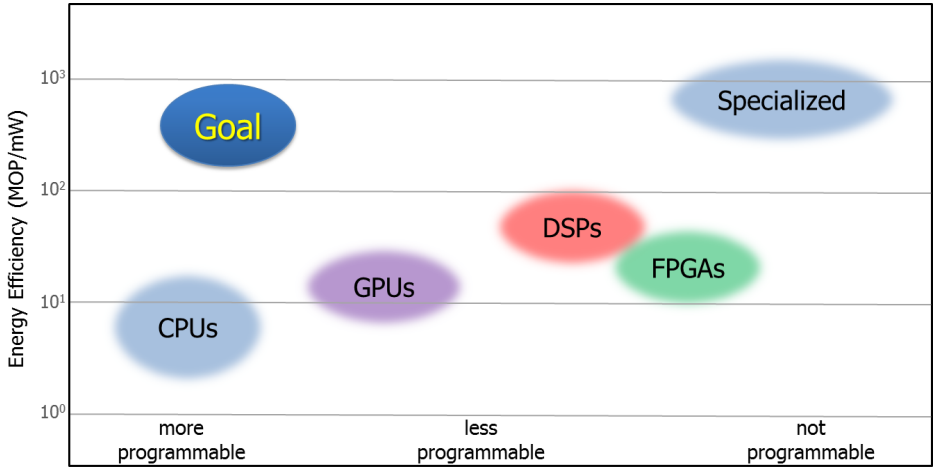
Dynamic responses and speed to new solutions need good programming models and efficient processors

Programmability

- Productivity has come at the cost of compute efficiency
- Abstraction tends to ignore the underlying hardware



ISAT 2012 study

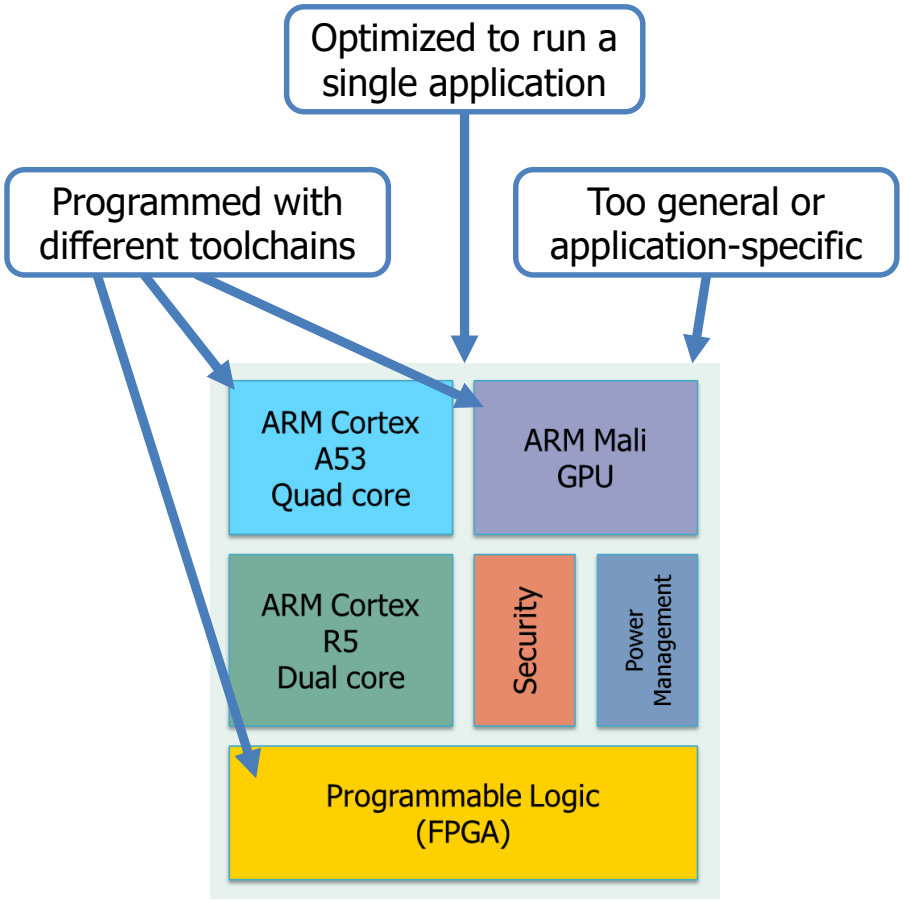


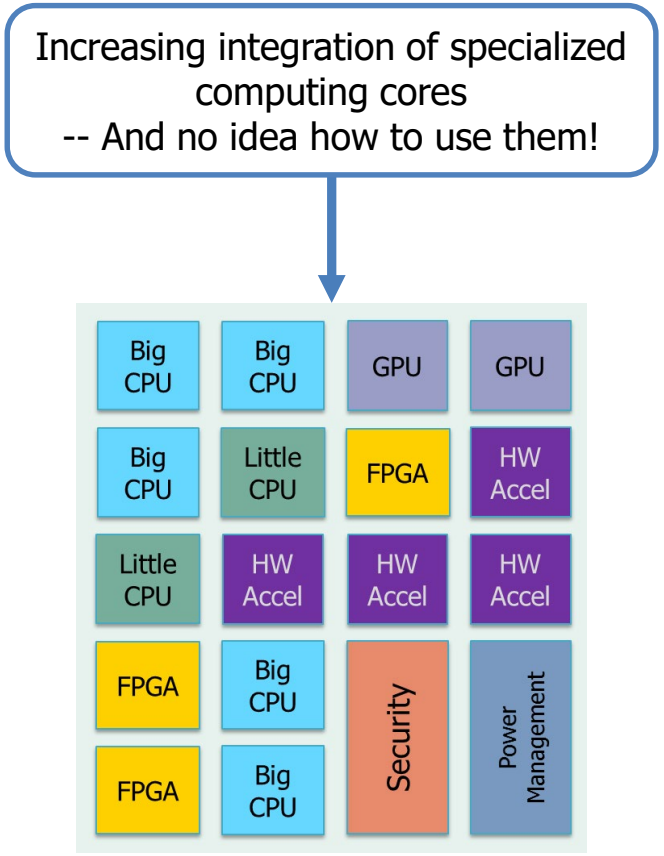
ISAT 2012 study

Specialization

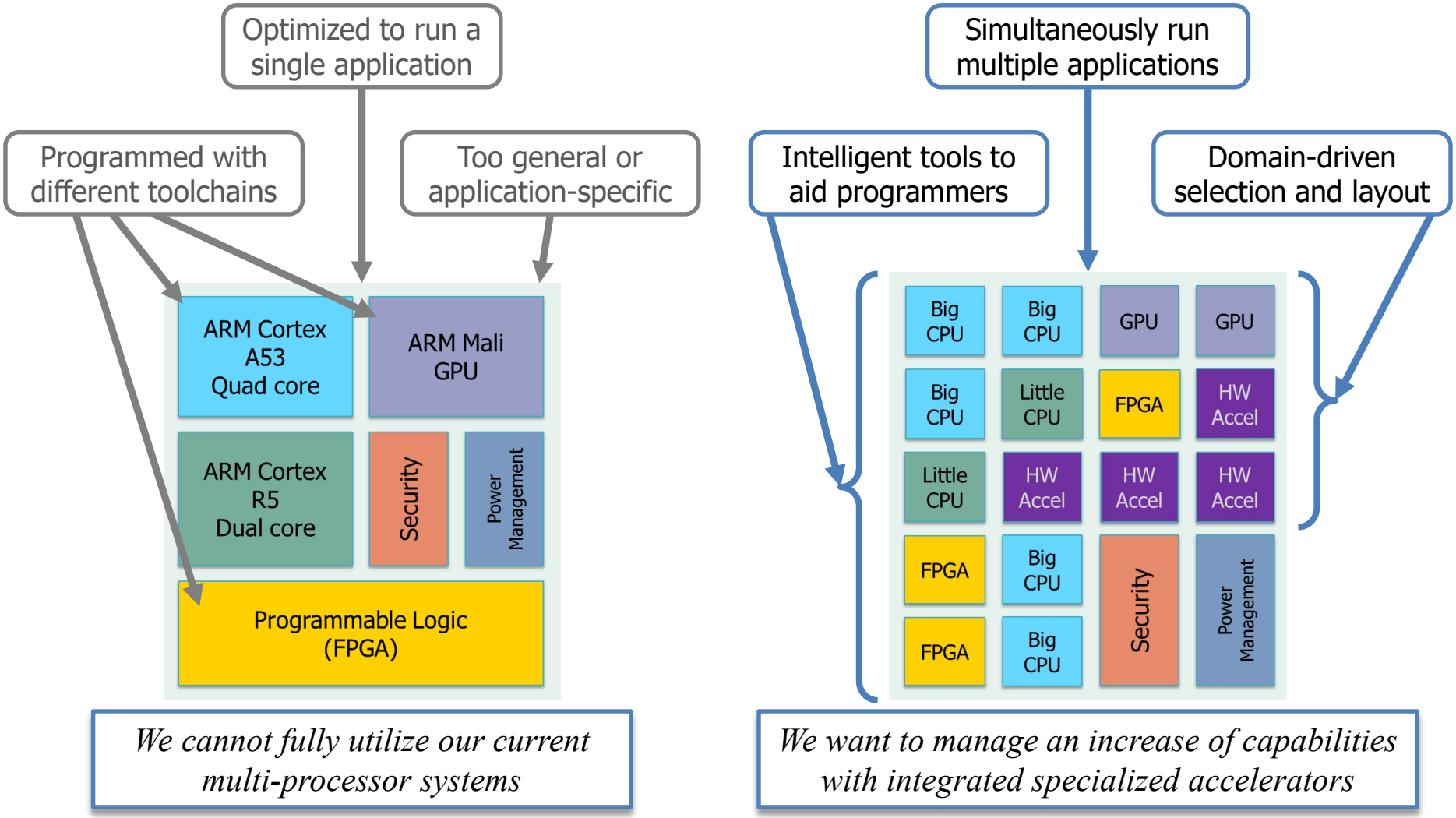
- Performance has come at the cost of usability
- Difficulty in programming and system integration

There is a trend to integrate more capabilities into a System-on-Chip

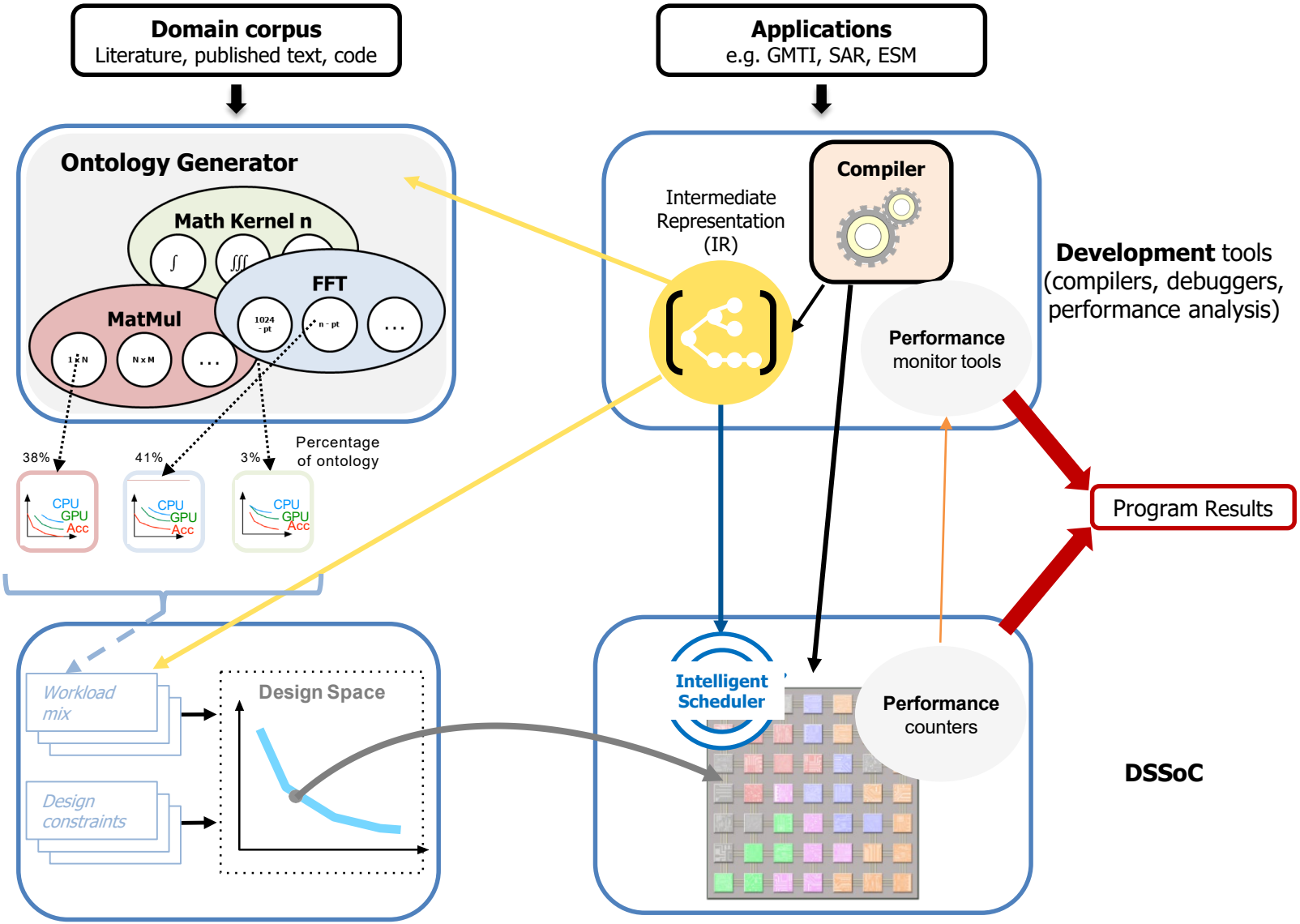




Domain-Specific System on Chip (DSSoC) looks to change this



DSSoC: Domain-driven design



Domain ontology **discovery**

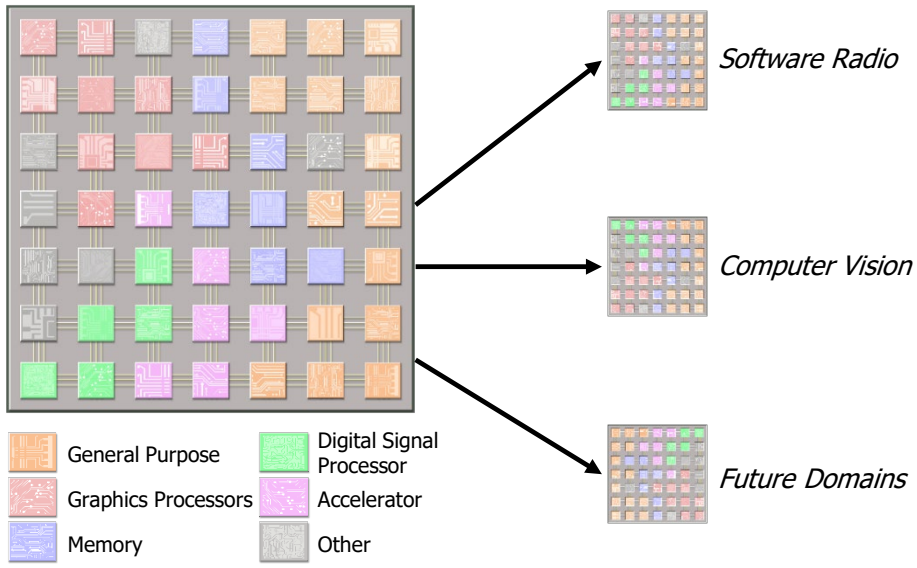
Development tools (compilers, debuggers, performance analysis)

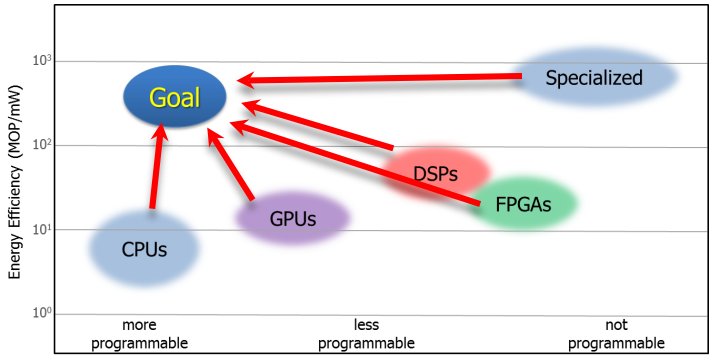
Design: Processor Element selection and affinity analysis

DSSoC

DSSoC is as much or more a software program as a hardware program

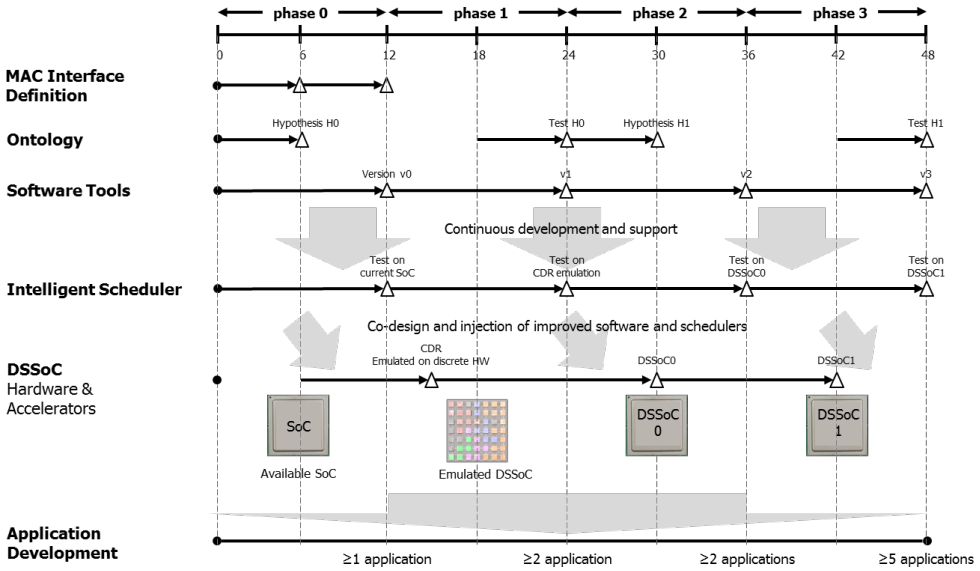
- Create a development ecosystem that takes advantage of the specialized hardware with no added burden to the programmer
- Design an intelligent scheduler for efficient data movement between DSSoC processor elements
- Build a DSSoC of advanced, heterogeneous processors and accelerators for domains like software radio and computer vision





DSSoC will enable rapid development of multi-application, heterogeneous systems through a single programmable device

DSSoC program and performer overview



DSSoC Performers

Arizona State University

IBM

Oak Ridge National Laboratory

Stanford University

	Phase 1	Phase 2	Phase 3
Chip & Scheduler			
Number of simultaneous apps	≥2	≥2	≥5
Integration time for new accelerators[1]		≤3 months	≤3 months
Power savings relative to previous phase		≤80%[2]	≤80%[3]
Utilization of PEs[4]	≥80%		≥90%
Max. time per scheduler decision	≤500 ns	≤50 ns	≤5 ns
Medium Access Control (MAC)			
Latency (PE to PE)	≤500 ns	≤50 ns	≤5 ns
Throughput (PE to PE)	≥25 Gbps	≥50 Gbps	≥100 Gbps
Power	≤50% of chip	≤40% of chip	≤20% of chip

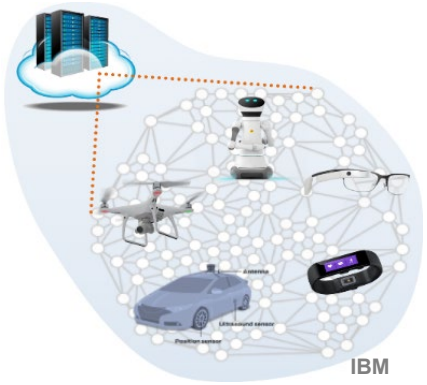
Power Constraints	
Embedded System (cell phone)	≤ 5 W
Portable System (laptop)	≤ 25 W

1. Three months to integrate new accelerators into DSSoC; enforced by program timeline
2. Compare the intelligent scheduler on DSSoC0 to the intelligent scheduler controlling the commercial SoC from phase 0.
3. Compare the intelligent scheduler on DSSoC1 to the intelligent scheduler on DSSoC0.
4. Ontology explains the required PEs and utilization; measure average utilization over developed apps.

DSSoC performer domains and applications

IBM T. J. Watson Research Center
Pradip Bose
Columbia University, Harvard University, Univ. of Illinois at Urbana-Champaign

CV+SDR
- Multi-domain application
- Multi-spectral processing
- Communications


IBM

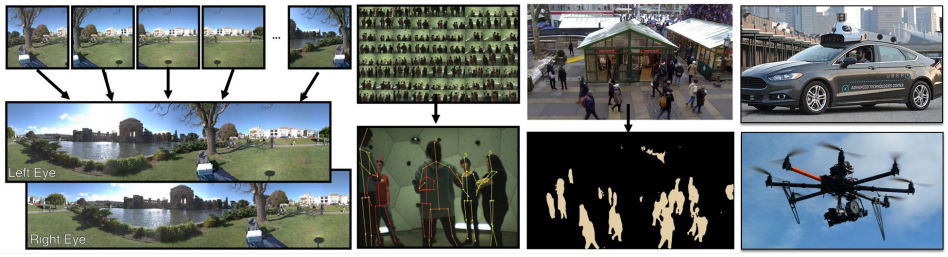
Arizona State University
Daniel W. Bliss
Univ. of Michigan, Carnegie Mellon University, General Dynamic Mission Systems, Arm Ltd., EpiSys Science

SDR
- Unmanned aerial
- Small robotic & leave-behind
- Universal soldier systems
- Multifunction systems


PlastyForma

Stanford University
Mark Horowitz
Clark Barrett, Kayvon Fatahalian, Pat Hanrahan, Priyanka Raina

Computer Vision
- Still image and video processing
- Autonomous navigation
- Continuous surveillance
- Augmented reality

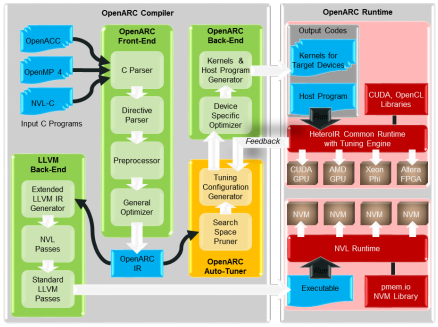


Stanford

Google/YouTube

Oak Ridge National Laboratory
Jeffrey Vetter

SDR
- Communications and signal processing focused
- Up-front processing / data cutdown
- Improving understanding of processing systems



ORNL

www.darpa.mil