Extending/Optimizing the USRP/RFNOC Framework for Implementing Latency-Sensitive Radio Systems

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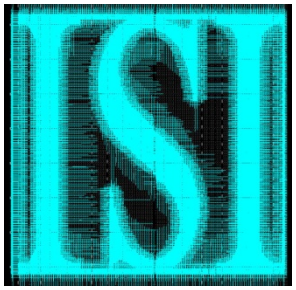
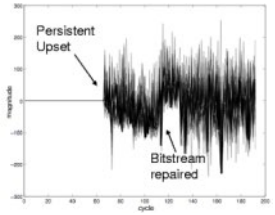
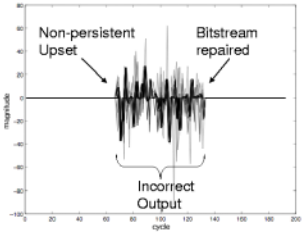
USC Information Sciences Institute

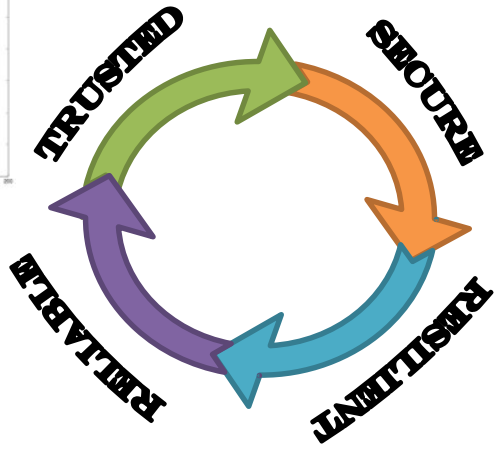
- **Reconfigurable Computing Group @ USC/ISI**
  - Over 20 years performing cutting edge FPGA research
  - > 100 Journal and Conference publications
  - Focused on FPGA and ASIC, System-Level Design, Productivity, TRUST and Security
  - Custom ASIC/FPGA CAD Tool (TORC)

- **ISI: A Large, vibrant, path-breaking research Institute**
  - Part of USC's Viterbi School of Engineering located in "Marina Tech Campus" (Marina del Rey) and in Arlington, VA
  - >$80M per year in funding from a diversified base of sponsors
  - ~300 people mostly research staff
  - Facilities to conduct ITAR, classified, and unclassified research









Overview

- Discuss Extensions/Optimizations to the UHD/RFNOC that allowed us to meet stringent *latency requirements* of the transceiver
- Experiences, lessons learned, and development efforts to implement a broadband CSMA/CA based OFDM transceiver on an Ettus E310 USRP Software Defined Radio (SDR) platform.
- Supports link layer latency-cooperative transmissions

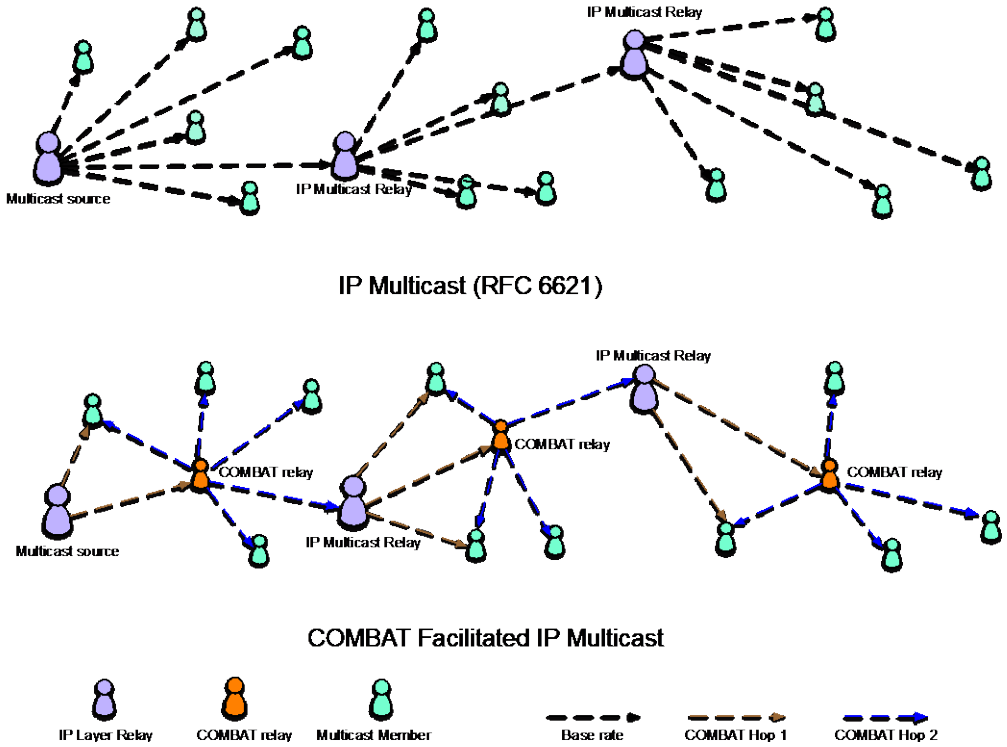
COMBAT Project



- **Over 95% of casualties in Operations Enduring Freedom, Iraqi Freedom, and New Dawn occurred after operations transitioned from linear, conventional fights to the nonlinear, nonconventional stabilization phase**
  - –A majority of missions during the nonconventional stabilization phase are carried out by dismount squads at the tactical edge
  - –Sharing situational awareness among soldiers is vital to mission successes
  - –Multicast plays an increasingly important role in edge networks
- **Goal: Improve the throughput of wireless multicast and broadcast in dismounted squad networks in order to significantly enhance the situational awareness at the tactical edge**

Sources:
1. C. Thielenhaus, P. Traeger, E. Roles, “Reaching forward in the war against the Islamic State,” PRISM, Nation Defense University 12/2016
2. E. Roles, Presentation on RAA in DARPA Industry Day, Jan. 2017

COMBAT Innovations

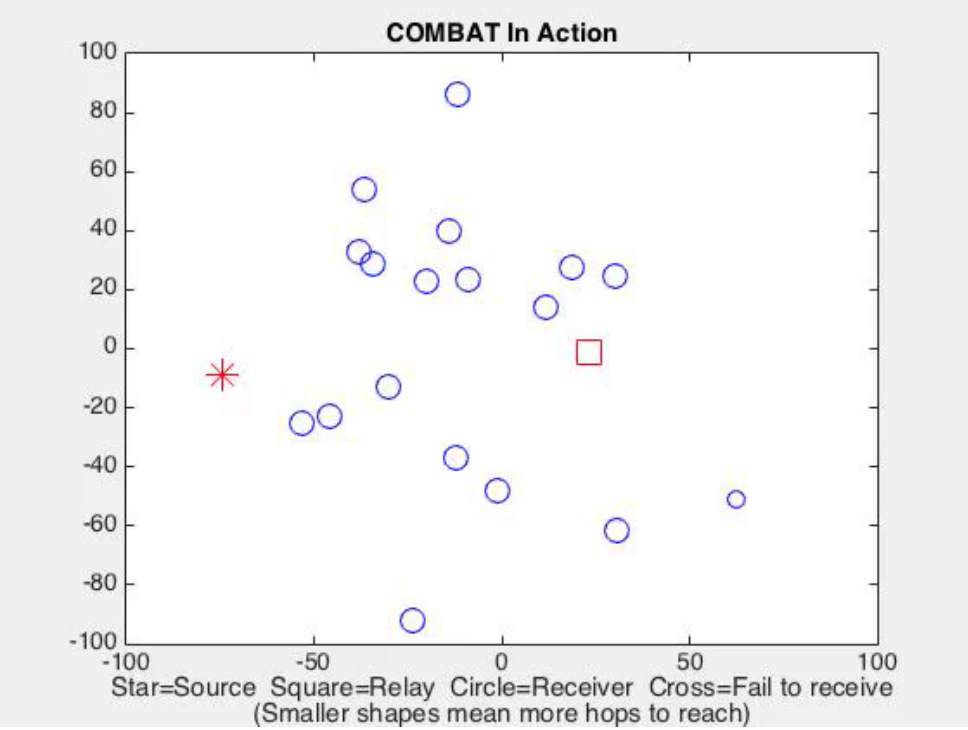


- ✓ Higher Data Rate
- ✓ Transparent to IP Layer
- ✓ Responsive to Channel
- ✓ Efficient Channel Utilization
- ✓ Reduced Complexity

- **COMBAT system works to support and improve IP multicast schemes such as the SMF in RFC 6621**
  - IP multicast to provide connections among clusters
  - Local mobility within clusters is handled by COMBAT in the link layer

System Level Simulation

- **Simulation Setup**
  - Topology: Mobile distributed on a disc R=100 meter
  - Radio Propagation: Path loss + AWGN
  - Traffic: Multicast only from a random node.
  - Random Waypoint Model: Velocity (0.1-4 m/s), Pause duration (0-60 s).

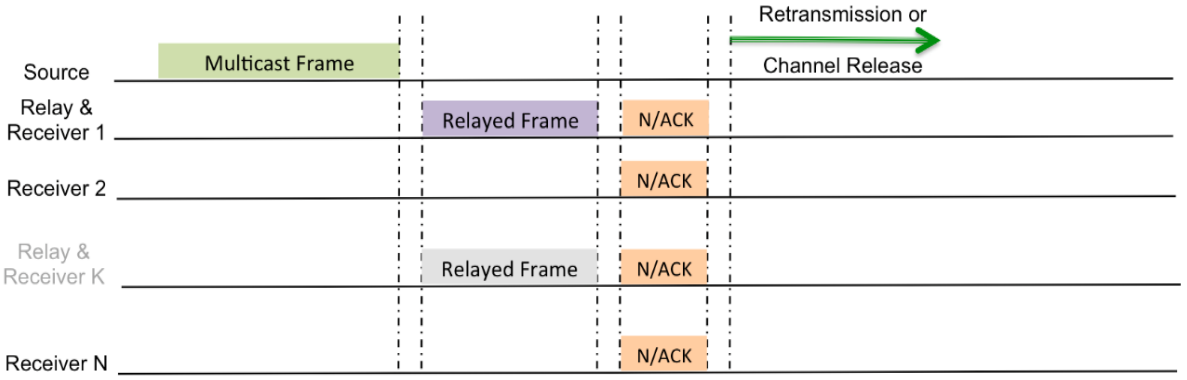


COMBAT Objectives

- **Demonstrate Improvements in Relay Throughput on Prototype OFDM Transceiver over Worst Link Scenario**
- **Requirements:**
  - 10 MHz Bandwidth, 40 MSPS
  - Utilize CSMA/CA

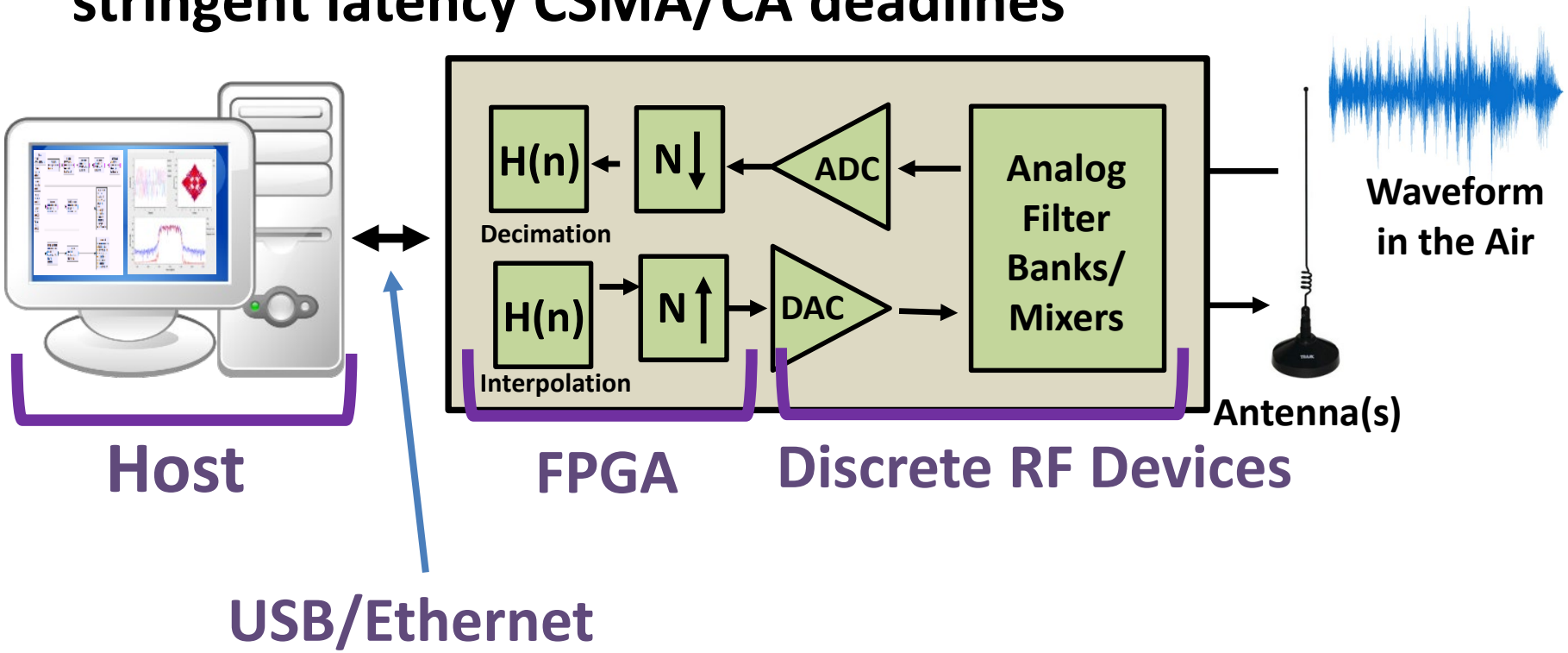
COMBAT Latency Requirements

- **Contention-free relay with PHY-assisted ACK/NACK**
- **CSMA/CA deadlines**
  - Enable Compatibility with Existing Systems
- **Throughput**
  - RX-to-TX Latency is critical for throughput



Software-Defined Architecture

- USRPs are latency-insensitive peripherals
- Latency is low, but SDRs not intended to meet stringent latency CSMA/CA deadlines



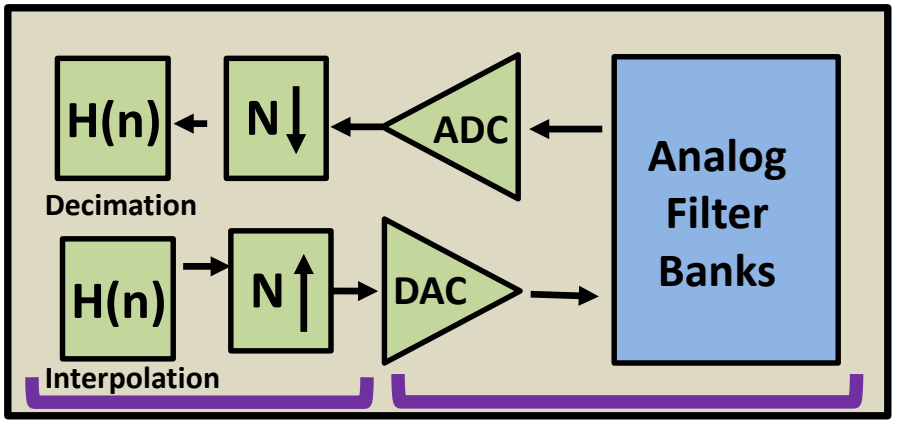
Enabling Advances in SDR Architecture

Standard SDR Architecture

Host

Ethernet/
USB
Connection

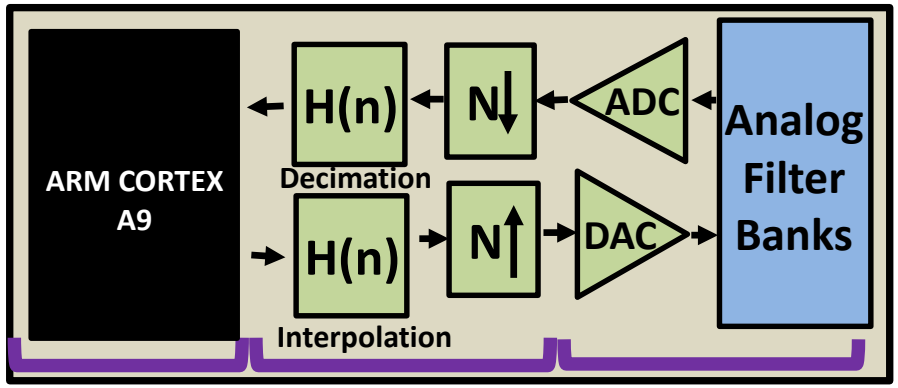
Block Diagram of N210



Embedded SDR Architecture

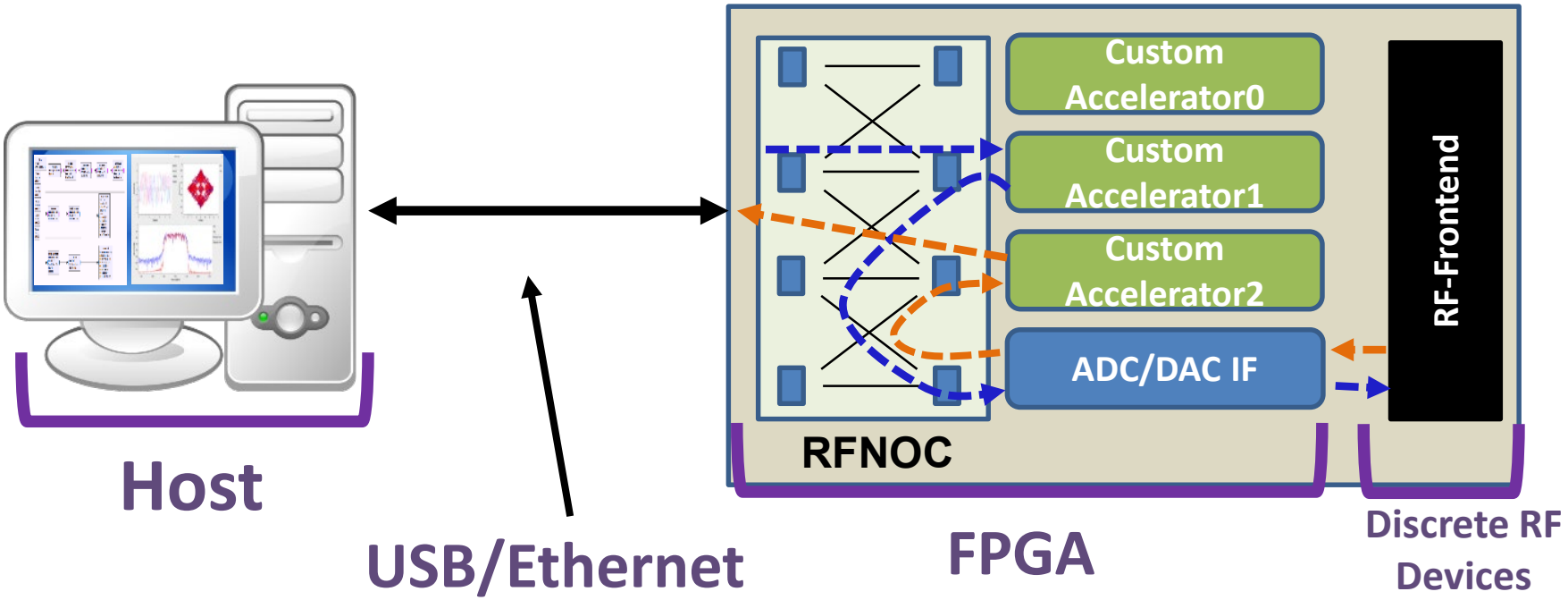
- Single Package
- Host/FPGA Latency Smaller
- Larger FPGA

Block Diagram of E310

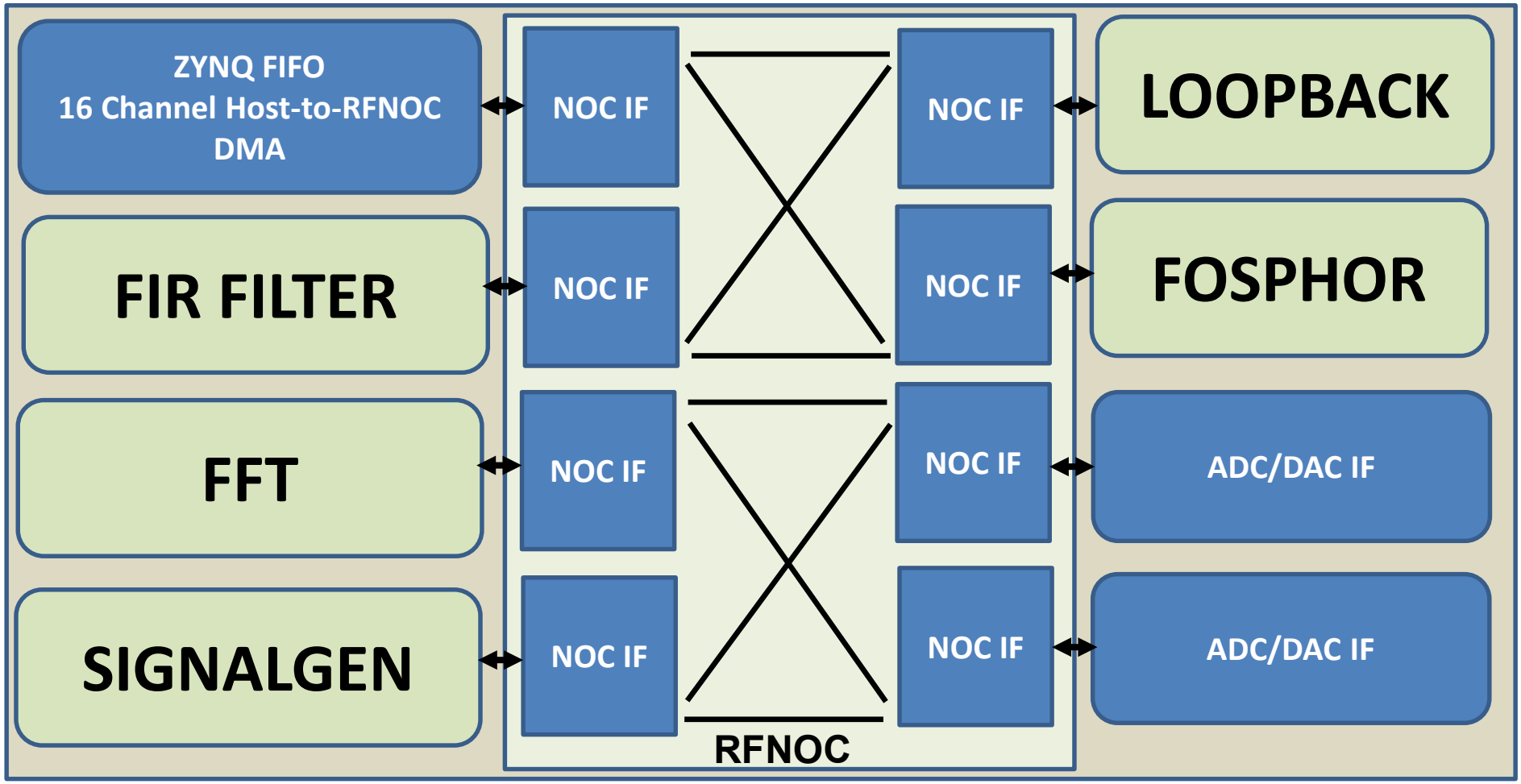


Radio Frequency Network on Chip (RFNOC)

- Dynamically Programmable Network-on-Chip
- Provides a design entry-point into the FPGA

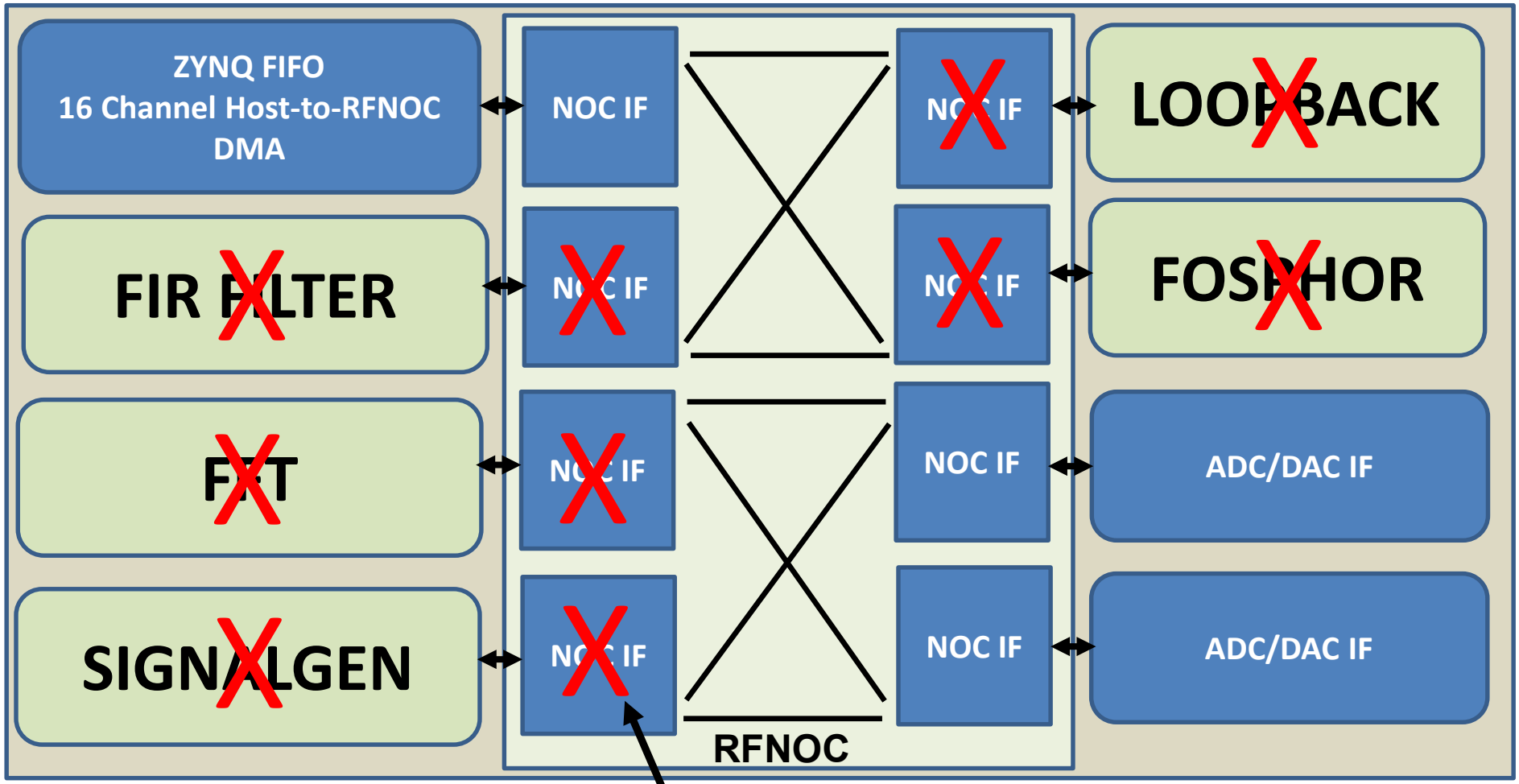


E310 RFNOC Base Design (FPGA Only)



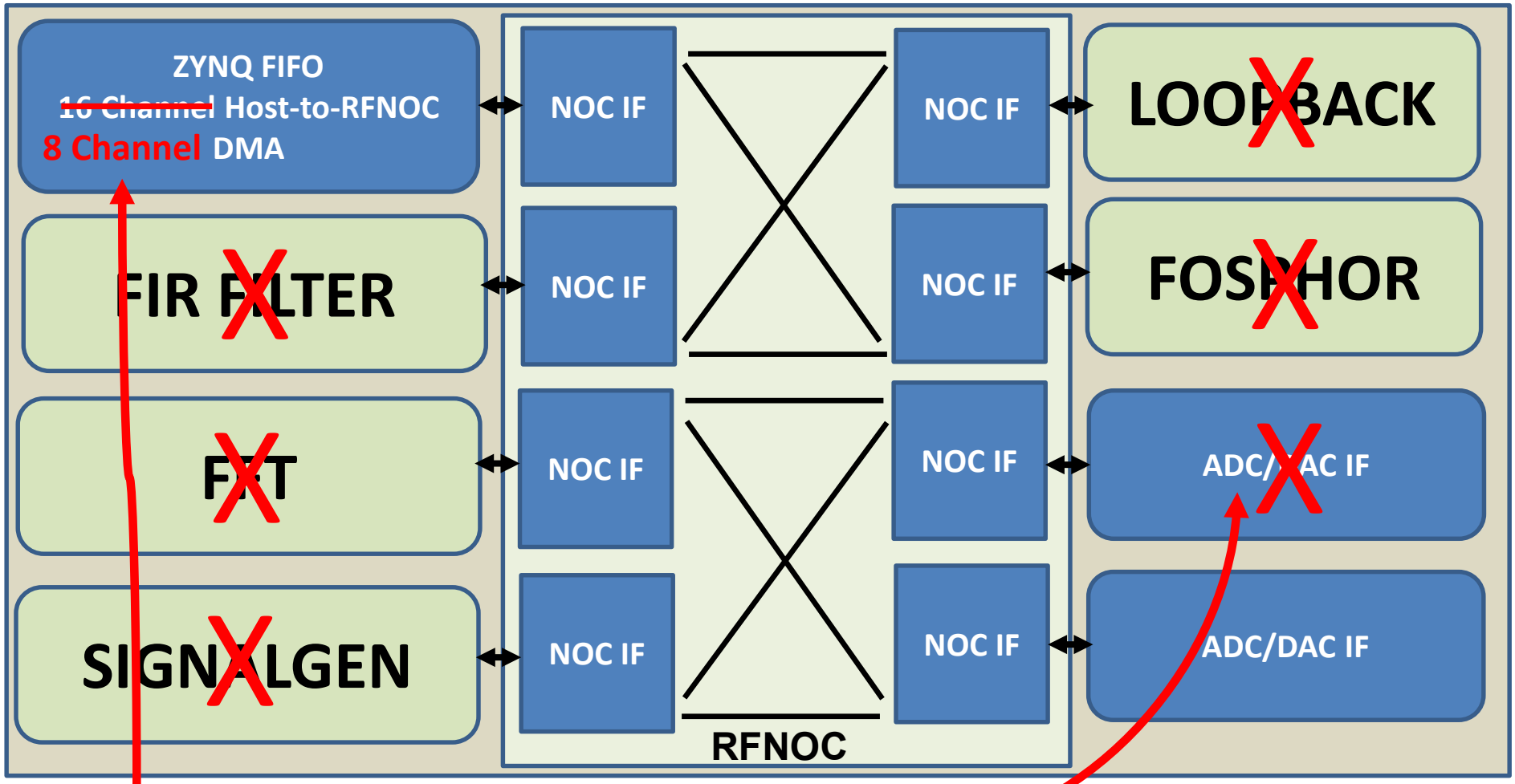
RFNOC Initial Configuration on E310

E310-RFNOC Base Design (FPGA Only)



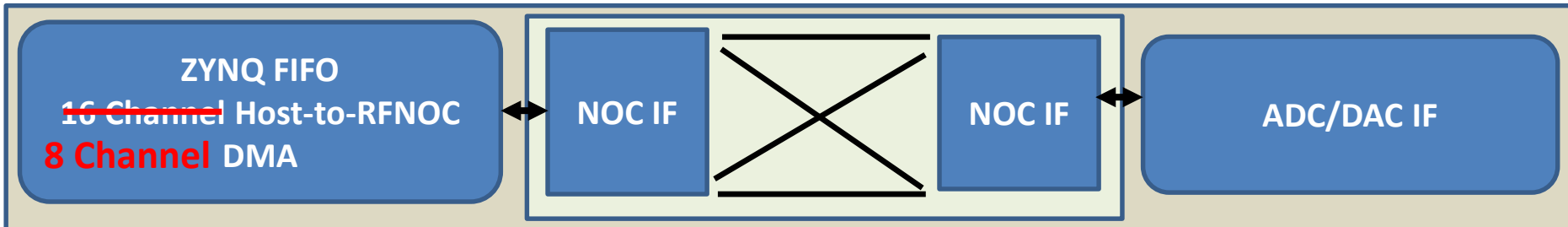
NOC IF are ~30% Resource Utilization

E310 RFNOC Base Design (FPGA Only)



*Required Extension/Update UHD

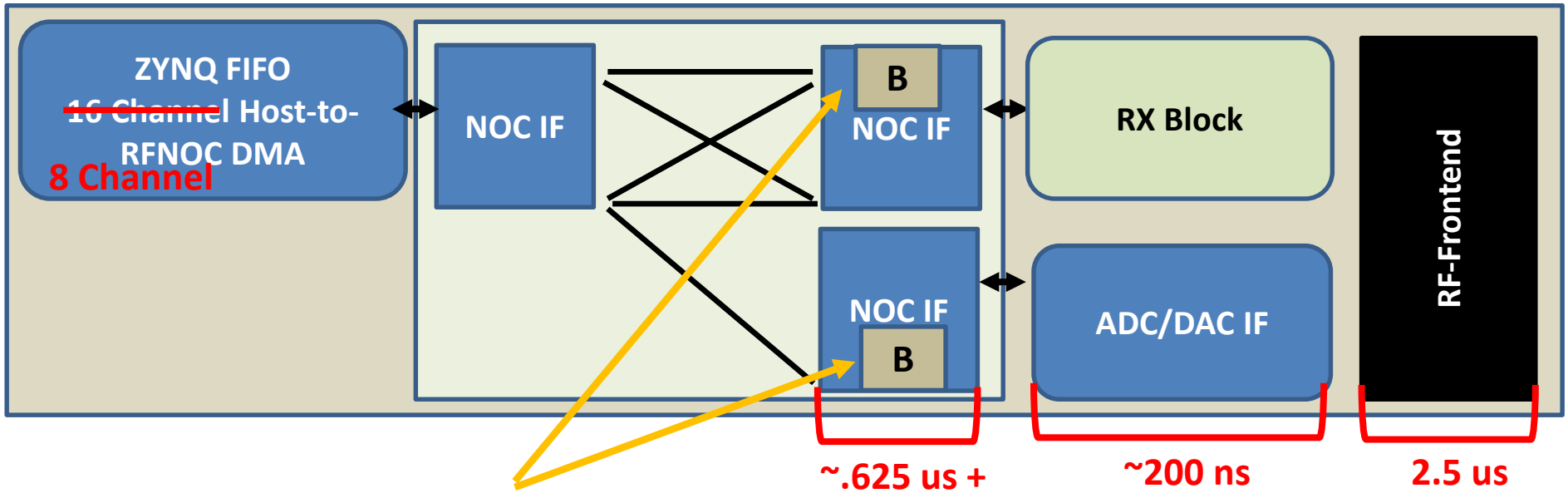
E310 RFNOC Base Design (FPGA Only)



Freed **53%** of the FPGA Resources!

	LUT	FF	BRAM	DSP
Total ZYNQ 7020 Device	53,200	106,400	140	220
RFNOC (Initial)	41,247 (77%)	55,783 (52.4%)	116 (82.8%)	146 (66.3%)
RFNOC baseline (RFNOC/Radio)	12,546 (23.5%)	15,840 (14.8%)	26 (18.6%)	0 (0%)
COMBAT optimized	45,319 (85.1%)	52,540 (47%)	104.5 (74.6%)	120 (52%)

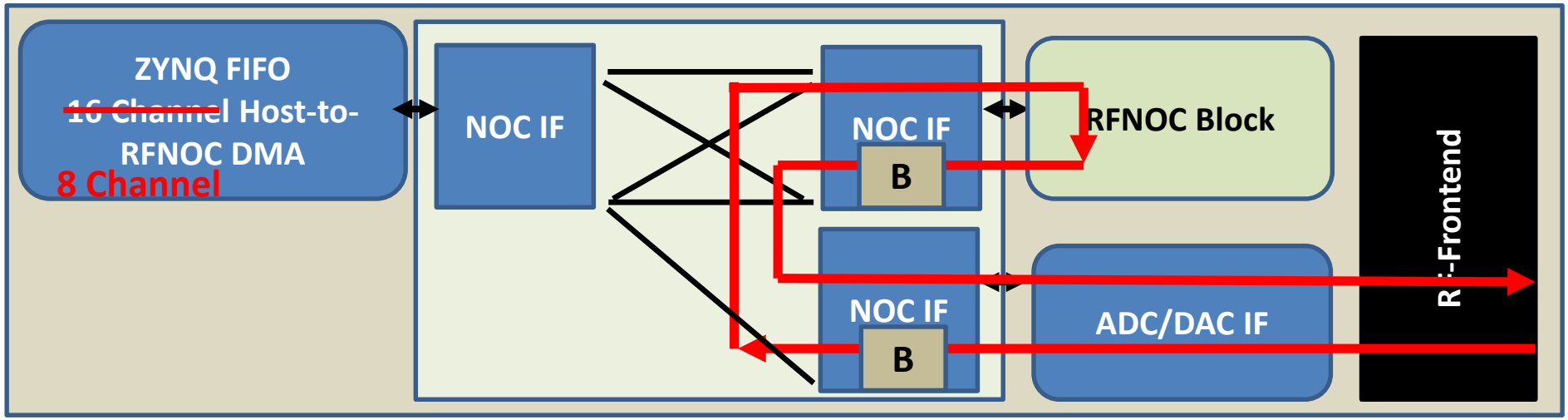
RFNOC Latency

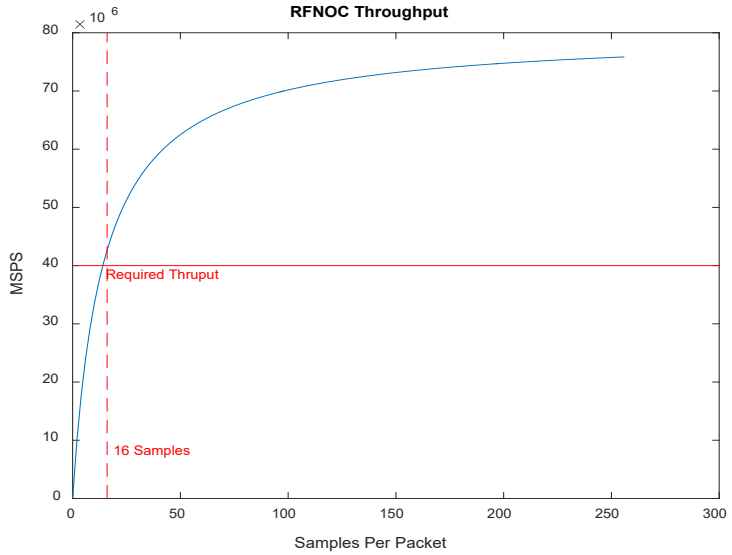


- Packet Buffering into RFNOC is Primary Cause of Delay.
- Dependent on Programmable Packet Size.
- Static Delay through RFNOC .625 us

RFNOC CLOCK = 50 MHz (400 MB/Sec)
CE CLOCK = 40 MHz (40 MSPS, 160 MB/Sec)

RFNOC Latency

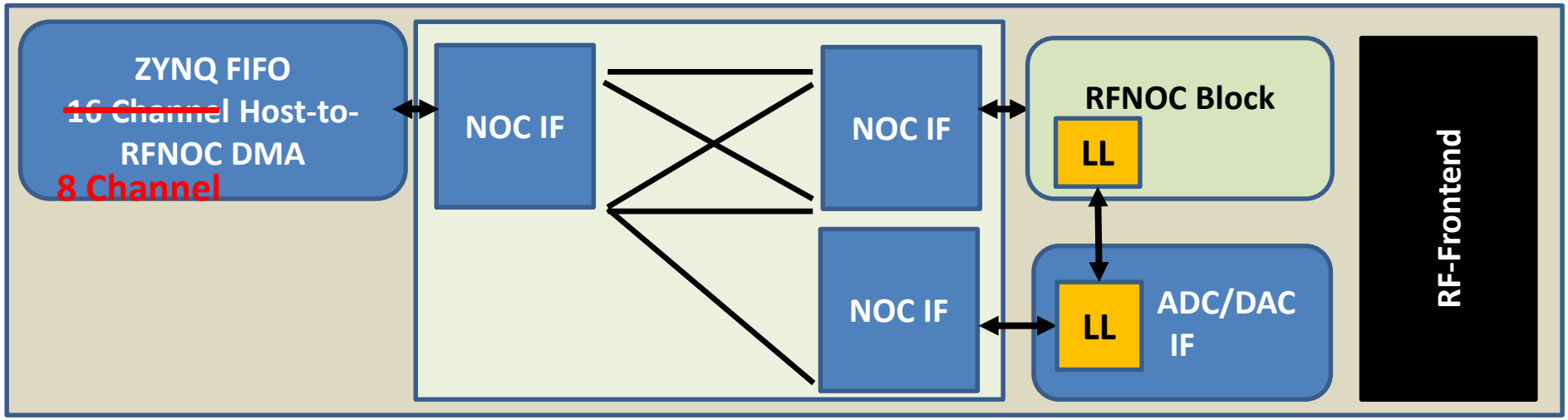




Minimum RX –to-TX Delay	
RFNOC	3.0 us
ADC/DAC IF	~250 ns
RF-Frontend	5.0 us
Total	**8.25 us**

RFNOC CLOCK = 50 MHz (400 MB/Sec)
CE CLOCK = 40 MHz (40 MSPS, 160 MB/Sec)

Low-Latency RFNOC Extension



Low-Latency RFNOC Block Benefits:

- **Minimum Latency Limited by RF configuration and a couple cycles**
- **Selectable – Select LL for TX, RX, or TX/RX**
- **Maintains Compatibility with RFNOC/UHD; however needs additional work to support GNURadio**

Minimum RX –to-TX Delay	
~~RFNOC~~	~~3.0 us~~
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Total	**5.25 us**

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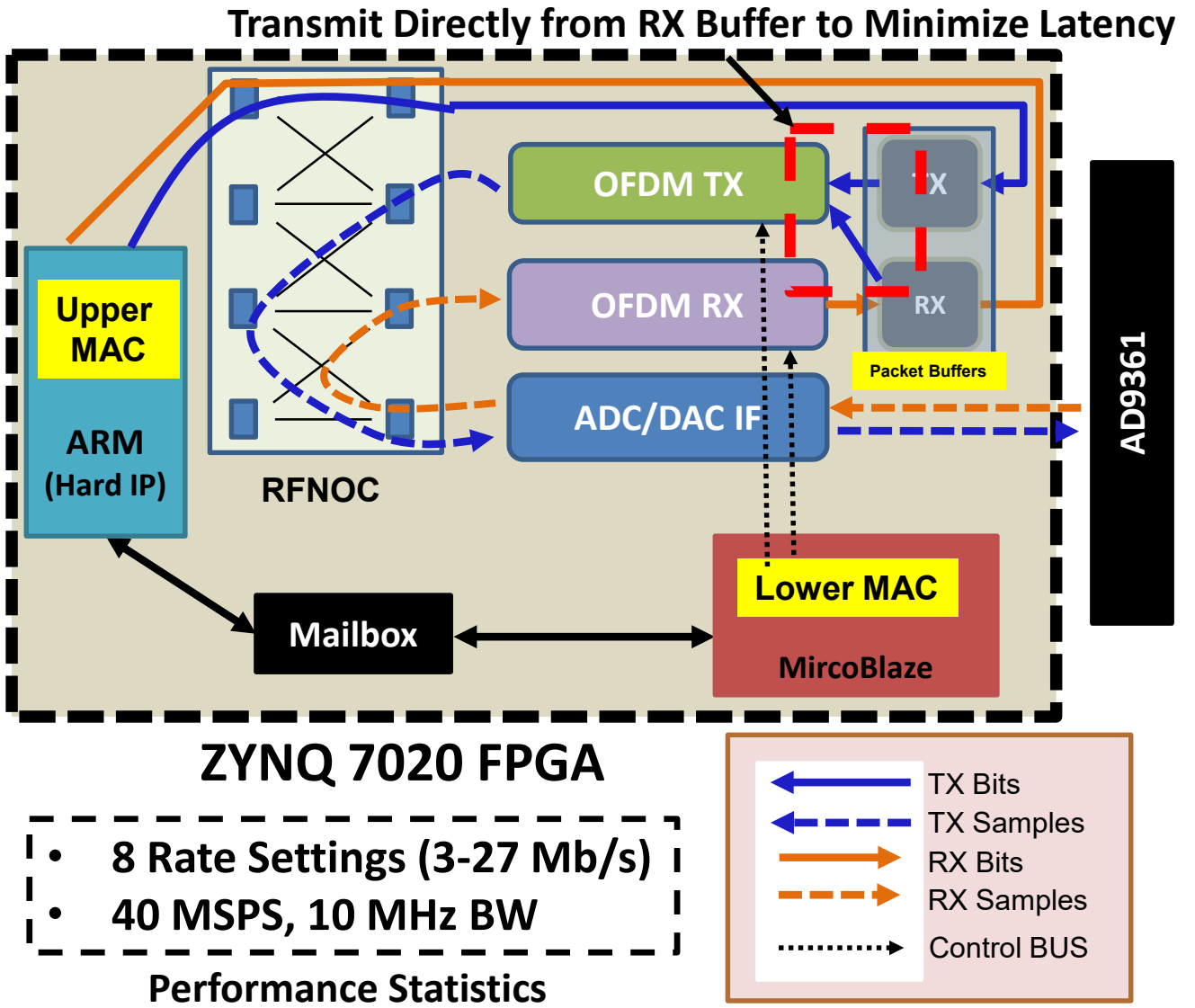
Other Mods/Extensions to E310/UHD

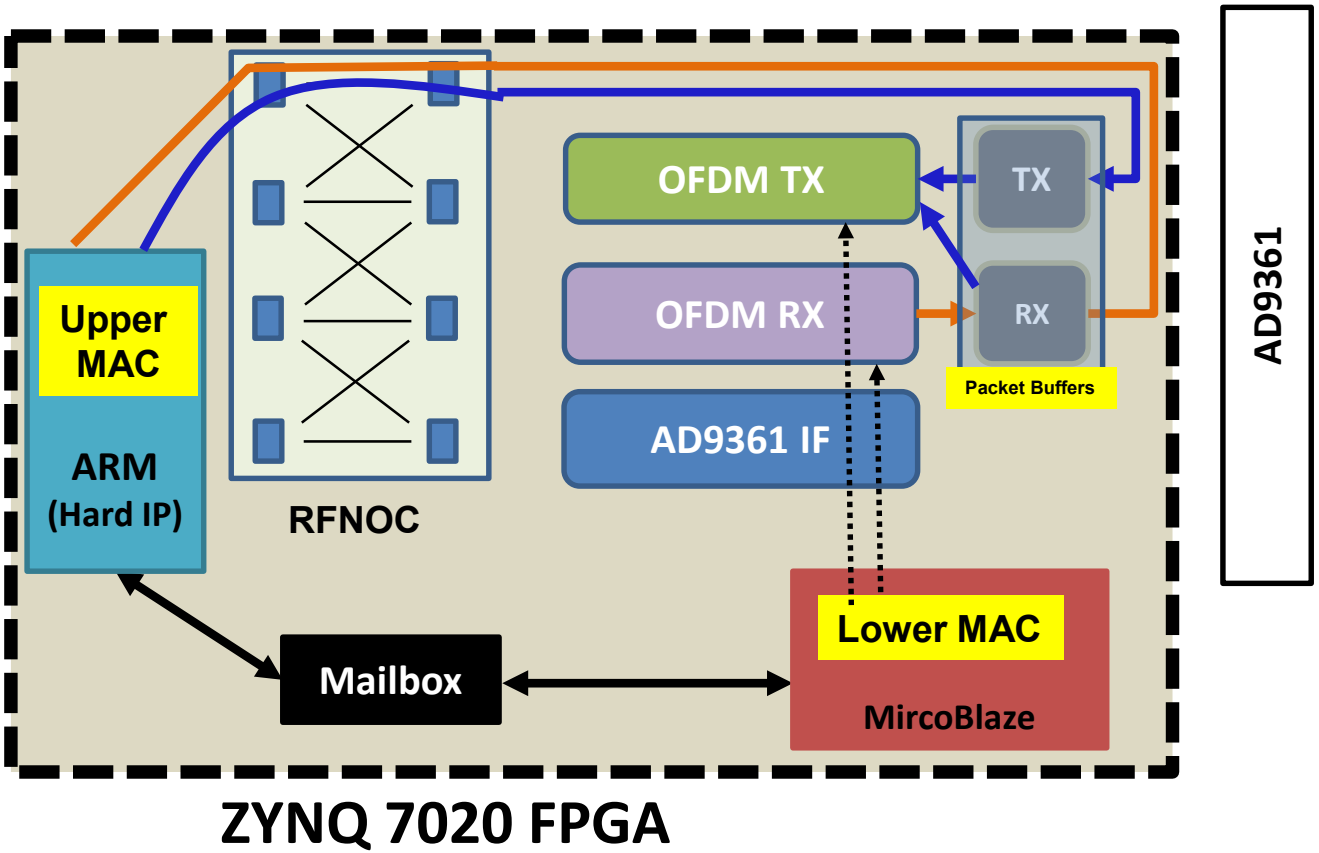
- **Updates to REPO**
  - Added Block Diagram Build Flow
  - Construct Vivado GUI Project for Block Diagrams
  - Smoother Integration Vivado IP
- **Exposed AD9361 Control**
  - Exposed SPI Interface to Write AD9361 Control
- **Debugging**
  - Built Custom Cable and Implemented Virtual JTAG
  - Integrated Virtual JTAG Server/Driver

OFDM Transceiver Architecture

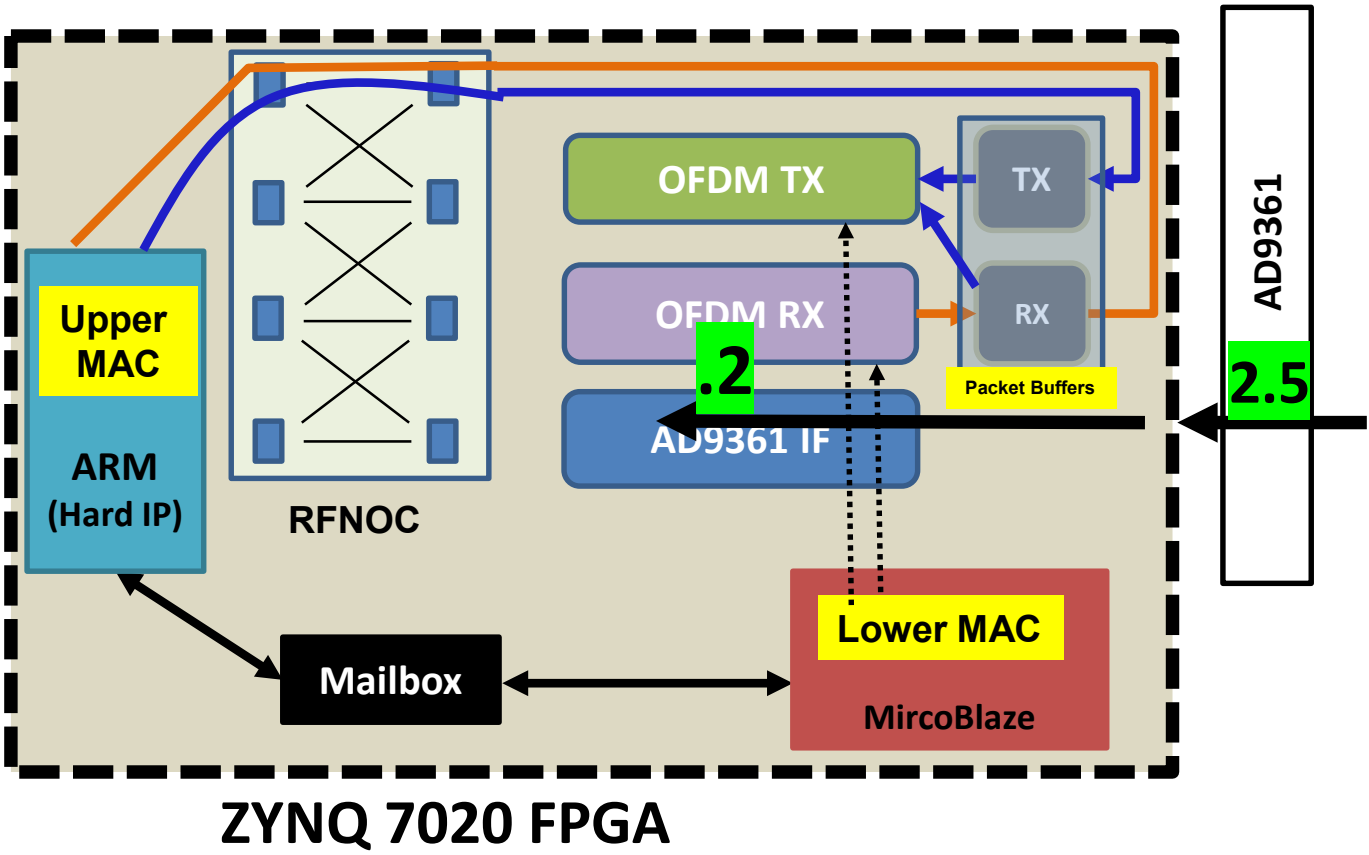
1. **Upper MAC**
   a) Wraps Payloads in Packets
   b) Manages COMBAT Protocols
   c) Moves Packets to and from Packet Buffers
2. **Lower MAC**
   a) Configures and Manages RX and TX
   b) Handles latency sensitive protocol (e.g. relay forwarding, etc.)
   c) Inform Upper MAC of received packets.
3. **Packet Buffers**
   a) TX: Hold packets that have been staged from Transmission
   b) RX: Hold packets that have been received and decoded
4. **OFDM RX/TX**
   a) TX: Transform Bits to OFDM baseband samples.
   b) RX: Transforms OFDM baseband Samples to bits



Latency Analysis



Latency Analysis



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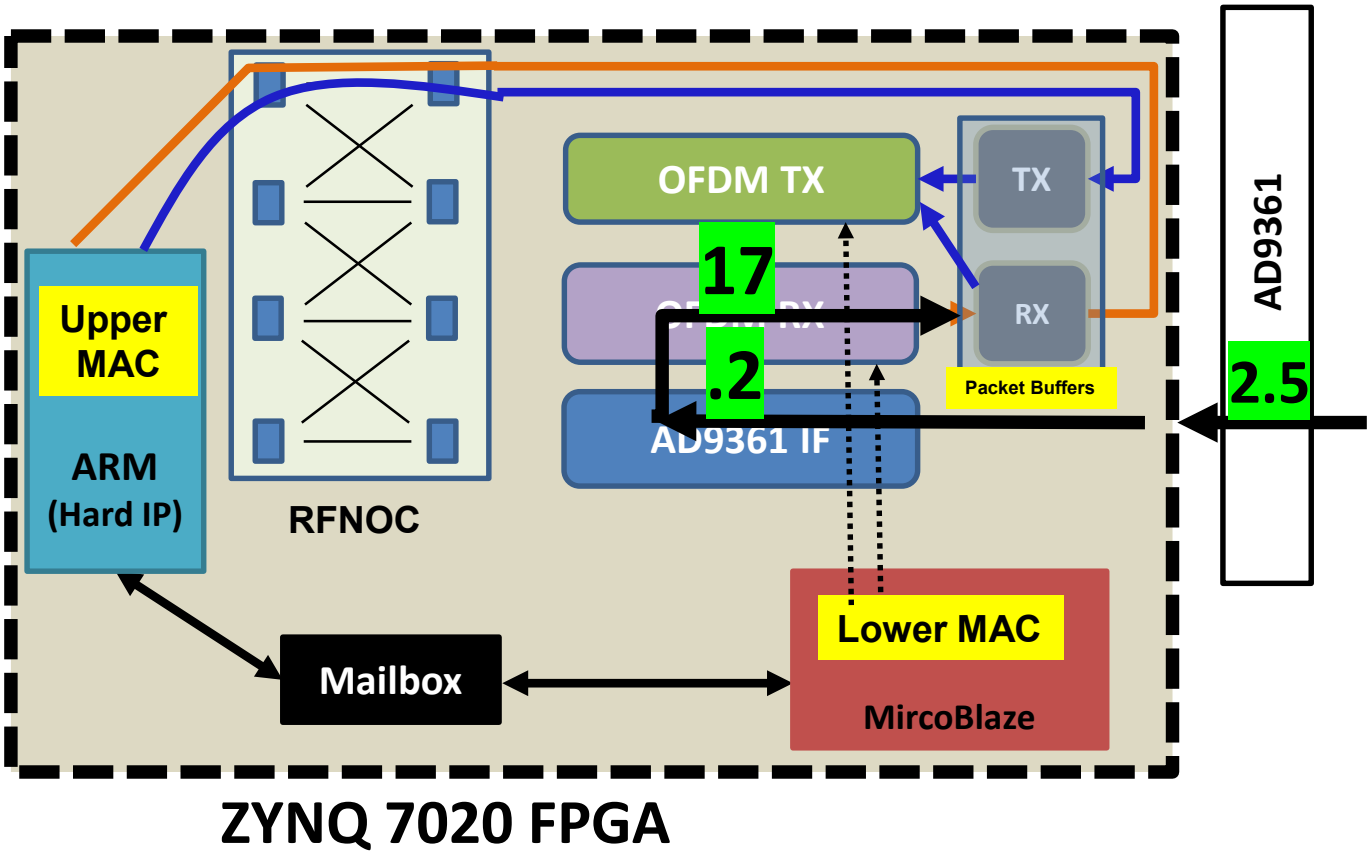

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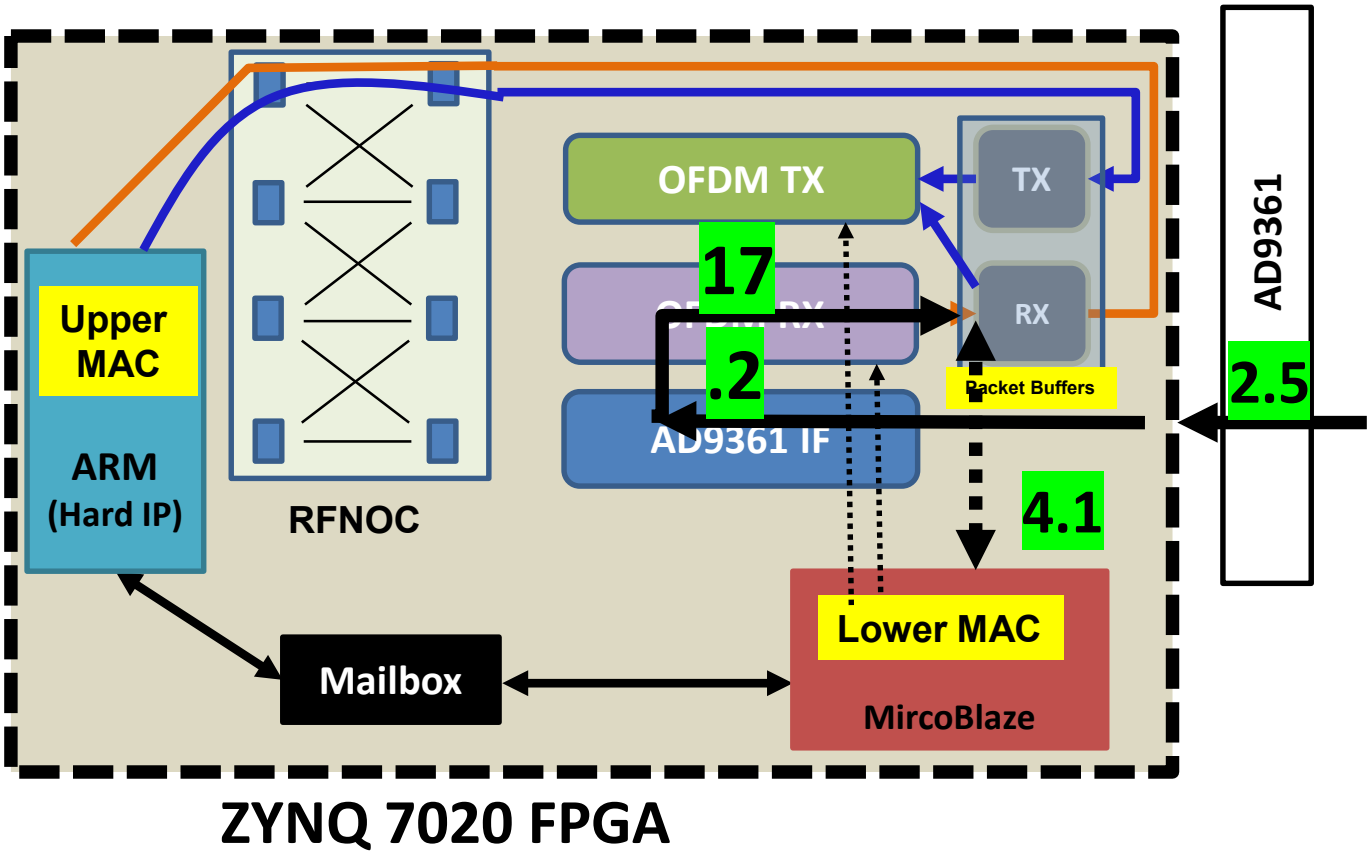
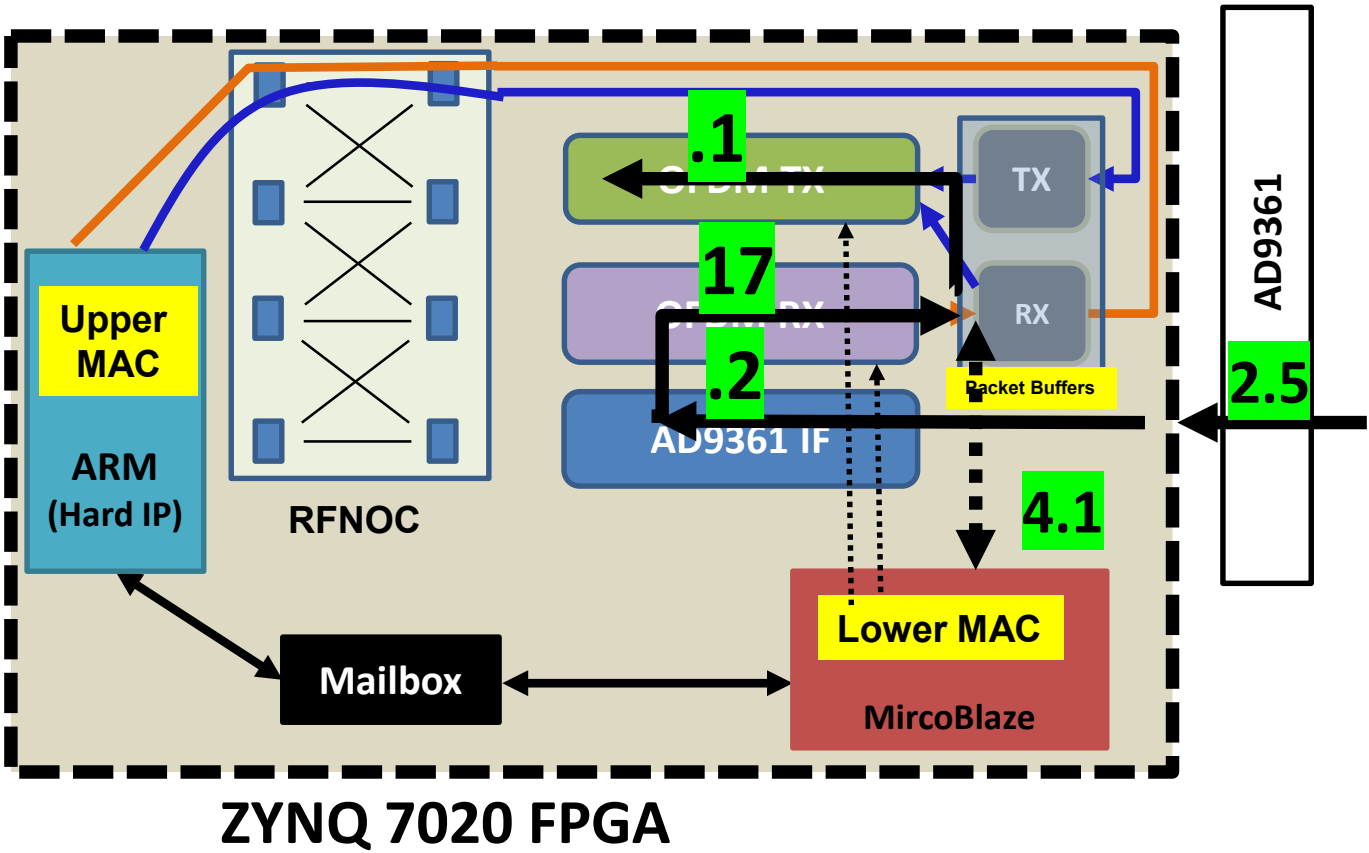


Latency Analysis



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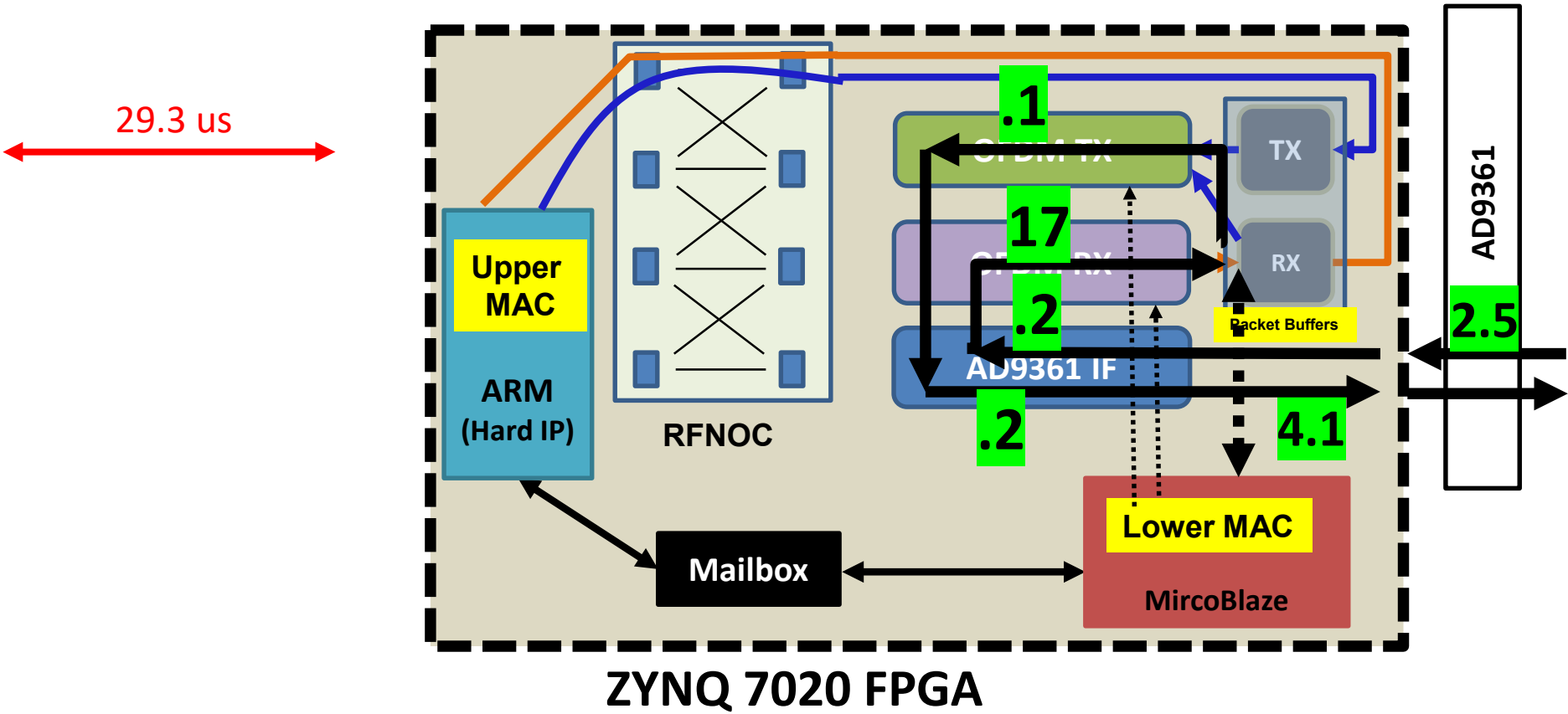
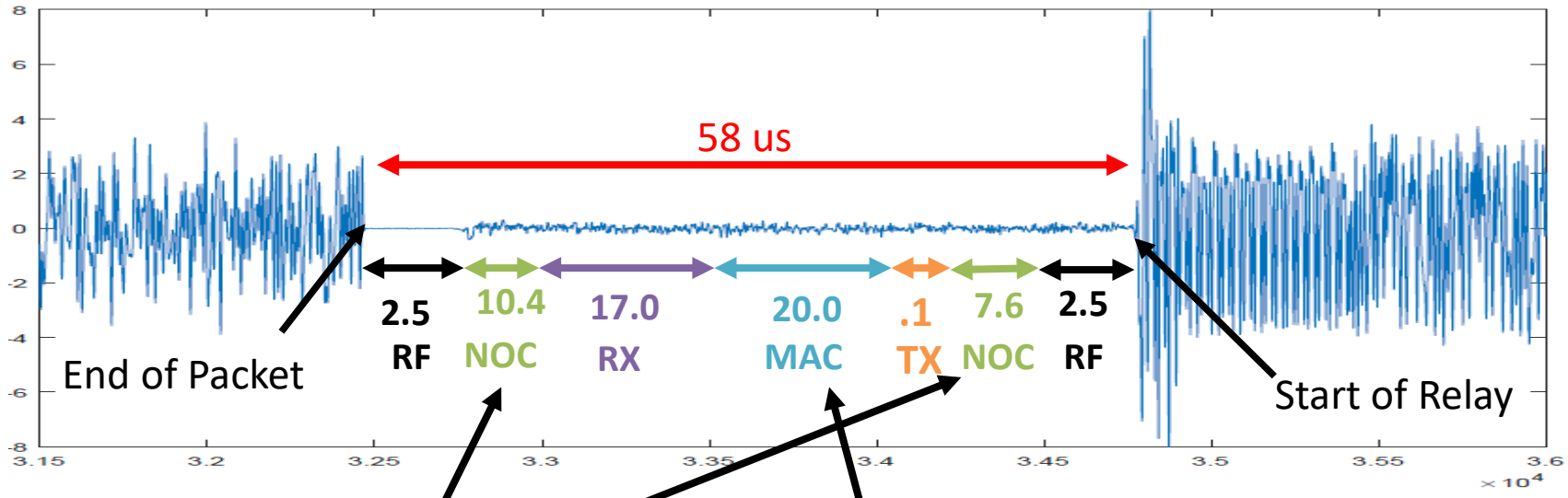


RFNOC Latency Measurements



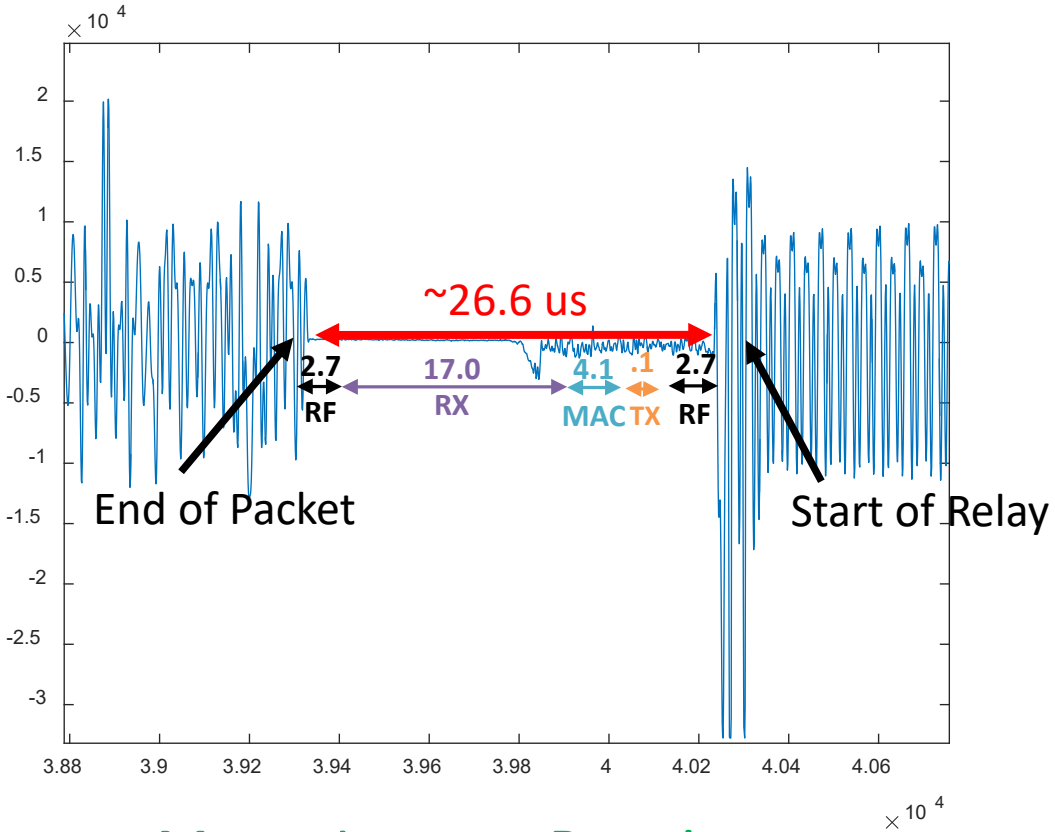
NOC Delays Primarily Related to RFNOC Packet Size & Buffering

Opportunities to further optimize MAC Code can be optimized

RX-to-TX Latency exceeds Requirement (34 us)!
Best Case Relay of 10.98 Mb/S

Low-Latency IF Measurements

- **Reduced RX-to-TX Latency by 50%!**
- **Optimizations:**
  - **RFNOC**
    - Adjusted FC Buffers
    - Adjusted FC ACKs
  - **MAC Code**
    - Added –O3 (50%)
    - Adjusted Algorithms
    - Overlapped More relay processing with RX
    - Added B. Shifter, Mult



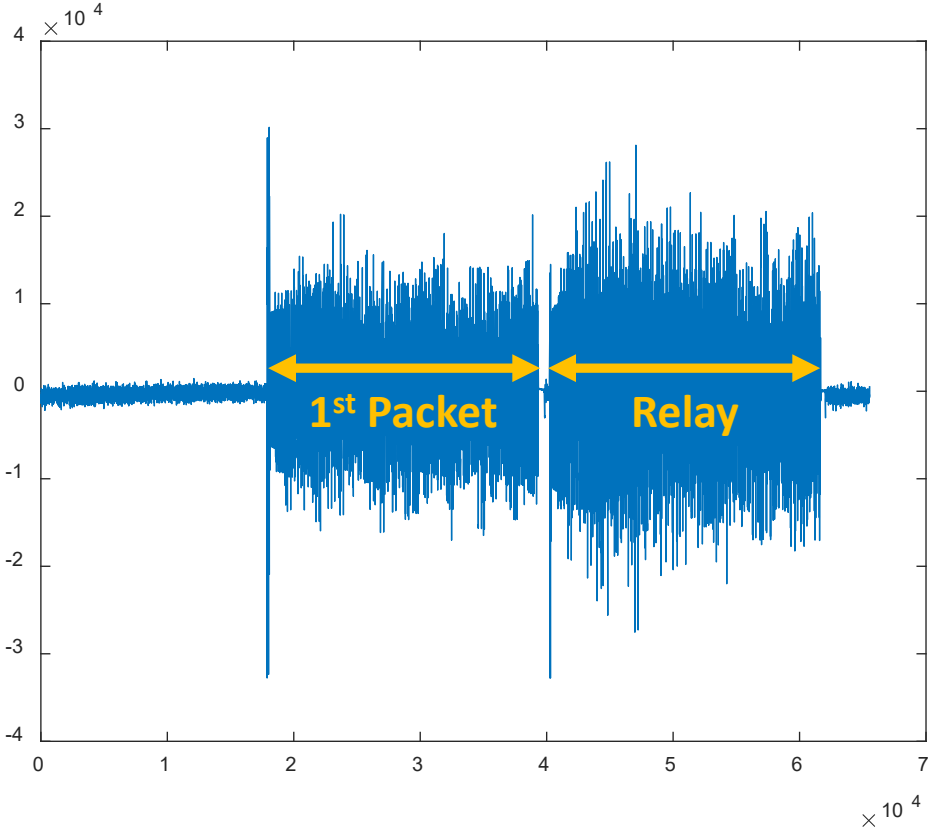
- Meets Latency Requirement

+4.7% Achievable Relay Throughput!

- **2.5% Packet loss due to TX Underrun**
  - **Likely due to Flow Control ACK**

Low-Latency IF Measurements

OFDM Relay 18 Mb/s Rate



Relay Latency: 22.6 us

RFNOC Review

Benefits	Drawbacks
Simple FPGA Design Entry Point into Ettus Stack	Not Intended for ultra-low latency processing
Excellent for High-level Design Tools like GNURadio/RFNOC	No Abstraction for Low Latency Signals communicating between blocks (e.g. state-inputs and outputs)
Excellent for Modular Design	
Flexible	
Stock IP to Connect To RFNOC	

- We will be releasing our Low-Latency RFNOC Block and NOC Radio Extension as open-source shortly on https://github.com/ISI-RCG (likely location)
- Recommended using these cores for ultra-low latency processing

Conclusion and Summary

- **Implemented Latency-Sensitive CSMA/CA Radio System on USRP E310/E312**
- **Made Several Extensions and Improvements to Permit Latency Sensitivity**
  - Created Low-Latency Radio Block and Low Latency RFNOC Block Shell
  - UHD Updates that Permitted RX->TX without Host
  - Enabled Vivado Block Diagram Build Flow
  - Implemented Lower MAC In Microblaze Processor
  - Enabled TX to Read from RX Packet Buffer
  - Transfer Packets to/from FPGA Rather than Samples
- **Future Work:**
  - Push Abstraction Levels Higher (Mapping to GNURadio)

Questions