



ASOCS



## ModemX

Heterogeneous Multi-Core  
Architecture for SDR Applications

*making wireless convergence TRANSPARENT*

*making wireless convergence TRANSPARENT*

# Agenda

- ▶ Introduction
- ▶ ModemX Architecture
- ▶ Application Examples
- ▶ Summary



# Introduction

## ► ASOCS Introduction

- ▶ Developer of many-core embedded processors enabling seamless connectivity over diverse wireless networks
- ▶ Pioneer of ModemX technology
- ▶ Expertise in algorithms, DSP, software and firmware for wireless, cellular and broadcast
- ▶ Founded in 2003, Head quarters in Afek Park, Israel
- ▶ Investors



## ► ModemX technology

- ▶ Heterogeneous Many Core Architecture
- ▶ Designed specifically for wireless application
- ▶ Field proven in various applications



# Introduction – Multicomm SDR platform

- ▶ Support of various waveforms and technologies.
  - ▶ Modulation schemes, Coding schemes.
  - ▶ Multiple access schemes.
  - ▶ Bandwidth and bit rates.
- ▶ In-the-field upgradability.
- ▶ Concurrent operation of multiple standards Waveforms
  - ▶ Zero latency re-morphing from one waveform to another
- ▶ Competitive in area and power.
- ▶ Easy robust development path.
- ▶ Scalability: same platform to support a wide range of applications.



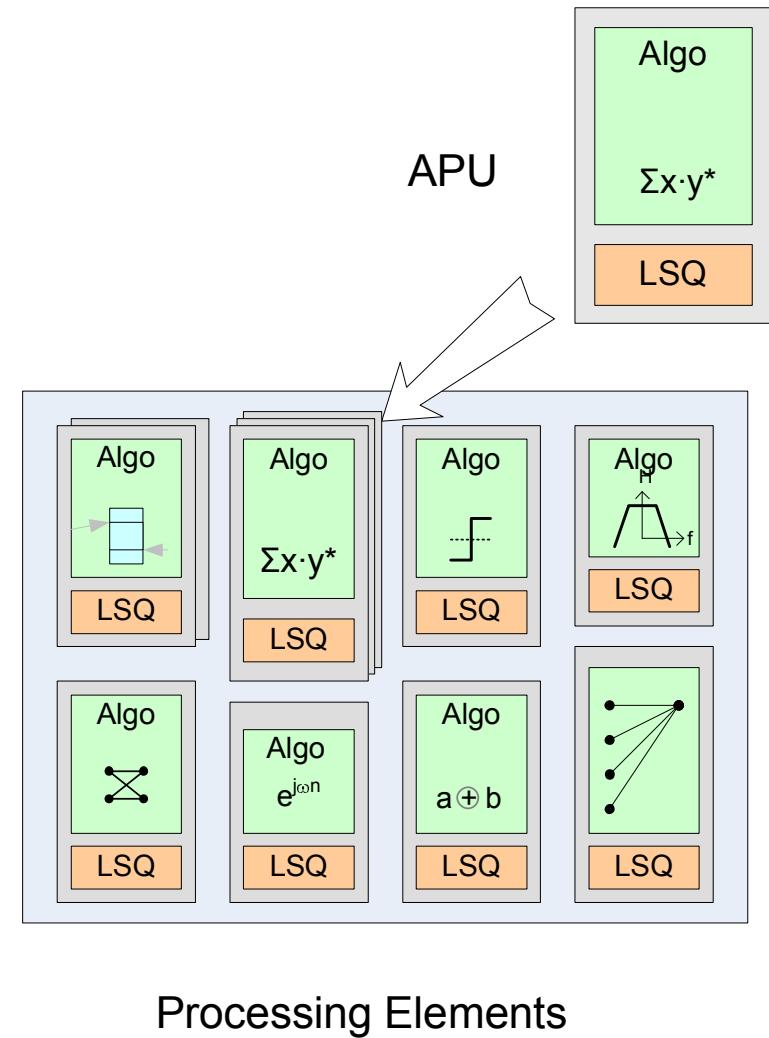
# Agenda

- ▶ Introduction
- ▶ ModemX Architecture
- ▶ Application Examples
- ▶ Summary



# ModemX architecture – Many Core Approach

- ▶ Heterogeneous Multi/Many Core Architecture.
- ▶ Core = Algorithmic Processing Unit (APU).
- ▶ Several types of APU.
  - ▶ # per type – design parameter
- ▶ Each APU is instantiated multiple times.
- ▶ 10s-100s of APUs in typical designs.



# ModemX Architecture – A closer look at APU

## ► Local Sequencer Unit (LSQ)

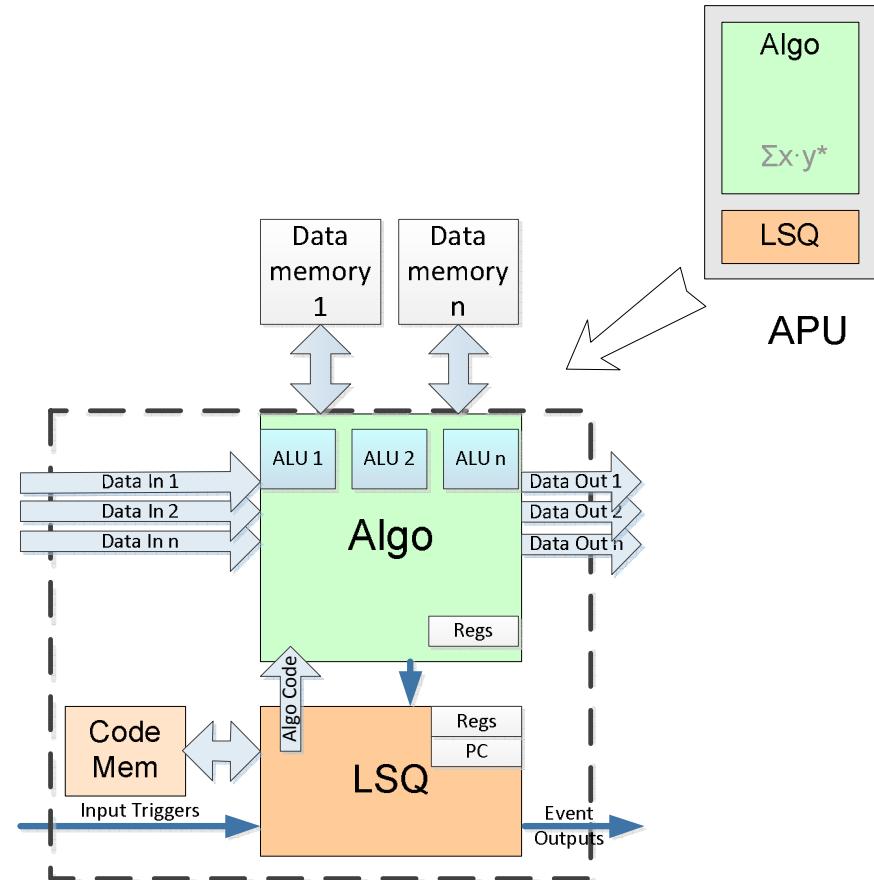
- ▶ Algo unit control:
- ▶ Cycle by cycle
- ▶ Configuration
- ▶ Flow control:
- ▶ Nested loops, branch, subroutine calls

## ► Algorithm Unit

- ▶ Specific to APU type.
- ▶ Efficient dedicated design.
- ▶ Multiple ALUs, registers.
- ▶ Access to Data memory

## ► Interfaces to other APUs

- ▶ Data
- ▶ Control
- ▶ Handshake signals



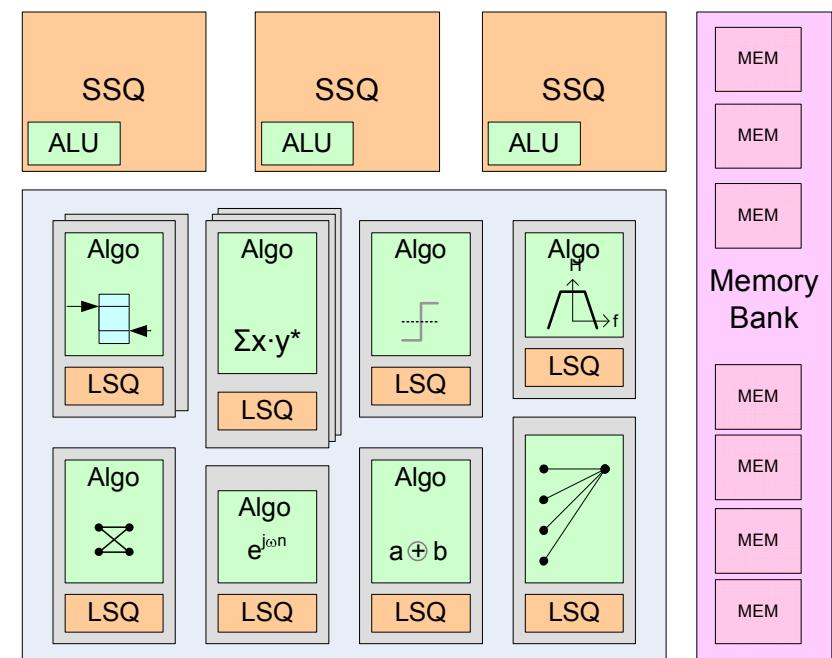
# ModemX Architecture- SSQ and Memory bank

## ► Standard Sequencer (SSQ)

- ▶ 16 bit RISC processor
- ▶ High level control
- ▶ APU configuration
- ▶ No participation in Data crunching
- ▶ One for each concurrent standards
- ▶ # - design parameter.

## ► Memory Bank

- ▶ Pool of single/dual port memories
- ▶ Data for APUs
- ▶ Code Data for SSQs
- ▶ Very high bandwidth interconnect.



# ModemX Architecture - APU Types

- ▶ Functional partitioning:
- ▶ Result of wide scope survey of wireless communication standards.
- ▶ Several APU types: varying in functionality & complexity.
- ▶ Some provide a high degree of flexibility and programmability

## Memory Gateway APU

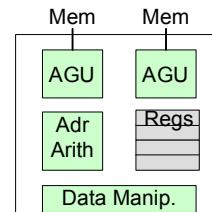
### **Memory intense operations**

Complex memory structures

Interleavers

Delay lines

Sample buffer



MGW APU

## Multiply Accumulate APU

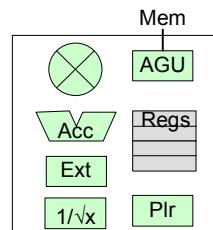
### **For real/complex signal processing**

Multiply/add/extract

Native complex arithmetic

Polar operations

$1/x$   $1/\sqrt{x}$ , semi - floating point



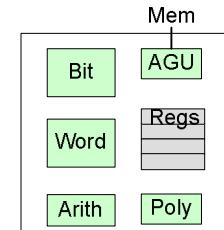
MAC APU

## Bit Manipulation APU

### **For operation on bits and words**

Scrambling, Encoding/Decoding

Message construction/parsing



BITMAN APU

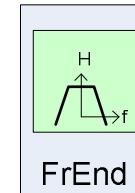


# ModemX Architecture - APU Types

- ▶ More APU examples
- ▶ Ubiquitous operations
- ▶ More specific functionality
- ▶ Less programmability

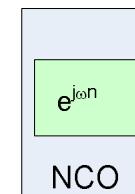
## Front End APU

Channel Filtering  
Rate conversion  
I/Q Correction  
DC correction



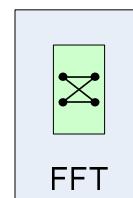
## Numerically Controlled Oscillator APU

Phase/frequency correction  
CORDIC operations



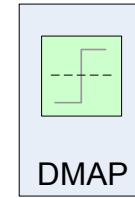
## FFT APU

FFT/ IFFT  
WHT  
Freq/domain filtering



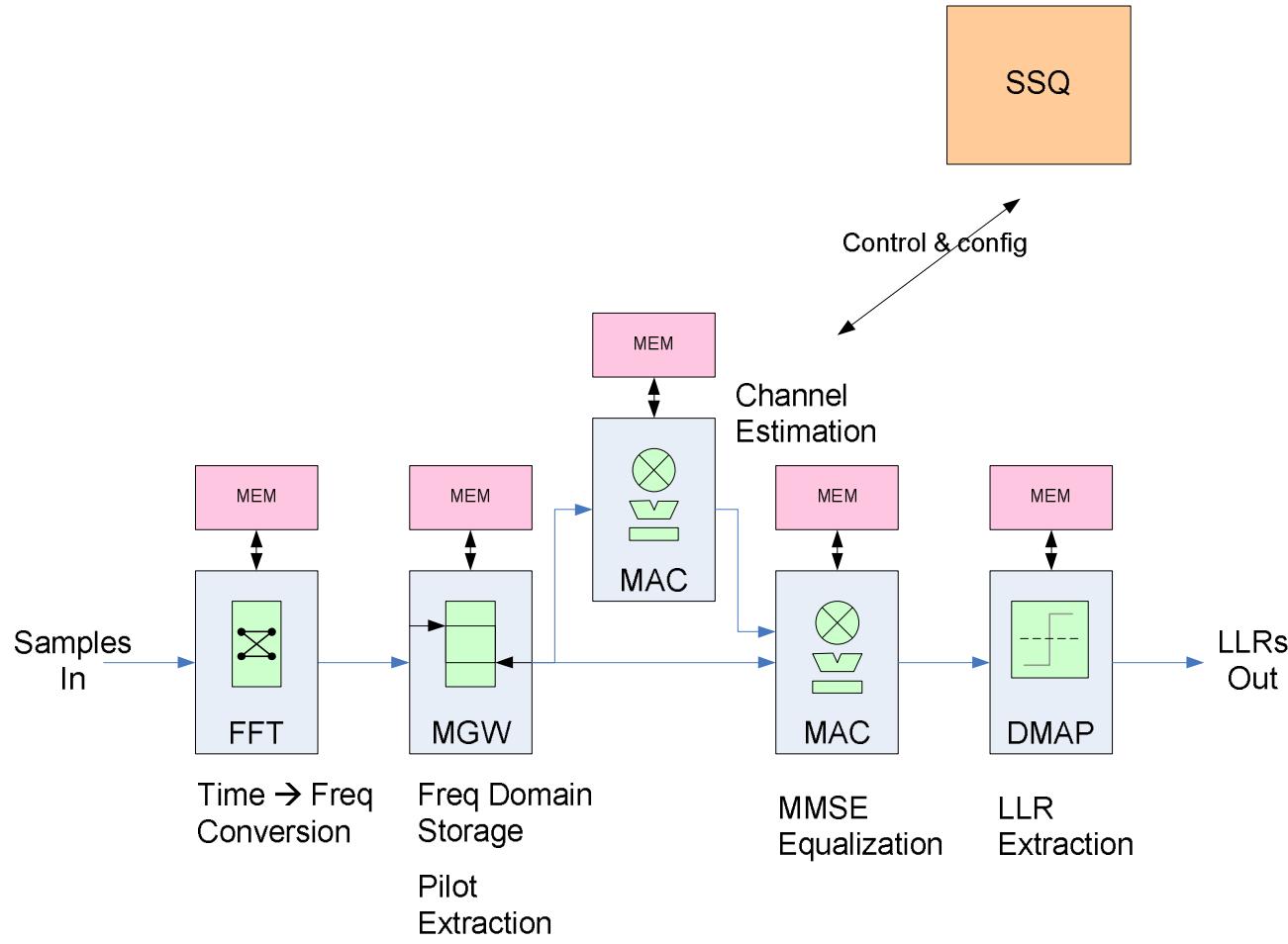
## Demapper APU

QAM slicing  
LLR extraction



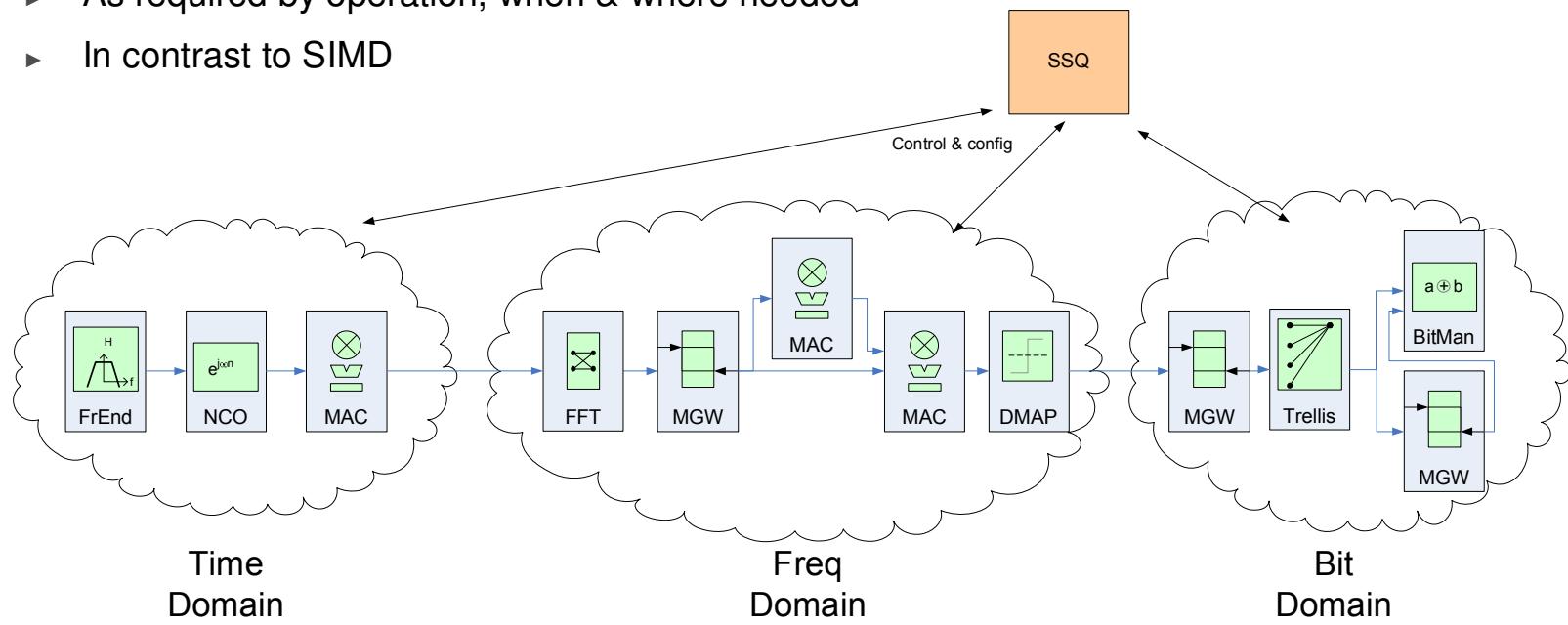
# ModemX Architecture - Processing Segment

- ▶ Multiple APUs form a Processing Segment
- ▶ Example: OFDM Frequency Domain Processing



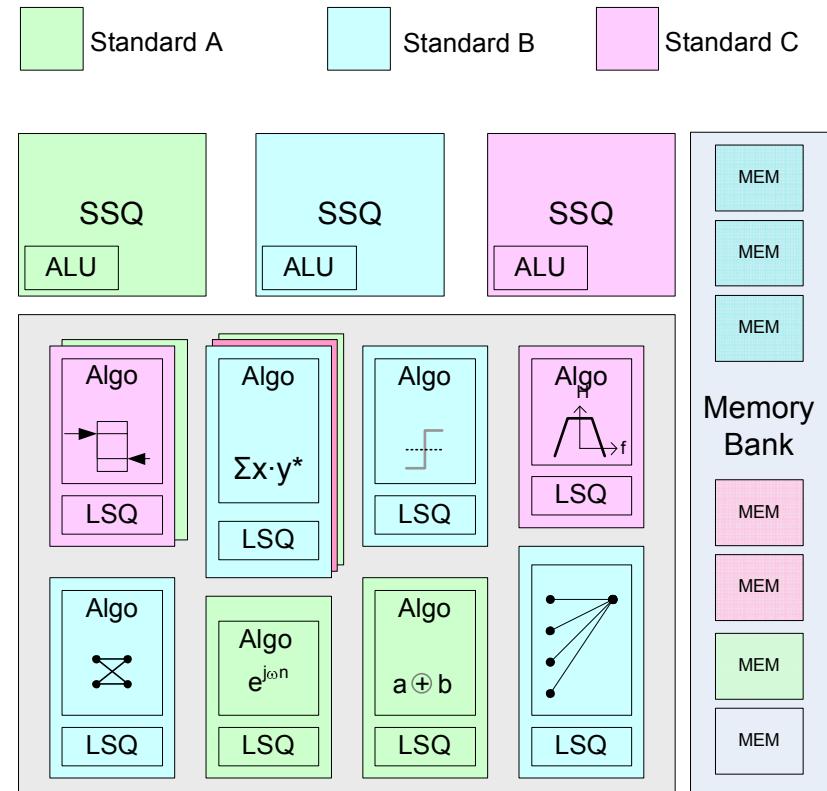
# ModemX Architecture - Multiple segments

- ▶ Zooming out to a complete design: Multiple processing segments
- ▶ Concurrently, or Sequentially
- ▶ Multiple Ad-Hoc processors.
  - ▶ Each tailored to a specific domain
  - ▶ With optimal processing resources
- ▶ Significant processing power
  - ▶ As required by operation, when & where needed
  - ▶ In contrast to SIMD



# ModemX Architecture - Concurrent operation

- ▶ Operation of multiple standards / waveforms
- ▶ One SSQ per Standard
- ▶ All resources are divided between standards
  - ▶ Orthogonal sets
  - ▶ No constraints/ bottlenecks between sets
  - ▶ Designer may choose to share resources
- ▶ New standards/waveforms can be loaded without affecting the currently active ones.



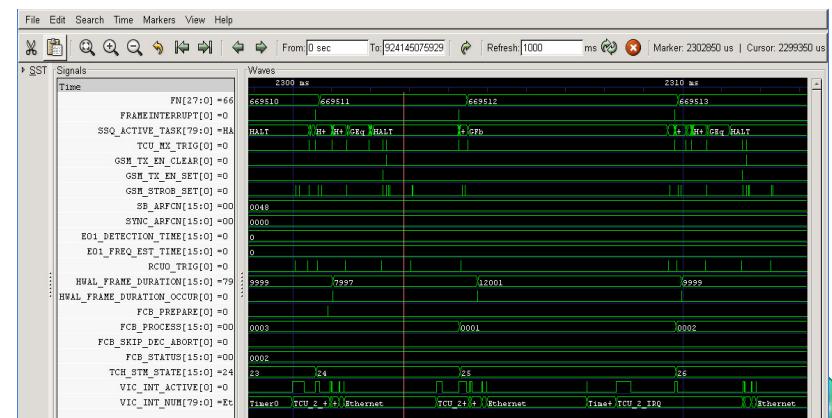
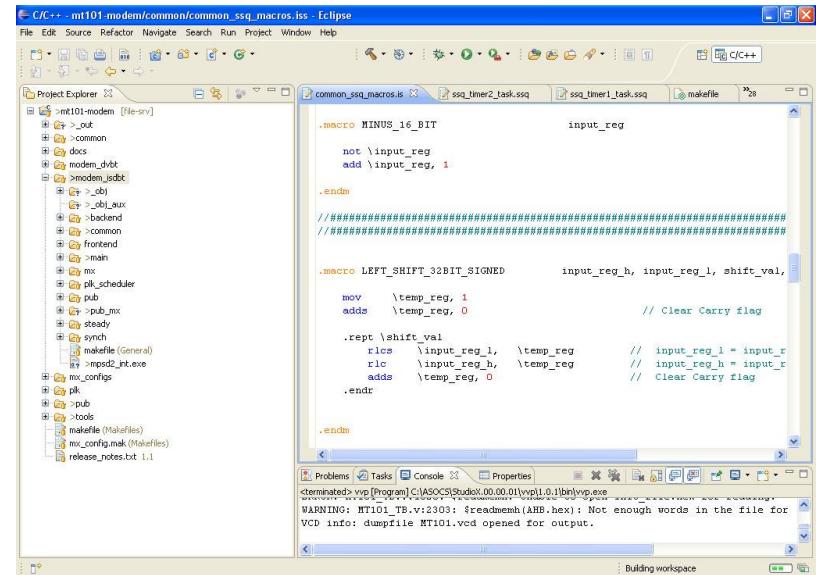
# ModemX Development Tools

## ► Main Challenges

- ▶ Real time code development in a **Heterogeneous Many Core** system
  - ▶ Programming for **Concurrent Operation**
  - ▶ ModemX Architecture abstraction

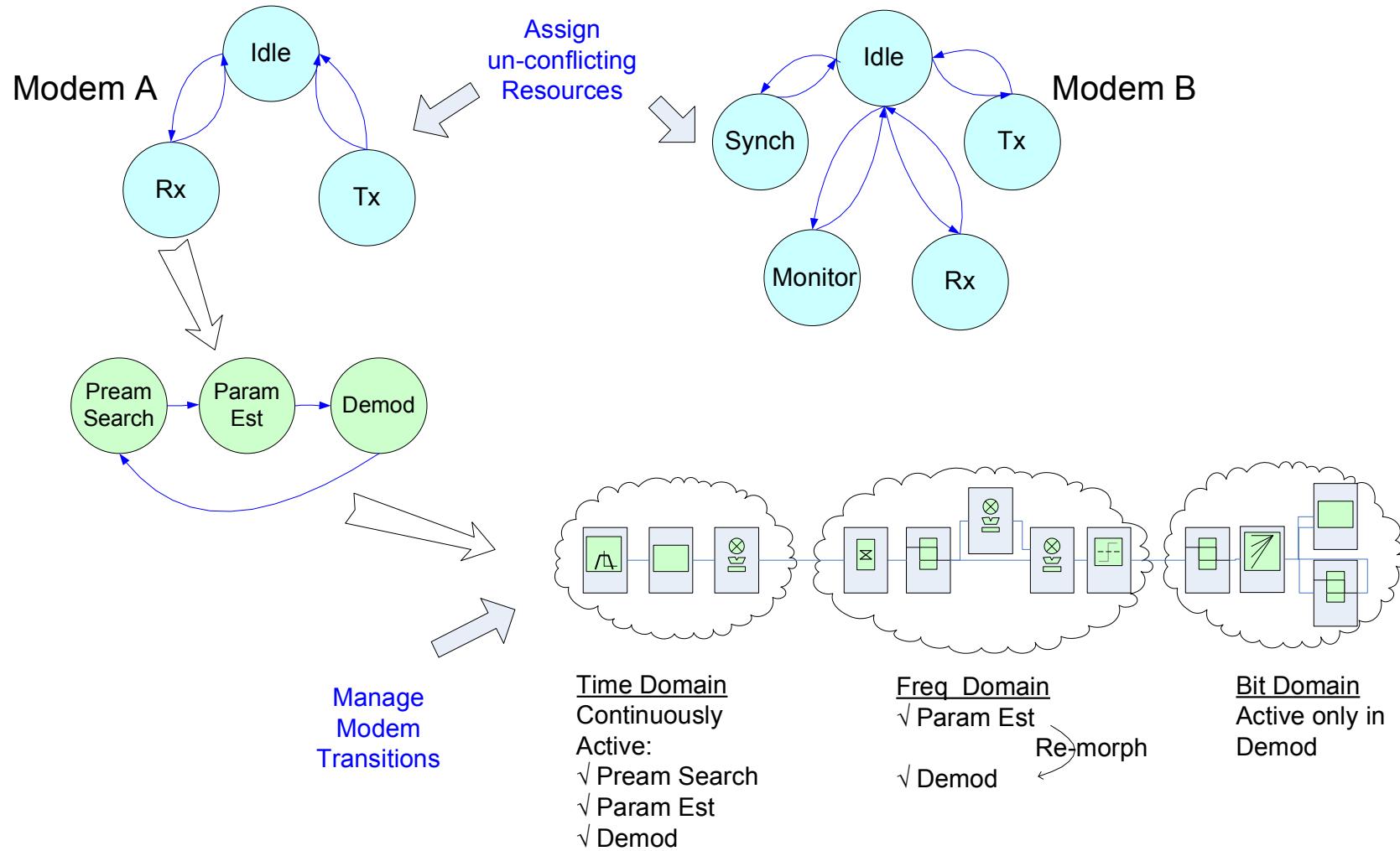
## ► Solution

- ▶ StudioX: Integrated Development Environment.
  - ▶ MPSD: Multi Protocol System Designer.
  - ▶ SSQ/APU Compilers and Assemblers.
  - ▶ Real-time debugging and monitoring tools.
  - ▶ Function libraries for frequently used algorithms.



ASOCS

# MPSD problem statement



# ModemX Architecture - Key points

- ▶ Significant Processing power
  - ▶ Example LTE (Cat 4 UE)
    - ▶ 100 real Multiply accumulate / cycle
    - ▶ 50 complex memory transfers per cycle
    - ▶ Available for multiple operations across the design
    - ▶ Elevates traditional SIMD limitations.
- ▶ Power/Area efficiency
  - ▶ Data path approach provides near dedicated H/W power consumption
  - ▶ Thin control layer
- ▶ Scalability
  - ▶ Resources are readily tuned to requirements
  - ▶ Same platforms for
- ▶ One Stop Shop for All processing requirements
  - ▶ In contrast to DSP + Accelerator suites



# Agenda

- ▶ Introduction
- ▶ ModemX Architecture
- ▶ Application Examples
- ▶ Summary



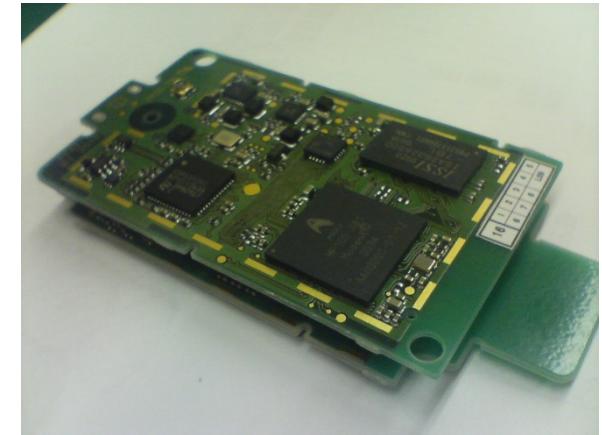
# ModemX Applications

- ▶ Mobile applications
- ▶ Digital TV
- ▶ Aerospace
- ▶ Infrastructure and Cloud - RAN



# Mobile Applications

- ▶ Field proven applications developed using ModemX technology
- ▶ Implemented on MP100 baseband processor chip:
  - ▶ GSM/EDGE
  - ▶ TD-SCDMA
  - ▶ CMMB (Chinese mobile Digital TV standard)
  - ▶ WiFi 802.11g
- ▶ Diverse requirements and technologies
  - ▶ Bandwidth from 200KHz to 20MHz.
  - ▶ Bit rates 240Kb/s – 54 Mb/s
  - ▶ Plethora of modulation scheme and demodulation techniques
    - ▶ Soft output trellis equalizers (GSM/EDGE)
    - ▶ Successive Interference Cancelation joint Detection (TD-SCDMA)
    - ▶ OFDM-11g variant: short symbols and burst, fast acquisition time.
    - ▶ OFDM-CMMB variant: long symbols, scattered pilots.
- ▶ Concurrent operation
  - ▶ GSM/ WiFi operation



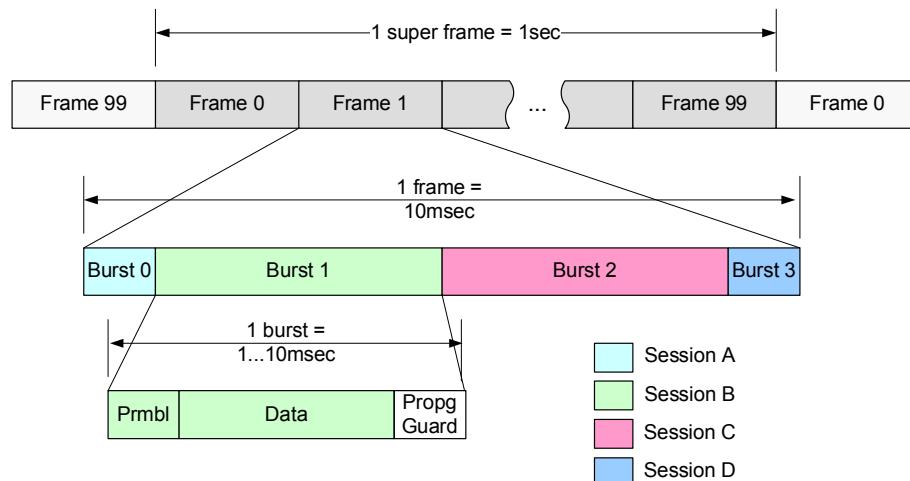
# Digital TV applications

- ▶ Terrestrial/Satellite Digital TV is an excellent playground for SDR:
- ▶ Various regional standards and modulation technologies.
  - ▶ DVB-T/T2 (Europe) ISDB (Japan) : OFDM
  - ▶ DVB-S/S2 (Europe) Satellite: Single carrier
  - ▶ ATSC- ATSC-M/H (USA): Terrestrial, single carrier
  - ▶ DTMB- (China) TDS-OFDM
- ▶ Receiver configuration and antenna diversity options
- ▶ ASOCS MT101
  - ▶ ModemX based IP for digital TV



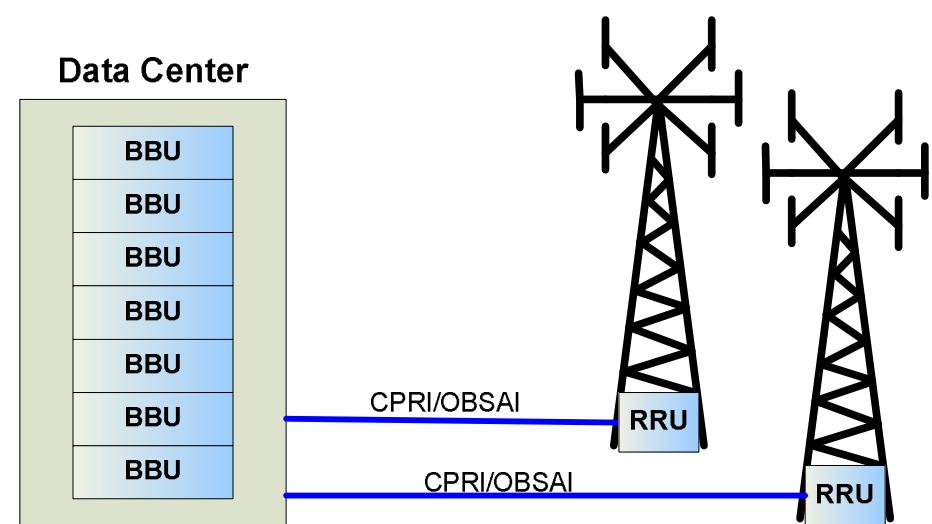
# Aero space application

- ▶ Developed per requirement of leading Aerospace company
- ▶ Two Concurrent Modems, 4MHz, 10Mb/s
- ▶ Coded OFDM over frequency hopping
- ▶ Small form factor module: 11x6x2.5 cm
- ▶ True SDR with a 400MHz- 4 GHz RF transceiver.



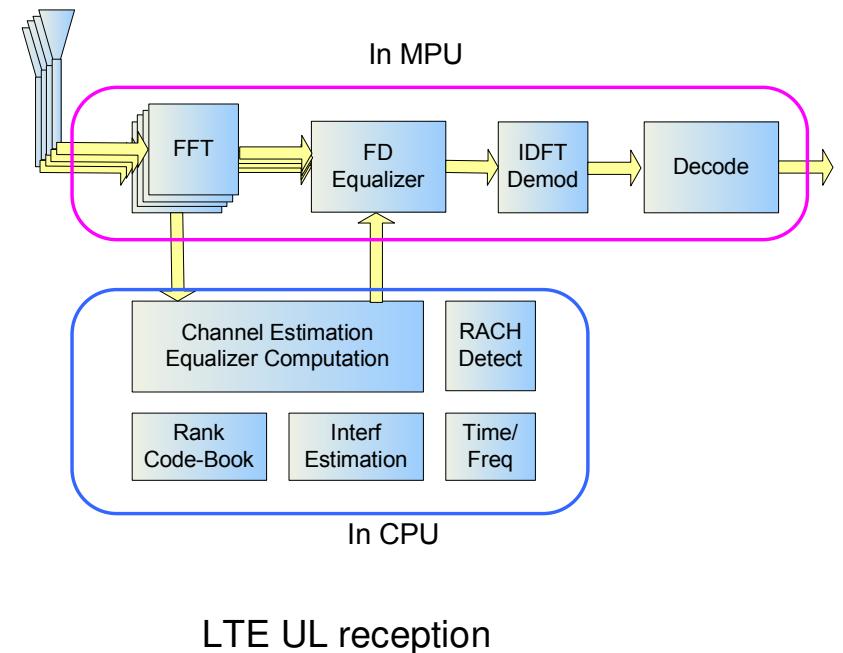
# Cloud RAN applications

- ▶ Cloud RAN Background:
  - ▶ Entire C-RAN processing is delegated to the ‘cloud’.
  - ▶ Implemented in large data centers.
  - ▶ On general purpose servers (x86)
- ▶ CAPEX reduction
  - ▶ economics of scale, GP
- ▶ OPEX reduction
  - ▶ lower power consumption
- ▶ Facilitates novel techniques:
  - ▶ Cooperative Multipoint (CoMP) operation



# ModemX in cloud RAN

- ▶ C-RAN implementation on x86 very challenging
  - ▶ High bandwidth/strict latency requirements
  - ▶ Processing tasks which are not in x86 architecture
    - ▶ E.g. Turbo decoding
    - ▶ Data transfers bottlenecks
    - ▶ Power efficiency for vector operations
- ▶ Proposed approach:
  - ▶ CPU off loading to Modem Processing unit (MPU)
  - ▶ Implemented using ModemX technology
- ▶ Requirements
  - ▶ Same solution for 2G,3G 4G
  - ▶ Support of complex and irregular algorithm
  - ▶ Easy to change and modify data path architecture
  - ▶ On the fly re-configurability
  - ▶ Power Efficiency



# Agenda

- ▶ Introduction
- ▶ ModemX Architecture
- ▶ Application Examples
- ▶ Summary



# Summary

- ▶ Presented ModemX architecture and applications
- ▶ New concept and architecture
- ▶ Facilitates true concurrent operation
- ▶ Powerful and flexible
- ▶ Scalable solution, supports a wide range of applications.
- ▶ Mobile applications
  - ▶ Power and size competitive with dedicated H/W solutions.
- ▶ Infrastructure applications
  - ▶ High processing for infra structure applications
  - ▶ Power consumption well below other SDR solutions.





ASOCS



# Thank you

*making wireless convergence TRANSPARENT*

*making wireless convergence TRANSPARENT*