

Reconfigurable Continuous-Time Delta-Sigma Analog-to-Digital Converters for Software-Defined and Multi-Standard Radios

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Abstract—Emerging wireless standards are continuously providing higher data rate and increased amount of flexibility. The recent trend in modern wireless transceivers is towards multi-standard radio solutions that can support a varied range of wireless voice and data transfer services, and Software Defined Radios (SDR). In order to support multi-mode radio operation and switching between standards, reconfigurable hardware architectures have become essential. Moreover, the transceivers should be energy scalable so maximize battery life of the the hand-held radios. This necessitates analog-to-digital converters (ADCs) with reconfigurable bandwidth from 200 kHz up to 160 MHz and with up to 14-bits of resolution. Continuous-time delta-sigma (CT- $\Delta\Sigma$) ADCs have recently been explored for wideband data conversion in wireless receivers due to much lower power consumption and inherent anti-alias filtering (AAF). Also, Delta-Sigma ADCs scale well with CMOS technology as they predominantly employ digital circuitry for achieving high dynamic range. Thus, a reconfigurable and digitally programmable CT- $\Delta\Sigma$ ADC is the logical choice for data conversion in multi-standard radios. We propose a digitally reconfigurable CT- $\Delta\Sigma$ ADC architecture with an ‘constant-capacitance scaled’ loop-filter and programmable clocking to allow multi-standard operation. The proposed constant-C scaled CT- $\Delta\Sigma$ ADC employs a 4th order noise-shaping with a programmable multi-bit quantizer to achieve higher performance, improved stability and energy scalability. The loop filter is implemented using digitally programmable, feedforward compensated Active-RC integrators for high linearity and wider swing. The proposed architecture will enable design of ADC with digitally programmable conversion bandwidth from 312 kHz to 32 MHz with 40 modes.

Index Terms—Analog-digital (A/D) conversion, cognitive radio (CR), continuous-time (CT), delta-sigma ($\Delta\Sigma$), multi-standard radios, software-defined radios (SDR).

I. INTRODUCTION

As the next-generation wireless standards emerge enabling yet higher data rate and increased amount of flexibility, reconfigurable hardware architectures have been essential. The trend in modern wireless transceivers is towards multi-standard radio solutions that can support technologies like 4G/LTE cellular, Bluetooth, WLAN (802.11 a/b/g/n/ac), WiMAX, Software Defined Radio (SDR) etc. This requires analog-to-digital converters (ADCs) with reconfigurable bandwidth from 200 kHz to upto 160 MHz and with up to 14-bits of resolution. Continuous-time delta-sigma (CT- $\Delta\Sigma$) ADCs have recently been explored for wideband data conversion in wireless receivers due to much lower power consumption and inherent

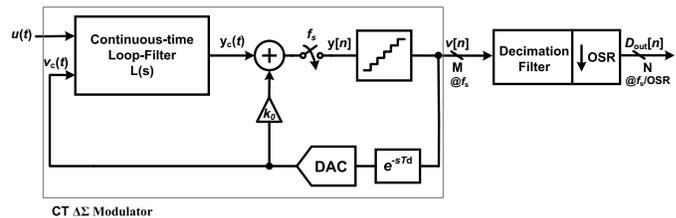


Figure 1. Block diagram of a Continuous-time Delta-Sigma ADC.

anti-alias filtering (AAF). The CT- $\Delta\Sigma$ modulator (see Fig. 1) comprises of a continuous-time (CT) loop-filter to provide high gain in the signal bandwidth, a low-resolution ADC (quantizer) and feedback DACs, and supporting digital logic for DAC linearization and time-constant tuning. The CT- $\Delta\Sigma$ modulator is followed by a digital decimation filter to filter the out-of band noise and thus achieving the required high-resolution.

Delta-Sigma ADCs scale well with CMOS technology as they predominantly employ digital circuitry for achieving high dynamic range. Thus, a reconfigurable and digitally programmable CT- $\Delta\Sigma$ ADC is the logical choice for data conversion in multi-standard radios. However, for a fixed dynamic range and assured stability of a CT- $\Delta\Sigma$ ADC, the characteristics of its noise transfer function (NTF) and signal-transfer function (STF) are extremely important. The out-of-band gain (OBG) in the NTF response allows a delicate trade-off between the performance, stability and the jitter noise sensitivity of the CT- $\Delta\Sigma$ modulator employed in the ADC. Thus, it is essential that the shape of the NTF is preserved for all the programmable modes of the ADC to ensure consistent performance and stability. Moreover, the reconfigurable ADC should be energy scalable, i.e. should able to scale down power consumption for lower performance modes. We propose a digitally reconfigurable CT- $\Delta\Sigma$ ADC with an ‘constant-capacitance scaled’ loop-filter and programmable clocking and oversampling ratio (OSR) to allow multi-standard operation with energy scalability. The proposed constant-C scaled CT- $\Delta\Sigma$ ADC architecture employs a 4th order loop-filter with a 3-bit quantizer to achieve higher performance and improved stability at a modest power budget. Simultaneous OSR and sample-rate (f_s) scaling is incorporated to allow sufficient

range of bandwidth and dynamic range to accommodate desired modes of operation. The loop filter is implemented with digitally programmable, feedforward compensated Active-RC blocks for high linearity and wider swing. The proposed architecture will enable design of ADC with digitally programmable conversion bandwidth from 312 kHz to 32 MHz with 40 modes. The frequency scaling will be achieved with consistent dynamic range performance, guaranteed stability and expected 40 mW power consumption in 130-nm CMOS technology. Also, the STF in the proposed CT- $\Delta\Sigma$ architecture also inherently realizes the programmable AAF.

The architecture and implementation details of the reconfigurable CT- $\Delta\Sigma$ ADC, employing a digitally programmable loop-filter and a 3-bit Flash quantizer, form the discussion of rest of the paper. Section II discussed the system-level architecture of the reconfigurable CT- $\Delta\Sigma$ ADC, and the application of constant- C scaling for achieving a robust design. Section III discusses the details of transistor-level circuit design in progress. Section IV presents the behavioral simulation results of the proposed modulator. Finally, section V draws conclusions about the work.

II. RECONFIGURABLE CT- $\Delta\Sigma$ ARCHITECTURE

In order to accommodate a wide range of bandwidth requirements in a multi-standard CT- $\Delta\Sigma$ ADC, a flexible architecture is required. Not only the required bandwidth should change over a range of two decades, but the ADC should also support the dynamic range (DR) and bit resolution (ENOB) by the supported standard and also provide sufficient alias filtering before the sampler. Taking a step further, ADC employed in a SDR should be able to provide a selectable DR and power trade-off for each of the bandwidth settings. Moreover, ADCs employed in SDR should be able to accommodate new standards in future with more complex modulation schemes. Several possibilities have been presented earlier which employ: (1) an *independent* fixed-frequency clock, and (2) an independent flexible-frequency clock [1]. At the same time the loop-filter needs to be scalable in order to cover the supported conversion bandwidths. A fixed modulator clock at the maximum frequency precludes a separate PLL for the ADC, and leads to smaller R and C values leading to a small layout size. However, such architectures do not result in power efficiency for lower bandwidth modes. Also, the digital design is complicated due to a larger sample-rate conversion in the decimation filter.

An independent flexible clock based modulator architecture results in power efficient analog and digital blocks at the cost of an additional wide-range clock generating PLL with sufficiently low phase-noise. The downside is that extra coefficient sets are needed for the loop-filter and the coefficients for the lower frequency settings lead to larger R and C values and hence a larger layout area. Recently, design of flexible CT- $\Delta\Sigma$ modulators have received wide attention [2], [3], [4], [5], [1] as a step towards developing portable multimode receivers. The maximum reported bandwidth setting for these modulators is 10 MHz with 11 bit resolution (WLAN mode). The preferred architecture has been a single-bit quantizer with a minimum

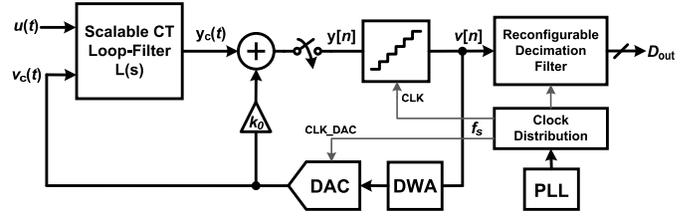


Figure 2. Block diagram for a reconfigurable CT- $\Delta\Sigma$ ADC with programmable clock distribution.

Table I
SPECIFICATIONS FOR WIRELESS COMMUNICATIONS AND SOFTWARE-DEFINED RADIO IMPLEMENTATIONS[3], [8]

Standard	Signal BW (MHz)	Dynamic Range
GSM	0.2	85 dB
UMTS (WCDMA)	2-4	74 dB
DVB-H	7.6	54-63.5 dB
Bluetooth	1	80 dB
WLAN 802.11a/g	20, 22	62-86 dB
WLAN 802.11b	22	50 dB
WLAN 802.11n	40	62-86 dB
WLAN 802.11ac	40, 80, 160	>68 dB
WiMAX 802.16	1.25-20	55-63 dB
GPS	2	62 dB
USRP2[6]	≥ 100	62-86 dB

OSR of 32 and with SCR feedback with other techniques for reducing power consumption [5].

However, the evolving SDR platforms (e.g. USRP2) require ADC resolution up to 14-16 bits and bandwidths over 100 MHz [6]. Recent CT- $\Delta\Sigma$ show that CMOS scaling enables higher sampling rates (1 GHz) resulting in conversion bandwidths traditionally offered by Pipelined ADCs, i.e. 125 MHz (OSR=16) with 70 dB dynamic range in 45 nm CMOS[7]. To satisfy the increased dynamic range and low-OSR requirements for flexible SDRs, a single-bit CT- $\Delta\Sigma$ will not be sufficient. It is evident that the single-bit $\Delta\Sigma$ modulators are bound to employ a lower out-of-band gain (OBG) of 1.5 to guarantee modulator stability, especially for third- or higher order modulators. This poses a restriction on the maximum achievable quantization noise suppression in the baseband. Even though single-bit CT- $\Delta\Sigma$ offer simple topology, a high linear feedback DAC and lower power consumption, multi-bit CT- $\Delta\Sigma$ are necessary for higher performance, especially for low-OSR designs.

In order to realize a reconfigurable CT- $\Delta\Sigma$ with higher performance and wider bandwidths, we propose an energy-scalable architecture employing a combination of frequency as well as OSR scaling. Fig. 2 shows block diagram of a flexible CT- $\Delta\Sigma$ ADC. A choice of flexible clock rate and flexible bandwidth may result in a large number of loop-filter coefficient settings. The subsequent sections describe methods of systematic design of scalable CT- $\Delta\Sigma$ which result in simpler loop-filter coefficient matrix.

A fully flexible CT- $\Delta\Sigma$ can potentially employ flexibility on all the components - loop-filter, quantizer and feedback DACs. Since a multi-bit quantizer is employed, the NTF can use an OBG of 3 for aggressive noise shaping. A CT loop-filter can have flexibility to select the number of inte-

Table II
BANDWIDTHS (MHZ) AND IDEAL SQNR (DB) ACHIEVED BY
SIMULTANEOUS CLOCK RATE AND OSR SCALING

f_s (MHz)/OSR	10	16	32	64	128
640	32	20	10	5	2.5
560	28	17.5	8.75	4.38	2.187
480	24	15	7.5	3.75	1.875
400	20	12.5	6.25	3.13	1.562
320	16	10	5	2.5	1.25
240	12	7.5	3.75	1.88	0.937
160	8	5	2.5	1.25	0.625
80	4	2.5	1.25	0.625	0.3125

(a) Scalable bandwidths (MHz) for different modes

N_0 /OSR	8	16	32	64	128
3-bits	71.7	98.7	131.4	164.7	143
2-bits	53.0	74.0	105.9	138.9	127

(b) Ideal SQNR (dB) for each OSR mode and quantizer resolution (N_0)

grators, state-space interconnections and coefficients ($K = [k_0 \ k_1 \ k_2 \ k_3 \ k_4]$). However, adding more flexibility results in a larger dimension coefficient matrix for each of the settings. A flexible quantizer can implement programmable resolution by selectively disabling comparators or by employing selective multi-step quantization[9]. But for lower quantizer resolution, the OBG needs to be reduced and thus increasing the complexity of the loop-filter coefficient matrix. A programmable feedback DAC shape can potentially be employed for programmable jitter reduction and alias filtering, but the resulting benefit in performance doesn't justify the increase in complexity.

The proposed fourth-order reconfigurable CT- $\Delta\Sigma$ employs simultaneous sampling frequency and OSR scaling to achieve fine granularity in bandwidth and DR selection. Behavioral modeling is performed for the modulator design in a 130-nm CMOS process. For each sample rate (f_s) setting, five (2-bit selectable) OSR modes are available. For the lower OSR modes, a 3-bit quantizer is employed and while for OSRs of 64 and 128, the quantizer is used in 2-bit mode for power reduction. As shown in Table II, for each bandwidth selection, multiple (f_s , OSR) settings are possible providing a trade-off between dynamic range and power consumption.

A. Loop-Filter OSR-Scaling

The various OSR -modes for any sample rate (f_s) set the bandwidth vs dynamic range tradeoff as shown in Fig. 3. For each of the OSR -modes, the optimum $NTF(z)$ zeros are obtained by using the *synthesizeNTF* function in the $\Delta\Sigma$ toolbox[10]. The obtained $NTF(z)$ for each of the OSR -modes, are mapped to the loop-filter topology by using the design-centering method explained in Section II-C, and the loop-filter coefficients $K = [k_0 \ k_1 \ k_2 \ k_3 \ k_4]$ are determined. From these coefficients, the R-C time-constants are determined after dynamic range scaling of the modulator for the highest sampling rate (f_s). The OSR -scaling is implemented by using a digitally programmable capacitor bank, while a resistance bank is used for f_s -scaling described next. The resistors (R_{z1} and R_{z2}), forming the resonator need to be switched for OSR -scaling. Thus, the proposed architecture provides the flexibility of choosing the optimum (f_s , OSR)

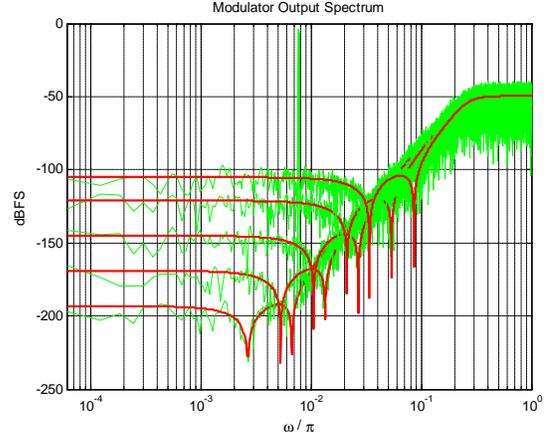


Figure 3. Fourth-order noise-shaping for each of the OSR modes shown in Table II. Here, the sampling frequency is normalized to 1 Hz and a 3-bit quantizer is used.

by decoupling the resistance and capacitor banks in the RC time constants.

B. Loop-Filter Time-Scaling

Time-scaling of the CT- $\Delta\Sigma$ modulator is performed to allow different f_s -modes without degrading the noise-shaping performance. With a change in f_s , the $NTF(e^{j\omega})$ should be invariant, while implies that the open loop response ($l[n]$) of the modulator shouldn't change with f_s -scaling (i.e. $f_s \rightarrow \alpha f_s$ and $T_s \rightarrow T_s/\alpha$). In order to maintain consistent f_s -scaling of the modulator, a constant excess-loop delay (ELD) of 0.5 is employed for each of the f_s -modes. This provides half clock period for the quantizer and the DAC mismatch noise-shaping (DWA) logic. The delay of the feedback DAC must be minimized to ensure consistency in f_s -scaling of the DAC pulse shape, $p(t) \rightarrow p(\alpha t)$. For the loop-filter impulse response, $l_c(t)$, we have

$$l[n] = (l_c(t) \otimes p(t))|_{t=nT_s} \quad (1)$$

which implies that the loop-filter should 'time-scale' as

$$f_s \rightarrow \alpha f_s \Rightarrow l_c(t) \rightarrow l_c(\alpha t) \quad (2)$$

to keep the open-loop response $l[n]$ invariant. In Laplace domain, time-scaling translates to

$$L_c(s) \rightarrow L_c\left(\frac{s}{\alpha}\right) \quad (3)$$

Time-scaling methods for CT filters has been previously developed for achieving wide-range programmability with constant dynamic range [11]. It has been demonstrated that constant- C scaling preserves the frequency response of the CT filter with time-scaling by ensuring that all the poles and zeros in the network scale by the same factor (α). Constant- C scaling states that all the conductances (G) and transconductances (G_m) should scale by α while all the capacitances (including the parasitic capacitances) in the network should stay constant. Intuitively, since the poles and zeros for a network comprised of conductances G_i and capacitors C_j is of the type $f(\frac{G_i}{C_j})$, linear scaling of frequency response can only be

achieved if C 's are kept constant while G 's scale linearly. Also, with constant- C scaling, the output noise power of the filter, worst-case distortion, maximum input signal level and the dynamic range stay independent of the scaling factor.

Thus, a loop-filter in a CT- $\Delta\Sigma$ employing constant- C scaling will guarantee a fixed dynamic range, maximum stable amplitude (MSA) and stability for each of the OSR settings. Also, the loop-filter coefficients will scale by α for all OSR modes and thus simplifying the switched RC matrix. If the loop-filter doesn't constant- C scale, then loop-filter coefficients for each of the (f_s, OSR) modes will be distinct and result in a complicated RC switching matrix. Figure 4 shows a constant- C scaled loop-filter designed using digitally programmable integrators with constant node capacitances. Active-RC loop-filter topologies are preferred over the $g_m - C$ implementation as the former provides higher linearity desired in high-performance ADCs for the same power budget. Further, active-RC topologies with two-stage opamp has been shown to provide higher linearity than single-stage OTAs [12]. Further, the two-stage opamps are designed with feedforward compensation to alleviate slew-rate limitation. The loop-filter scaling is achieved by digitally selecting the g_m -stages and the programmable resistor. For a particular OSR setting, the integrating capacitance is kept constant. The transistor-level circuit details for the loop-filter are provided in Section III. Active summation of weighted integrator states

$$y = \mathbf{K}^T \begin{bmatrix} -v_c \\ \mathbf{x} \end{bmatrix} = -k_0 v_c + \sum_{i=1}^M k_i x_i \quad (4)$$

is performed using the capacitors (C_{11}, C_{21}) and R_4 to avoid an additional power-hungry opamp for summation. Here, $\mathbf{x} = [x_1 \ x_2 \ \dots \ x_M]$ are the modulator states, M is the order of the modulator and v_c is the continuous-time feedback DAC output.

The preservation of the loop-filter response when using constant- C scaling also preserves the jitter transfer properties of the CT- $\Delta\Sigma$ modulator as well as the signal-transfer function (STF) response for all the modes. The resistor bank implementation is discussed in Section III-B.

C. Systematic Design

The integrators in the loop-filter are implemented using two-stage opamps. Feedforward compensated opamps have been preferred for their superior slew performance [13]. In a feed-forward loop-filter topology, the first integrator in the modulator processes the maximum signal content and sets the linearity and noise for the overall ADC. Thus this opamp is designed with higher performance i.e. larger unity-gain frequency (f_{un}), sufficient DC gain and high slew-rate performance. Thus the first opamp consumes a larger share of power budget in the loop-filter. The opamp performance requirements usually reduce as we go towards the quantizer. The fourth opamp needs better linearity as it also acts as the summer. As a designer, it is important to optimize the opamp power consumption for the given performance by minimizing the f_{un} , while meeting the ADC performance requirements.

Since the integrator is implemented using feedforward two-stage opamps, each with two pole and a LHP zero

$$A(s) = A_o \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right)} \quad (5)$$

the resulting integrator response is given by a third-order transfer-function, $I(s)$, as opposed to $\frac{\omega_I}{s}$ for an ideal integrator.

Finite DC gain and unity-gain frequency (f_{un}) of the opamps impairs the characteristics of the loop-filter and thus modifies the resulting NTF [14]. Conventionally, the feed-forward loop-filter coefficients $K = [k_0 \ k_1 \ k_2 \ k_3 \ k_4]$, are obtained by fitting the impulse response of the desired discrete-time loop filter given by

$$L_d(z) = 1 - \frac{1}{NTF(z)} \quad (6)$$

to the corresponding continuous-time loop-filter ($L_c(s)$). This synthesis can be performed using the `synthesizeNTF_ct` function in the $\Delta\Sigma$ toolbox for a given feedback DAC pulse shape[10]. The `synthesizeNTF_ct` function assumes ideal integrators with a normalized transfer function given by $\frac{1}{s}$. This impulse response fitting method leads to error when applied to the real integrators with finite op-amp DC gain and limited f_{un} . To obtain the desired NTF, either the DC gain and f_{un} of the opamps needs to be increased, resulting in significant increase in the modulator power consumption. Alternatively, the coefficients $K = [k_0 \ k_1 \ k_2 \ k_3 \ k_4]$ can be tuned to compensate for the excess loop-delay due to finite gain and f_{un} of the opamps[14].

The opamp transfer function can be included when curve-fitting loop-filter coefficients, \mathbf{K} , to the open loop-response $l[n]$. However, the finite error in this curve fitting can result in unacceptable closed-loop response, i.e. the $NTF(z)$. Thus the desired closed-loop response should also be involved while determining \mathbf{K} . A systematic design centering method, which involves both $L_d(z)$ and $NTF(z)$ and the linear non-idealities of the integrators, was recently proposed in [15]. Since the relationship between the noise-transfer function, $NTF(z)$, and the discrete-time loop-filter response, $L_d(z)$, is given by 6. This relation (6) is incorporated into the impulse response fitting by using the following curve-fitting criterion [15]

$$[h_0 \ h_1 \ h_2 \ h_3]K = \delta[n] - h[n] \quad (7)$$

Here, $h[n]$ is the discrete-time impulse response of the desired $NTF(z)$ and $h_j[n] = l_j[n] \otimes h[n]$. Also $l_0[n]$, $l_1[n]$, $l_2[n]$ and $l_3[n]$ represent the sampled DAC pulse response at the output of each integrator.

A constant- C scaled loop-filter preserves the design centering when using real opamps by ensuring that all the poles and zeros in the opamp scale linearly with the frequency. Thus binary weighted resistors can be used for scaling the loop-filter time constants with f_s -scaling. If constant- C scaling is not used, then we would need to determine loop-filter coefficients using the systematic design procedure for all (f_s, OSR) modes leading to a complicated R-C switching matrix. Fig. 5 illustrates the simulated NTF responses when

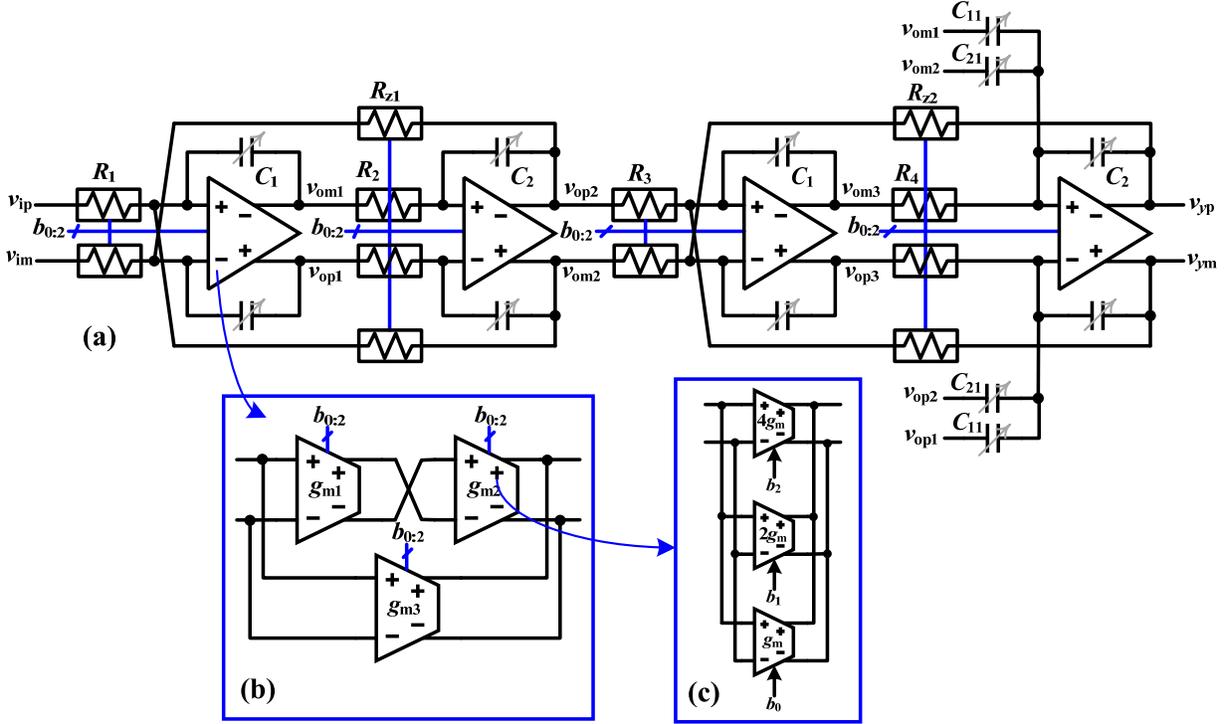


Figure 4. (a) Scalable CT- $\Delta\Sigma$ Loop-filter with constant- C scaling, (b) programmable two-stage opamps used in the loop-filter, (c) a digitally programmable transconductance element.

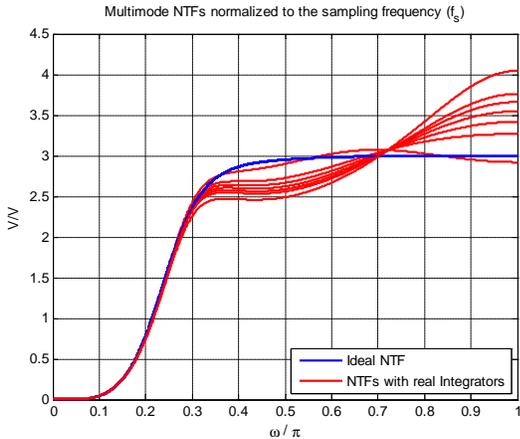


Figure 5. Extracted $|NTF(e^{j\omega})|$ plot for all the f_s -modes when using opamps without constant- C scaling. Here, $OSR = 16$.

constant- C scaling is not used. Systematic design is performed for the highest mode ($b_{0:2}=111$ setting) and the integrators do not maintain constant node capacitances when the g_m 's are scaled down. The opamp model used in the simulation, normalized transfer function given $\frac{2120(1+\frac{s}{6.13})}{(1+\frac{s}{0.1125})(1+\frac{s}{0.1875})}$ at the highest mode setting. Here, we can observe that the NTF shape changes for different f_s - modes leading to higher OBGs. This will deteriorate the modulator performance and may lead to instability.

Fig. 6 shows the simulated noise-transfer functions ($|NTF(e^{j\omega})|$) for all the seven sampling frequency settings when constant- C scaling of the loop-filter is employed. The

behavioral simulation in MATLAB used the models for the digitally programmable opamps described in Sec. III-A. Here, we can observe that the systematic design centering is preserved for all the modes and the OBG is well behaved.

D. Dynamic Range Scaling and Noise

The loop-filter needs to be dynamic range scaled so that the integrator outputs are in the linear region of operation[16]. This is obtained by linear transformation of the loop-filter state-space. Now, for a reconfigurable CT- $\Delta\Sigma$ we may need to perform dynamic range scaling (DRS) for all the modes. However, since constant- C scaling preserves the integrator outputs for all the modes, it is sufficient that DRS is performed for only one f_s -mode. The input-referred thermal noise is dominated by the input resistor (R_1), R_{z1} and the feedback current DAC and will scale proportionally with f_s -scaling. The thermal noise contributes 75% of the in-band noise budget for dithering the $\Delta\Sigma$ modulator[10].

E. R-C Time-constant Tuning

In a nano-CMOS process, the capacitors and resistors can vary by a maximum of $\pm 15\%$ from one die to another. This leads to a maximum loop-filter RC time-constant variation of $\pm 30\%$, leading to faster and slower loops at different process corners. However, the RC time-constant variation on a single die is maximum $\pm 5\%$ and is not a concern. The RC time-constant variation can potentially impact the noise-shaping and jitter performance of the CT- $\Delta\Sigma$ modulator and in some cases render it unstable. This necessitates RC time-constant tuning in the loop-filter. Several methods have been proposed

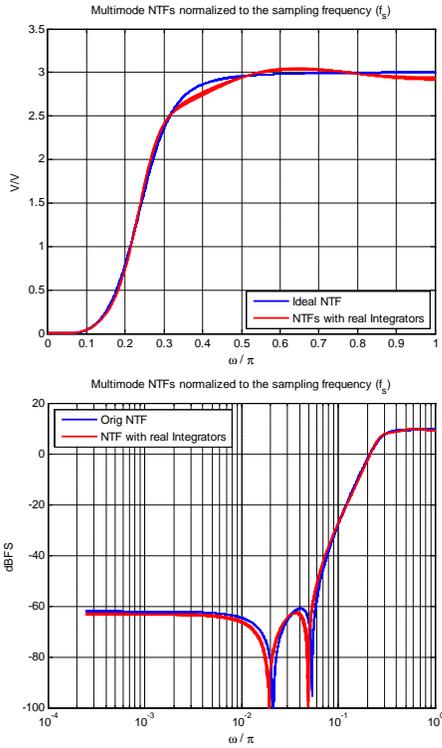


Figure 6. Extracted $|NTF(e^{j\omega})|$ plots (linear and log y-axis) for all the f_s -modes with constant- C scaling of the loop-filter. Here, $OSR = 16$.

in literature for estimating the RC variation on chip and then tuning the loop-filter using a capacitor bank[1]. However, a lucrative method was proposed in [17] for automatic tuning of multi-bit CT- $\Delta\Sigma$ modulators purely in digital domain without adding any extra analog circuitry. This method is based on the observation that the variance ($\sigma_{\delta v}^2$) in the *wiggling* in the modulator output ($\delta v[n] = v[n] - v[n-1]$) is purely governed by the out-of-band characteristics of the modulator. As the normalized loop-filter coefficient (k_p) increase (or decrease) together with RC variation, the OBG increases (or decreases) and hence leading to larger (or smaller) value of $\sigma_{\delta v}^2$. The relation between $\sigma_{\delta v}^2$ and k_p is monotonic and can be implemented as a digital look-up table for tuning of capacitor banks. When constant- C scaling is employed, we only need to store the reference $\sigma_{\delta v}^2$ values in the look-up table for each of the OSR modes. Fig. 7 illustrates the resistor and capacitor banks for a single integrator in the loop-filter. The RC time constant tuning capacitors are merged with the OSR setting capacitor. The capacitor bank design is performed similar to [4].

III. CIRCUIT IMPLEMENTATION

This paper details the behavioral modeling results for the proposed reconfigurable CT- $\Delta\Sigma$ ADC. However, the circuit design details of the work in progress are presented to provide an insight into the transistor-level architecture. The reconfigurable CT- $\Delta\Sigma$ modulator is being implemented in a 130nm CMOS technology with nominal supply voltage (V_{DD}) of 1.2V.

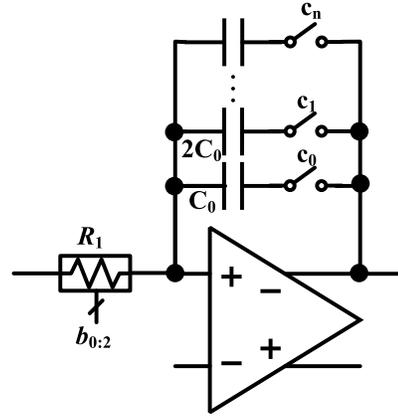


Figure 7. Schematic illustrating the resistor and capacitor bank selection for a single integrator.

A. Operational Amplifier

The schematic and block diagram for the programmable opamp is shown in Fig 8. The programmable opamp comprises of cells with switchable transconductances, controlled by a binary code. The opamp cell employs a two-stage design (g_{m1} and g_{m2}) with feedforward compensation (using g_{m3}). The feedforward path g_{m3} re-uses the current in the second stage to form a class-AB output buffer. Dummy circuits are used for all the transconductances to maintain constant parasitic capacitances on the dominant pole contributing nodes. The common-mode feedback (CMFB) loop is shared by all the opamp cells. The proposed digitally programmable opamp accommodates large integrator output swings in the CT- $\Delta\Sigma$ modulator. The first opamp in the modulator sets the noise and linearity for rest of the loop-filter, and thus larger bias currents are used. The opamp designs are expected to provide an open-loop DC gain of 60dB. The scalable unity-gain frequencies (f_{un}) for the four opamps in the loop-filter are expected to be of the order of $2f_s$, $1.5f_s$, f_s and $1.5f_s$ respectively. The dummy circuits always sink bias current from the supplies (V_{DD} or V_{CM}) and thus the loop-filter consumes constant static power in all modes. Carefully designed MOS capacitors can be switched in and out to emulate constant node capacitances instead of using the dummy circuits. However, this will cause degradation in design robustness. PMOS input stages are used in the opamp cells for reducing input-referred flicker noise.

B. Programmable Resistors

A design strategy similar to [18] is employed to realize the programmable integrating resistors in the loop-filter. This design, shown in Fig. 9, uses smaller size of transistors, biased in deep-triode using higher supply voltages, to reduce parasitic capacitances. A resistance tuning loop is used to maintain a fixed value of unit programmable resistor as shown in Fig. 10. The tuning loop uses a feedback mechanism to refer the value of the unit programmable resistors to a stable resistor, preferably off-chip. If the reference resistor is implemented on chip, the tuning mechanism to compensates for the process

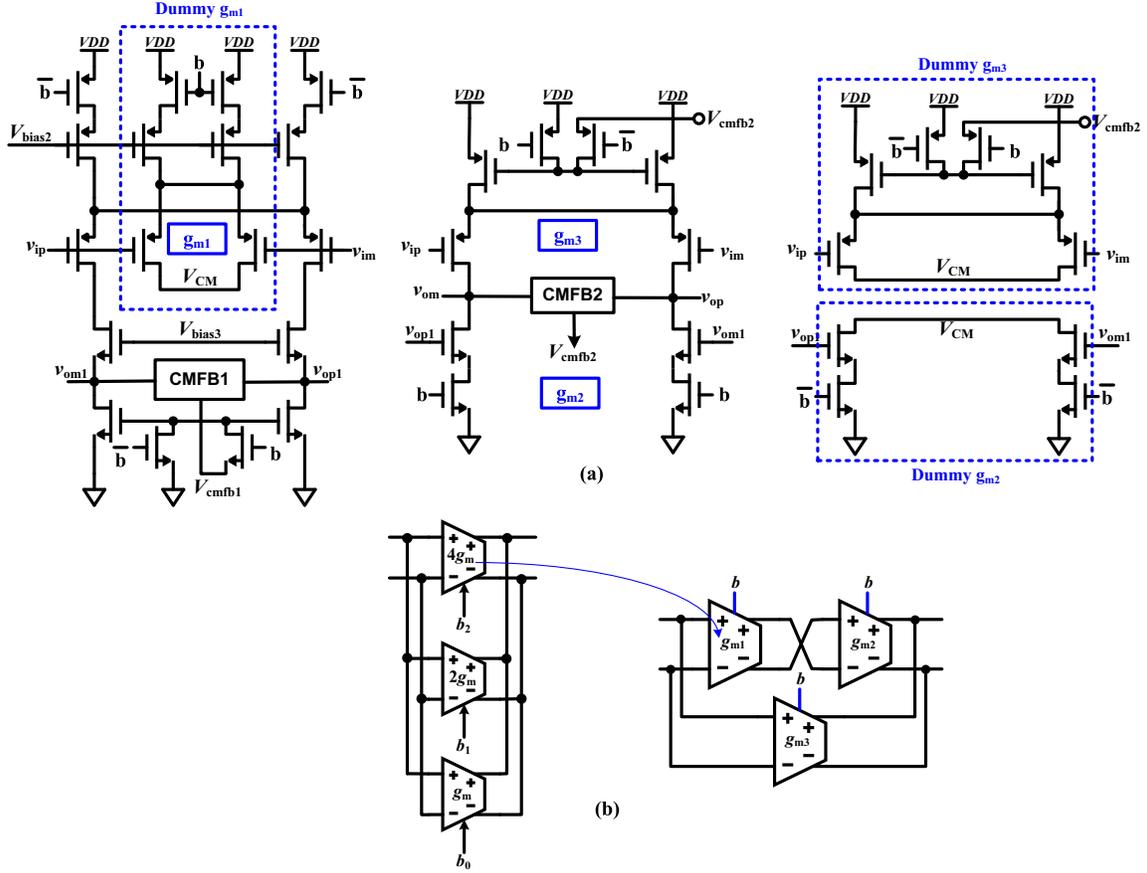


Figure 8. (a) A class-AB opamp cell used in the integrators. (b) 3-bit programmable class-AB opamp formed using the opamp cell.

variations must be included. A higher supply voltage of 1.8V, readily available in communications systems, is employed to maintain high linearity of the switches.

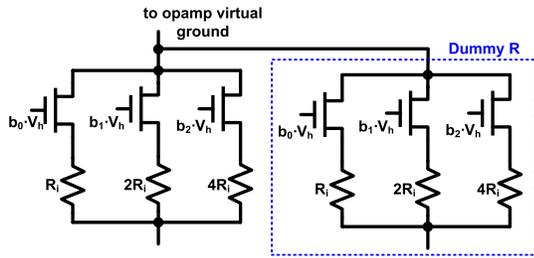


Figure 9. Programmable integrating resistors for f_s -scaling [18]

The programmable resistors forming the resonator loop (R_{z1} and R_{z2}) change with both OSR and f_s scaling and need a finer switchable resistor bank.

C. Quantizer

A 3-bit Flash ADC, shown in Fig. 11, is used to implement the quantizer. The quantizer consists of 7 differential comparators and has a full-scale range of $1.6V_{pp}$ resulting in a step size of 200 mV. The quantizer is designed to meet the specifications at the maximum sampling frequency of 640 MHz and a maximum delay of 475 ps.

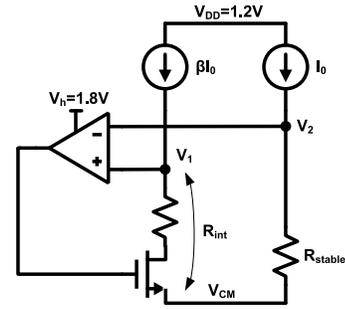


Figure 10. Schematic of the resistor tuning loop[18].

The comparators used in the quantizer, should be able to provide sufficient regenerative gain to mitigate the effects of metastability at high-speed settings. This presents a trade-off between the performance and the static power consumption in the comparators[19]. Fig. 12 shows the high-speed comparator used in the modulator, similar to [20]. Here the first stages uses a differential difference amplifier for reference subtraction. The amplifier is loaded with cross-coupled PMOS latches to provide initial regeneration followed by a clocked latch. The second stage latch provides a large regenerative gain and resolves the outputs to full logic level. The latch is disconnected from the input to avoid kickback noise. A reset phase is used to remove memory in the latches. A trimming

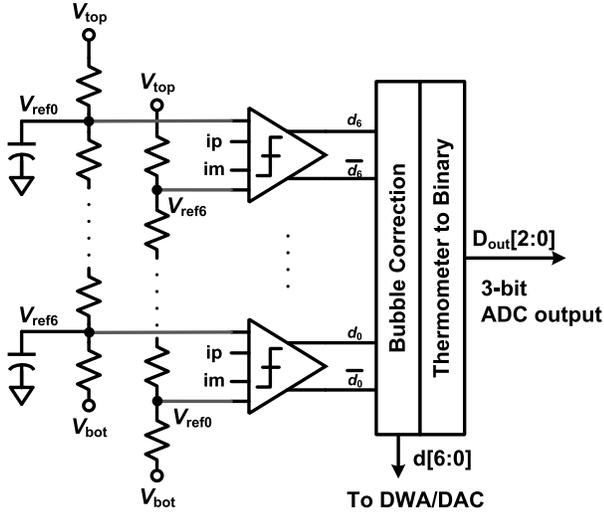


Figure 11. Schematic of the 3-bit Flash quantizer used in the ADC[19].

current DAC is required for the comparators to compensate for the mismatch in the diff-pairs and the tail current sources[20].

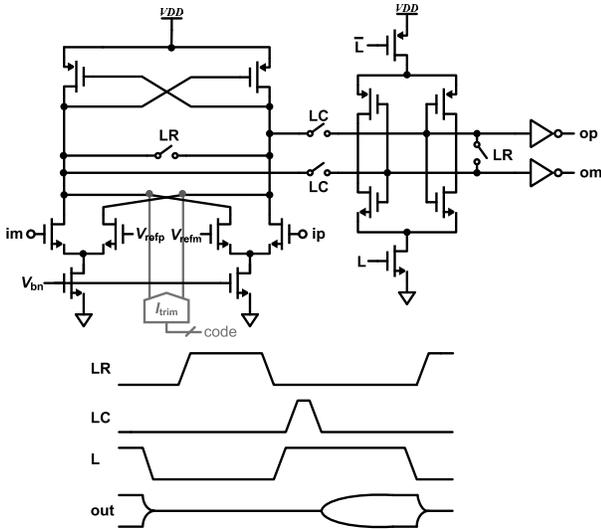


Figure 12. Comparator circuit used in the quantizer with timing diagrams[20].

D. DAC and DWA Logic

Fig. shows the feedback DAC cell used in the modulator [16].

Dynamic weighted averaging (DWA) logic will be used for first-order DAC mismatch noise shaping[16], [19]. The digital logic will be synthesized using standard cells with a maximum delay set by the highest sampling mode (i.e. 300 ps).

IV. SIMULATION RESULTS

The proposed 4th-order CT- $\Delta\Sigma$ ADC architecture was simulated with a schematic containing a combination of transistor-level and behavioral schematic. Transistor-level design of the quantizer and current DACs were used, while the opamps were behaviorally modeled. The simulation model employs digitally

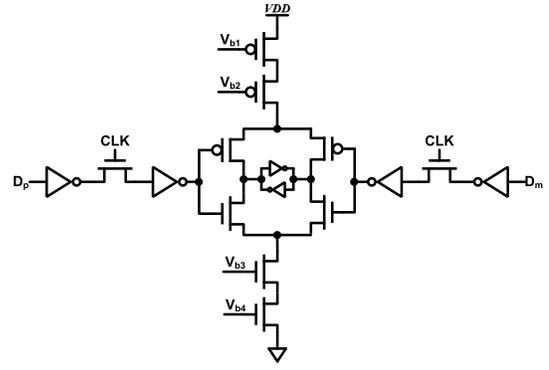


Figure 13. A current DAC unit-cell.

programmable opamps and resistor banks controlled by the digital word $b[2:0]$ for scaling the sampling frequency. The OSR is scaled by selecting a capacitor bank and resonator feedback resistors by digital word $c[2:0]$. In order to evaluate the design methodology, accurate opamp macro model include major non-idealities coded in the Verilog-A macro model. The digitally programmable opamp parasitics were modeled by using capacitance data for transistors in 130-nm CMOS technology. Fig. 14 shows the simulated spectrum results for selected modes. In simulation, a sine wave input with a frequency near the center of the desired bandwidth and an amplitude of 90% of MSA was used. 8192 samples were taken from the modulator output to compute the FFT. Hann window was used for the FFT to minimize the quantization noise leakage in spectrum. The 3-bit control word scales the master clock from the PLL, and the g_m 's of the opamps. The digital word $c[2:0]$ also selects the quantizer resolution for the OSR modes. Using 3-bit quantizer, the peak SQNR of 72.2 dB, 77.8 dB and 60.1 dB were observed for selected WLAN, WiMAX and SDR maximum bandwidth modes respectively. Simulated peak SQNR of 81.7 dB and 79.7 dB was observed for GSM and Bluetooth modes using 2-bit quantizer setting. Table summarizes the simulated performance of the modulator for few standard modes. Power consumption and the Figure of merit (FoM) are not reported as these numbers will be available after the transistor-level implementation is completed.

V. CONCLUSION

A digitally reconfigurable CT- $\Delta\Sigma$ ADC architecture is presented and is being implemented in 130nm CMOS technology. A systematic design method employing constant- C scaling in the loop-filter is presented for robust multi-mode operation. The CT loop-filter preserves its impulse response for a wide range of frequency scaling and thus maintains the stability and performance of the modulator closed-loop. Simultaneous OSR and clock rate scaling is employed to achieve a wide range of bandwidth and dynamic range settings. Carefully designed, programmable feed-forward opamps are used to ensure linear scaling of all the poles and zeros in the response. A 3-bit quantizer is employed for aggressive noise shaping, robust stability and high dynamic range performance required for SDRs. Behavioral simulation results are presented to demonstrate the architecture for few selected standards. In

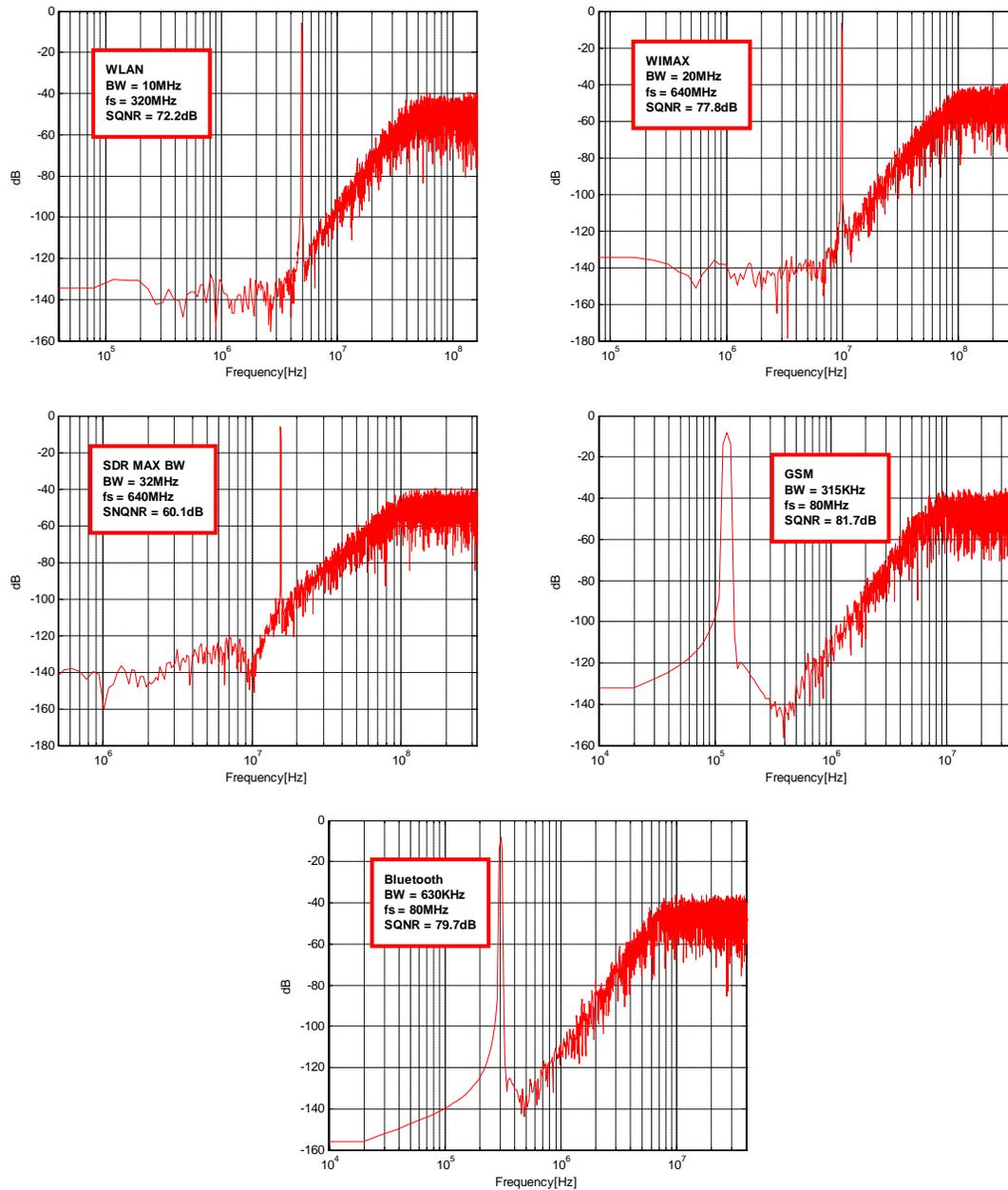


Figure 14. Simulated output spectrum of the reconfigurable CT- $\Delta\Sigma$ modulator for the modes: (a) WLAN ($b_{2:0} = 011$, $c_{2:0} = 001$), (b) WiMAX ($b_{2:0} = 111$, $c_{2:0} = 001$), (c) SDR with maximum bandwidth setting ($b_{2:0} = 111$, $c_{2:0} = 000$), (d) GSM ($b_{2:0} = 000$, $c_{2:0} = 101$), and (e) Bluetooth ($b_{2:0} = 000$, $c_{2:0} = 100$).

future, detailed transistor-level simulations will be performed for the design closure followed by chip fabrication and testing.

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