

Practical Use of Reconfigurable Radios in Air Combat Training Systems

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This paper reviews and analyzes the collaborative efforts of DRS Training & Control Systems, LLC (DRS TCS), DRS Signal Solutions (DRS SS), and SCA Technica to transition a legacy data link to a modern Software Defined Radio (SDR) that will provide interoperability with fielded legacy data links while providing “reconfigurability” to support new more advanced waveforms. Several efforts are described including:

- Extracting the legacy air combat training data link waveform from hardware based data link product.
- Modeling the waveform for rapid prototyping on an SDR platform and porting the waveform to an appropriate target radio.
- Identifying a target SDR radio that will support the SCA, the modeled waveform, and provide the Hardware (HW) infrastructure to support future Joint Tactical Radio Systems (JTRS) airborne networking waveforms planned for air combat training.

The paper will summarize the development challenges and resulting innovations experienced during the development and planned fielding of a backward compatible radio that is reconfigurable to support a future JTRS air combat training waveform.

1.0 INTRODUCTION

The Net-centric Enterprise Solutions for Interoperability (NESI v3.1) best practices (BP 1880, rev 5) stipulates that all future data links which interface tactical systems to the Global Information Grid (GIG), via data link, “**Justify, document, and obtain a waiver for all radio terminal acquisitions that are not JTRS/SCA compliant.**” Many US tactical and strategic data links may be upgraded to JTRS networking standards and Software Communications Architecture (SCA) specifications within the next few years. This has motivated DRS to invest in upgrading their radio links to JTRS/SCA standards as a best practice. The goal of

this DRS internal investment is to develop an advanced SDR data link that is compliant with the JTRS/SCA standard and capable of supporting both legacy Data Link Transceiver (DLT) waveform and other future data link waveform(s) specified by Test and Training Range customers. The expectation of next-generation waveforms is to include a GIG interface for airborne training instrumentation.

This paper reviews the development approach and related challenges associated with identifying the appropriate SDR platform capable of supporting the legacy P5 training data link waveform and future JTRS/SCA waveforms. The legacy P5 DLT provides a real time ad hoc network for air combat training instrumentation systems interfaced to tactical combat aircraft. Each instrumentation system loaded on participant aircraft generates Time-Space-Position Information (TSPI) at rates of up to 10 Hz using the Global Positioning System (GPS) time as a reference. This TPSI data is exchanged among participants, ground stations and control stations using a Time Division Multiple Access (TDMA) network for two-way communication.

The link is required to have 99% of the messages successfully exchanged when two or more ground stations are within Line-Of-Sight (LOS). Messages are relayed between participants. Messages must be successfully exchanged with relative velocities of up to 5,000 ft per second between transmitter and receiver. The maximum permissible Bit Error Rate (BER) is 10^{-6} . The system operates in the upper L-band and S-band radio frequency spectrum. The TDMA network incorporates frequency diversity such that all messages from participants are transmitted twice on two user-selected frequencies. The frequency settings are software controlled and real time agile. Frequency diversity greatly reduces the effects of fading due to multi-path as well as degradation from interference. The TDMA network allows 330 slots per second, each of which can be assigned to any participant or ground station for uplink. Only one participant or ground

station may transmit during a particular slot. Filtered Minimum Shift Keying (MSK) modulation is employed with a transmitted 99% power bandwidth of less than 2.0 MHz. Each slot contains a buffer time, preamble, header and Cyclic Redundancy Check (CRC) code. A Viterbi encoder is used and the data is convolutionally interleaved.

The P5 legacy waveform is implemented using a combination of an Application Specific Integrated Circuit (ASIC) / Field Gate Programmable Gate Array (FPGA) and General Purpose Processor (GPP) in the legacy DLT. DRS TCS plans to replace the legacy DLT with a combined FPGA/GPP only SDR/SCA platform as a best practice goal.

2.0 PORTING THE LEGACY WAVEFORM TO AN APPROPRIATE TARGET RADIO

DRS conducted an extensive trade study in 2009 to identify candidate SDR hardware platforms capable of meeting P5 DLT Size, Weight, and Power (SWaP) requirements; legacy waveform performance; and the potential to host future waveforms. After considering RFP responses from several small form-factor SDR Original Equipment Manufacturer (OEM's), DRS determined the ideal solution, from a Technology Readiness Level (TRL) perspective, was a modern SDR transceiver capable of transmission and reception in the Very High Frequency/ Ultra High Frequency (VHF/UHF) range developed by DRS SS. This new DRS SS SDR technology, called DRS Advanced Radio Transceiver (DART) has significantly decreased SWaP making it more viable to fit within the volume of the targeted product enclosures while providing significant processing power and frequency agility.

A clear benefit of using the DRS SS DART SDR is the open design approach that can take advantage of planned future investment in DRS SS product road maps. The SI-3249 DART, shown in Figure 1 and Figure 2, is a wideband, software-definable VHF/UHF transceiver whose small size, lightweight and low power requirements make it ideal for low SWaP applications.

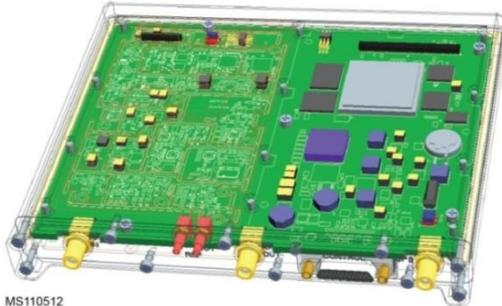


Figure 1. DART Circuit Card (MS110512)

The transceiver is capable of providing 25 MHz of instantaneous bandwidth. The device has separate synthesizers for the receiver and transmitter enabling them to be locked to the same frequency or tuned independently. The DART is equipped with a dedicated internal GPS receiver that generates 1 PPS and 10 MHz reference signals. It also enables synchronization and reference signals to be directly injected into the radio enabling N-channel phase coherent DF or beamforming capabilities.

DRS SS was able to significantly reduce the size and weight by limiting the receiver frequency range to 20 MHz to 3 GHz and setting the transmitter frequency range to 400 MHz to 4400 MHz to reduce the chip count from previous design. Incorporating the DRS SS earlier receiver architecture makes it possible to leverage a proven development environment and the components of proven modem communication waveforms.

DRS SS re-used the modular design of the production Picoceptor platform to develop the DART. DRS utilized the receiver, Analog-to-Digital Converter (ADC) and Virtex-4 FPGA Picoceptor design and added new exciter/transmitter circuitry to achieve a working single board SDR transceiver. The DART platform incorporates one Virtex-4 FPGA. The FPGA can be sized between Virtex-4 FX-12 or Virtex-4 FX-60. The modular HW design of the Picoceptor yielded a rapid, low risk DART development effort. The program very quickly had HW in 10 weeks with initial functionality in less than 16 weeks. The working DART prototype provided a ready reference platform for development, integration, test, and verification efforts achieving a functioning Legacy P5 transmitter within a reduced development cycle.

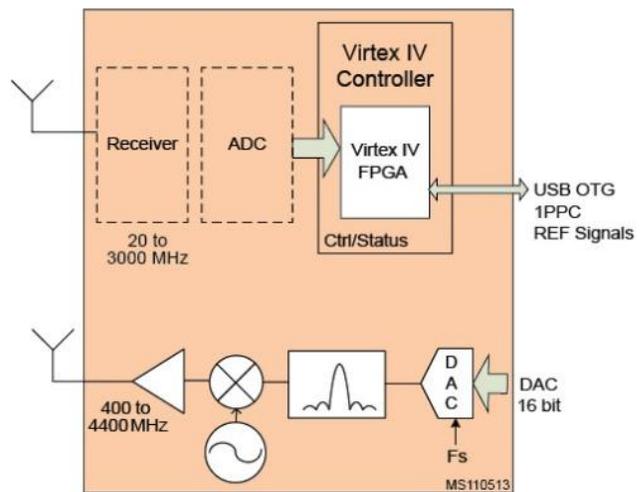


Figure 2. DART Building Blocks (MS110513)

The DART Digital Signal Processing module is based on powerful FPGA technology. The DART is truly an open HW platform that provides an ability to develop and deploy third party signal processing algorithms in the unit. The waveform developer may take advantage of the entire FPGA fabrics (7.2 million gates plus embedded PowerPC cores) and the 32-bit fixed-point general-purpose processor chip for firmware and software development and field deployment.

The system block diagram shown in Figure 3 depicts the progress, to date, on porting the P5 waveform to the internal design structure of the DART. Additionally, it summarizes how the Radio Frequency (RF) processing, digital control, and signal processing building blocks are assembled for ease of reconfigurability.

The green items shown in Figure 3, which include the basic RF and digital HW, represent DART SDR transceiver components that are currently operational portions (transmit side) of a Legacy P5 MSK modem. DRS TCS and DRS SS

have been working collaboratively with this design to implement the existing P5 MSK modem architecture. The receive side portion of this design has been tested in simulations and in legacy DLT HW at the DRS TCS facility in Fort Walton Beach, Florida in early December 2010. The RF hardware and digitizers have been demonstrated to meet the performance requirements needed for the existing P5 DLT.

3.0 DEVELOPMENT FLOW AND ASSOCIATED CHALLENGES

The goal of the SCA given in the 9-Mar-2011 specification is to provide an interoperable infrastructure for the “deployment, management, interconnection, and intercommunication of software components in embedded, distributed-computing communication systems” in SDRs with the additional goals of maximizing software application portability, reusability, and scalability through the use of commercial protocols and products.

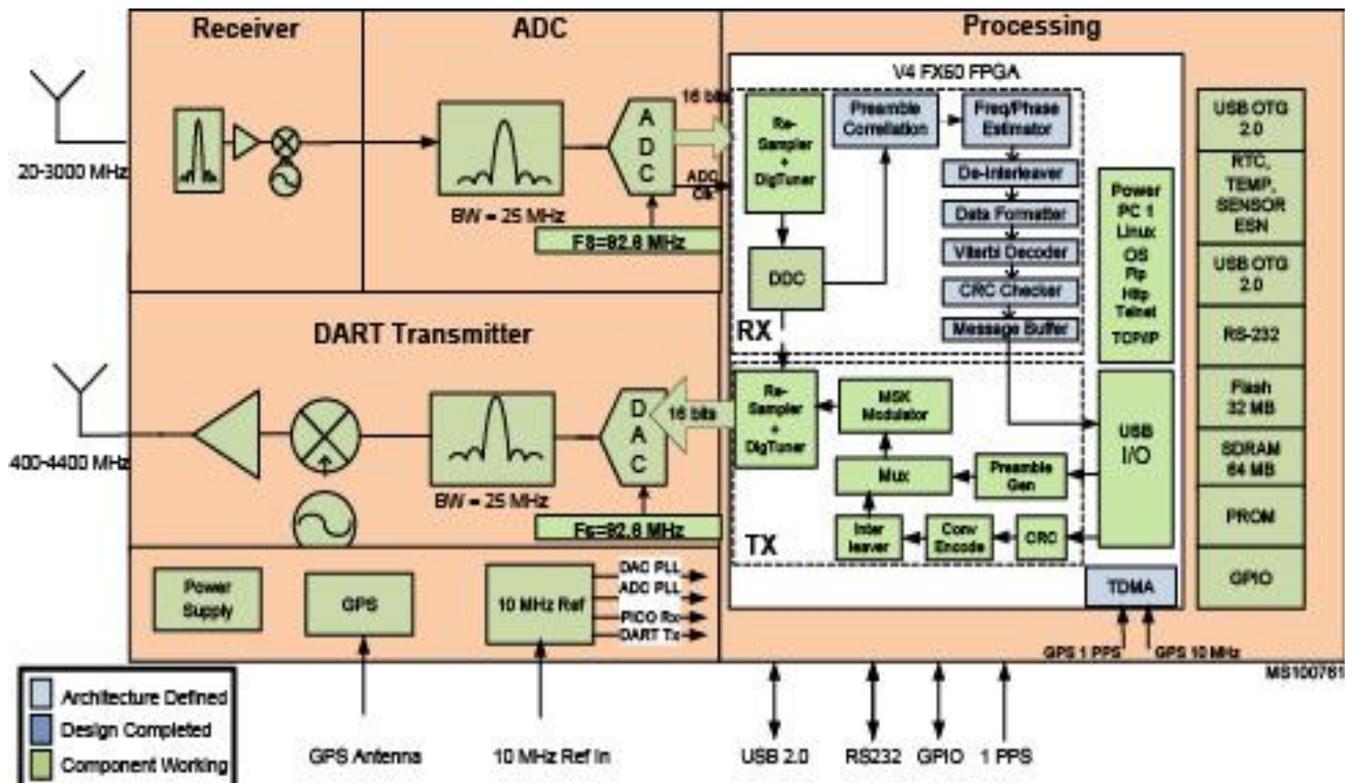


Figure 3. P5 Legacy Waveform Assembled in DART (MS100761)

The SCA specification defines an infrastructure within which many different types of modulation waveforms can be ported. It does not define how to describe “waveform processing” and therefore various approaches to waveform processing implementations can cause significant amounts of time to port a waveform from one hardware framework to another. In this paper what is meant by “waveform processing” includes the sample-to-sample operations performed to create and/or receive an RF signal. These functions include:

- Preamble Generator/Detection
- Frequency/Phase Estimation
- Resampler/Rate Adjustment
- Timing/Slot Controller
- Convolution Encoding/Decoding
- Interleaver/De-Interleaver
- Modulation Mapper (BPSK, MSK, etc.)
- CRC Generator/Checker

The DART open architecture design can be updated for SCA compliance with the integration of appropriate software modules. The porting of the P5 legacy waveform considered the above stated waveform functions and aligned the functions with the SCA standard for ease of future upgrade to SCA compliance. This approach will be considered for “best practice” implementation across DRS TCS and DRS SS to increase efficiency in achieving portability, reuseability and scaleability in DRS radio products and also in porting DRS waveforms to third party SCA-compliant radio platforms.

To facilitate the porting process, DRS selected and used the SIMULINK to FPGA design flow. Utilizing SIMULINK’s primitive and communication toolboxes, the design flow accelerates the porting process. The VHDL code is generated automatically through the SIMULINK waveform models. Additionally, the code can be verified with the same input and output test vectors generated during simulation with MATLAB / SIMULINK. VHDL simulators, such as Modelsim, can also utilize the test vectors that SIMULINK automatically generates – this functionality provides tremendous time savings to the porting engineer.

There are two processes required during the SIMULINK modeling 1.) the high-level (or reference) SIMULINK modeling and 2.) low-level (or implementation) SIMULINK modeling. The high-level SIMULINK waveform model contains the SIMULINK primitive functions for verification but not implementation. The high-level models allow the engineer to quickly verify the functionality and performance of the waveform model. The low-level model contains the vendor dependent primitives.

Once the high-level model is developed, the functional blocks of the model will be replaced by different vendor-provided low-level models. The benefit to this strong correlation between reference and implementation models is that it is identical data passed to a reference model component and its implementation counterpart can verify correctness of the implementation component; this is a good indication of the completeness of the waveform development. It also allows side-by-side comparison of the reference and implementation models for debugging, testing, and system verification.

DSP BUILDER is Altera’s Signal Compiler tool [Ref 1], which is included as one of the toolboxes in SIMULINK. DRS selected this tool mainly due to its low cost and DRS TCS’ Altera based legacy modem. Altera DSP BUILDER or Xilinx System Generator are able to convert the SIMULINK models to VHDL code, but the generated codes are all vendor dependent; this means they cannot be ported to different brand of FPGA. Porting the VHDL code was a challenge for DRS as the legacy waveform was modeled with Altera’s toolset, but the DART was designed using a Xilinx based FPGA requiring a multi-phase porting effort.

The latest tools from Mathworks enable the definition of primitives in SIMULINK that can be automatically ported to either Altera or Xilinx FPGAs. The original development of the legacy P5 waveform/modem was done prior the availability of these newer Mathworks design flow tools and thus the Altera DSP BUILDER primitives were used to describe the waveform for the legacy modem. This definition was used as a design requirement to port the waveform to the Xilinx Virtex 4 FPGA using the Xilinx System Generator SIMULINK tool. If the original waveform definition was to start today then the vendor independent primitives from either Mathworks or Synopsys (Synplify DSP primitives) would be a better development approach. The SIMULINK design flow enabled the design to be tested and validated incrementally.

Figure 4 shows the Altera UG-DSPBUILDER-9.1 and the SIMULINK / DSP BUILDER to FPGA design flow. The porting and testing process between the Altera HW and the Xilinx HW was done in several phases. The first phase was to replicate the Altera DSP BUILDER primitives-based design with the Xilinx System Generator design and compare the design outputs from CRC generator through Modulator Mapper as shown in Figure 4. The Xilinx SIMULINK design was stimulated with the same input as the Altera SIMULINK design. The results from each component along the data path were compared and modifications were made until the data results through the complete path were the same.

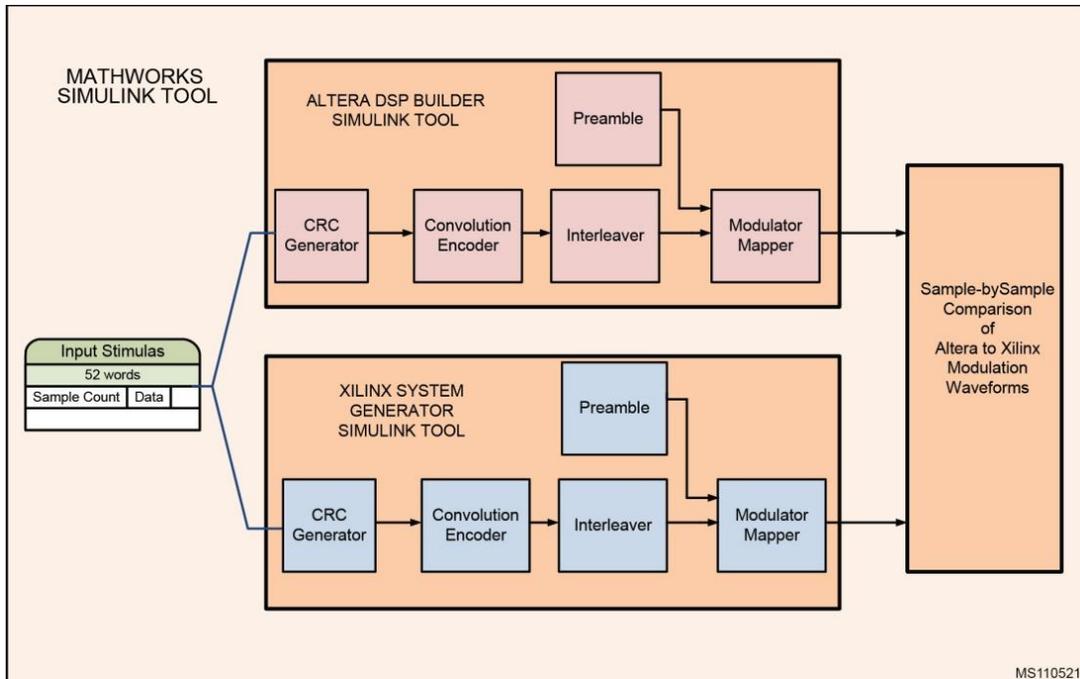


Figure 4. SIMULINK Tools Used to Validate the Xilinx Based Design Correctly Replicated the Altera Based Design (MS110521)

After successful comparison of the XILINK SIMULINK model was completed, the design was compiled to VHDL and linked with the other DART VHSIC Hardware Description Language (VHDL) design files for the device drivers and operating system. The DART image was loaded into the FPGA and tested in HW.

The HW testing used the Xilinx ChipScope tool to probe the output of the waveform modulator and compare the symbols generated in HW to those previously described in our software simulation (Figure 4). This validation was done prior to the mapper because the mapper contained a resampler to enable the DART implementation of the design to use different reference clock frequencies and ADC clock speeds. The end-to-end validation of the design in HW was done via two methods. The first was using an Agilent MXA Signal Analyzer which enabled visualization of the hard-decision outputs of the waveform in comparison with the expected symbols. The MXA can be setup to match modulation type, baud rate and other signal modulation characteristics. It proved to be an invaluable tool to validate that the desired modulation waveform was properly generated. A screen shot of the MXA display is shown in Figure 5. The four quadrants of the display were all used to show the modulation constellation, synchronize the time of when to demodulate the bursting signal, spectrum display, and informational text. This text included the Error Vector Magnitude (EVM) of the signal and the hard decision bit pattern. After successful testing with the MXA, the DART's modulation waveform was used to stimulate a legacy P5

transceiver and use its built-in-test to show successful reception of the modulation waveform.

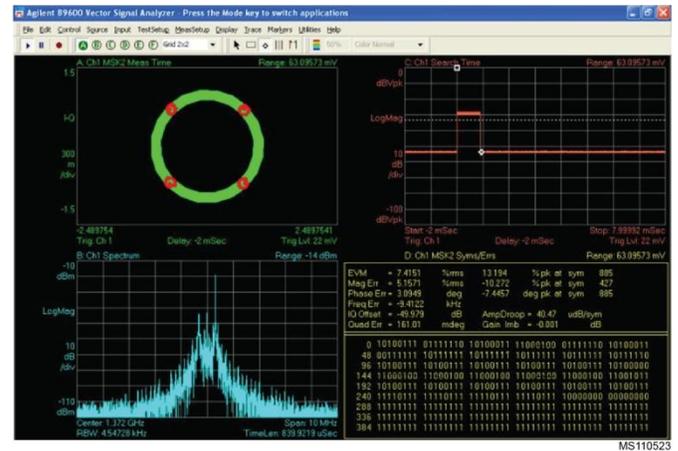


Figure 5. Agilent MXA Analyzer Used to Perform Initial Hardware Validation (MS110523)

Another waveform porting challenge was the HW differences between the legacy P5 DLT and DART platform. For example, the legacy DLT ADC sampling rate is designed exactly as a multiple of the symbol rate and the reference frequency. The DART has a much wider bandwidth and a different ADC sampling rate which is not an exact multiple of the legacy waveform symbol rate. It also uses a 10 MHz reference frequency; this is different

from the legacy DLT. The differences created a problem for direct portability since the original waveform model was targeted at the legacy DLT. To resolve this problem, two additional waveform modules were designed and inserted to the legacy waveform. The two waveform modules designed are a symbol synchronizer and re-sampler. Both modules are applicable to future waveform ports to SCA-compliant HW platforms. These waveform components would be required in a common library pool (or component containers in SCA terms) and should be standardized. Additionally, they also need to be parameterized for on the fly tailoring of different symbol rates by the software. Whenever possible all waveform components should be designed as parameterizable. Again, DRS will consider these waveform components as a “best practice” to achieve reusability of waveforms.

In early 2011, DRS successfully ported and demonstrated the legacy transmit waveform on the DART; messages transmitted by DART were received successfully by the legacy P5 DLT. The conversion of the legacy receiver and TDMA network are scheduled to be ported to DART by the end of 2011.

4.0 FUTURE WAVEFORMS PLANNED FOR THE DART

Following successful porting of the P5 waveform, DRS plans to port several additional waveforms to the DART platform. As a multi-band SDR, plans for the DART include an up-banded (4-6 GHz) variant of P5 legacy waveform and next-generation tactical instrumentation waveforms compliant with JTRS and NESI networking standards. DRS estimates the signal processing capability of the Virtex 4/FX-60 exceeds the processing requirements for these waveforms making the DART a versatile and practical platform to support test and training instrumentation well into the future. Air Combat Instrumentation equipped with the DART will allow users to select from several legacy or advanced waveforms on a mission by mission basis. This capability will facilitate backward compatibility with legacy fielded systems while allowing new higher performing airborne networks to be utilized with DART equipped systems.

5.0 DART SCA COMPLIANCE

The DART platform incorporates one Virtex-4 FPGA (either FX-12 or FX-60) to implement the SCA infrastructure. The FX-12 size FPGA is sufficiently large enough to host the JTRS SCA compatible operating environment. This environment includes CORBA and Core Framework support, in addition to control and interface to the Trusted Guard. The Virtex 4 FX-60 size FPGA enables complex waveform processing. The FX-60 was utilized to support porting the legacy P5 waveform and can support

other software-defined wideband airborne networking waveforms.

Figure 6 shows the functional allocations for an SCA-compatible DART including an SCA compatible Real-Time Operating System (RTOS), CORBA ORB, Core Framework, and SCA-compliant Application Programming Interfaces (API) [Ref 2]. As shown in the diagram, DRS will initially implement a Trusted Guard (TG) module to replace the normal Cryptographic Subsystem (CSS) found in a standard SCA red/black radio system. A subset of regular SCA API's will be supported by the TG's software adapter. DRS is considering two methods of implementing a state-of-the-art Modem Hardware Abstraction Layer (MHAL) for SCA compliance. In addition to a conventional MHAL approach to match the P5 legacy DLT Board Support Package (BSP), DRS will also evaluate the use of FPGA-CORBA endpoints, a revolutionary approach which offers superior speed and integrity over traditional SCA MHAL approaches. The MHAL promises simplified SCA interfaces and deployments to FPGA devices as well as more trouble-free operation.

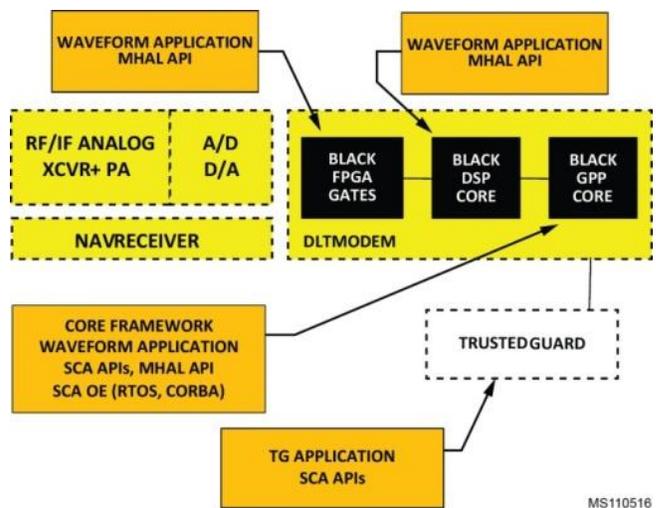


Figure 6. Functional Allocations for an SCA Compatible DART (MS110516)

Implementing an SCA infrastructure within the DART will allow rapid waveform portability and reconfigurability via the DART's open software architecture. DRS plans include a DART SCA compliance upgrade by the end of 2012, providing the DART with cross-channel connectivity such that the radio can "bridge" different radio protocols. A secondary goal is to further reduce the form factor, cost and weight.

DRS has targeted the following radio modules for standardization to further aid in rapid radio re-configurability.

- "radio frequency control" to manage the analog parts of the radio
- "modem control" manages resources for modulation and demodulation schemes (FM, AM, SSB, QAM, etc.)
- "waveform processing" modules perform the modem functions
- "key processing" and "cryptographic processing" manages the cryptographic functions
- "multimedia" module performs voice processing,
- "human interface" provides local or remote controls
- "routing" module for network services
- "control" module to monitor all functions

DRS estimates an SCA-compliant DART radio will download a stored FPGA waveform in about 20 ms. This would allow the DART to change waveforms and frequencies in 1/15th of a second - such a unique capability would enable near real-time waveform reconfigurability of the radio. There are faster reconfiguration techniques that use minimal FPGA changes or multiple co-resident code modules that will be evaluated, but are more complex to implement.

6.0 DART DEMONSTRATIONS

Two successful demonstrations have been held in DRS TCS Fort Walton Beach facility. The objective of these demos was to show the DART SDR HW platform is capable of hosting the P5 legacy waveform. The objective was satisfactorily met.

During November 2010, the first demonstration, Figure 7, used the DART as a P5 legacy DLT repeater. It accepted the RF signal generated by one legacy DLT then digitized it internally and retransmitted to the another legacy DLT. This demo verified DART's RF performance and backward compatibility to the legacy DLTs.

In June 2011, DRS demonstrated the DART transmitter successfully transmitting 10 messages per second to the legacy DLT. The demo demonstrated the readiness of the TDMA timing control, digital MSK modulation and IF frequency offset solution bringing the DART technology to TRL 6/7. DRS plans to move the DART to TRL 8 in 2011 and field the radio as a form-fit-function replacement of legacy P5 DLTs. The DART will provide airborne test and training instrumentation with a reconfigurable SDR capable of operating as a legacy DLT and ready for advanced networking waveforms.

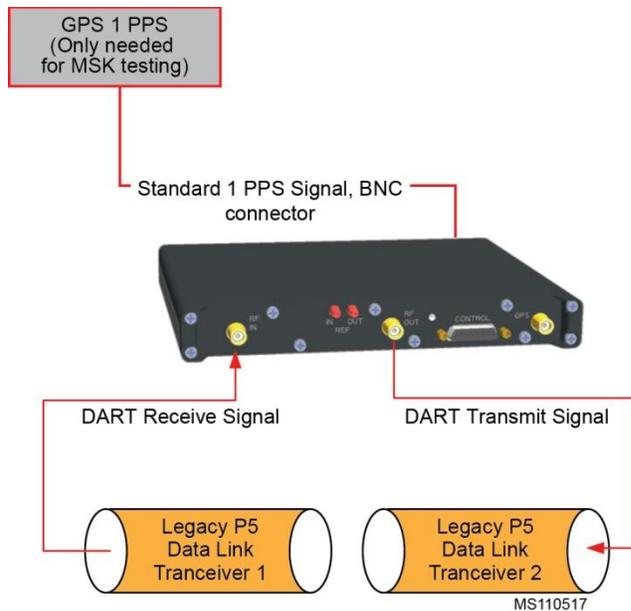


Figure 7. Demonstrations of DART RF Performance (MS110517)

7.0 CONCLUSION

Through cross corporation internal investment supported by SCA Technica Inc.'s strong experience in software communication architecture technology, DRS has developed concepts and techniques that use a software defined radio platform for rapid development of airborne RF networking capability. DRS is developing "best practices" to take full advantage of the DART platform's flexibility as not only a development and SCA reference platform, but also as an airborne network product. The DART will provide DRS' test and training product line with significant flexibility to run multiple legacy and modern JTRS airborne networking waveforms. In addition, the DART has potential for cross-channel connectivity that would greatly increase interoperability among systems operating on disparate airborne networks.

Through developing internal "best practices", DRS plans to fully embrace the power of software defined radio technology and the SCA to develop next generation airborne network capability, specifically:

- Hosting legacy waveforms to the DART SDR
- Hosting advanced waveforms with bandwidths up to 25 MHz and data rates > 75 Mbps to the DART SDR
- Hosting the SCA architecture on the DART to enable porting of JTRS waveforms
- Hosting customer specified advanced instrumentation waveforms to the DART SDR
- Integrating encryption via the SCA CSS

To date, DRS has successfully ported the transmitter side of the P5 Data Link Transceiver to the DART SDR and demonstrated this capability in the lab. The P5 DLT receive side is planned to be completed in 2011. The DART's architecture is adequate to host other advanced waveforms and the SCA environment establishing a viable platform for future JTRS waveforms.

DRS has experienced several challenges during the development effort, resulting in several lessons learned that will be incorporated in future DRS development efforts as "best practices". The first lesson learned involved using the SIMULINK tool flow for defining and porting the P5 legacy waveform to the DART. The developer should always select a SIMULINK tool flow that enables primitives or blocks compatible with multiple hardware targets, instead of using FPGA vendor specific blocks. This will significantly decrease the effort to port the modulation waveform to different FPGA or DSP architectures. This approach is valid when porting waveforms to SDR platforms with or without the use of the SCA. A second lesson learned is waveform designs should expect different hardware architectures to use different clock rates. The waveform should be designed so it can be implemented on different hardware platforms with different clock rates. Defining the modulation waveform in a manner that makes it easy to change reference frequency and data converter clock rates will simplify the porting process. DRS is considering an approach to standardizing waveform development processes as a "Best Practice".

In summary, DRS successfully demonstrated the capability to rapidly port waveforms to the DART platform establishing backward compatibility with legacy data links. In-house demonstrations of the DART have established the technology to be TRL 6/7. DRS expects to complete porting the receive side of the legacy P5 waveform within several weeks since the verified transmitter model can now be used as a test stimulus in SIMULINK.

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- [2] Design of Multi-Platform & SCA-compliant Software Components, Daniele Olmisani – SELEX Communications S.p.A, <http://data.memberclicks.com/site/sdf/SCA-Olmisani.pdf>

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