SDR'11 – WInnComm

A Software-Defined Radio Prototyping Platform for Cognitive Radio Applications

Christian Kocks

Department of Communication Technologies

University of Duisburg-Essen

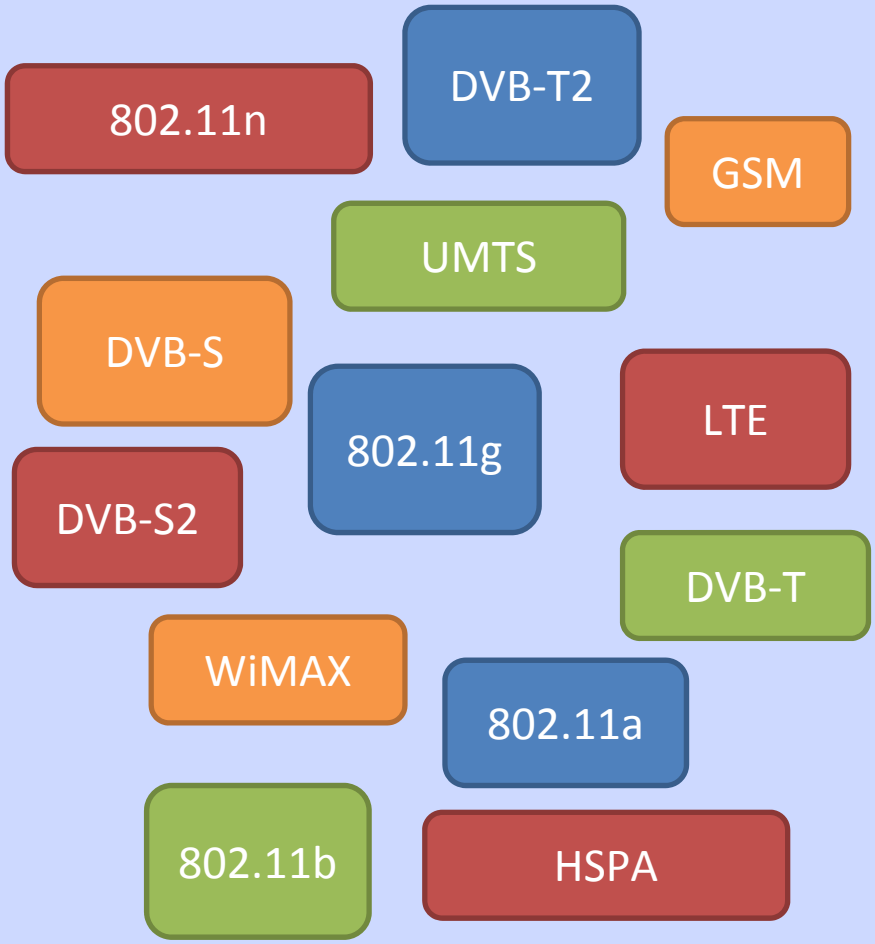
christian.kocks@kommunikationstechnik.org

Outline

- Motivation
- Platform Overview
- Cognitive Radio System Implementation
- Sensing Results

Motivation

- Multitude of wireless communication systems came up in the last years
- Increasing system complexity (higher-order modulation, sophisticated forward error correction etc.) to increase spectral efficiency



Motivation

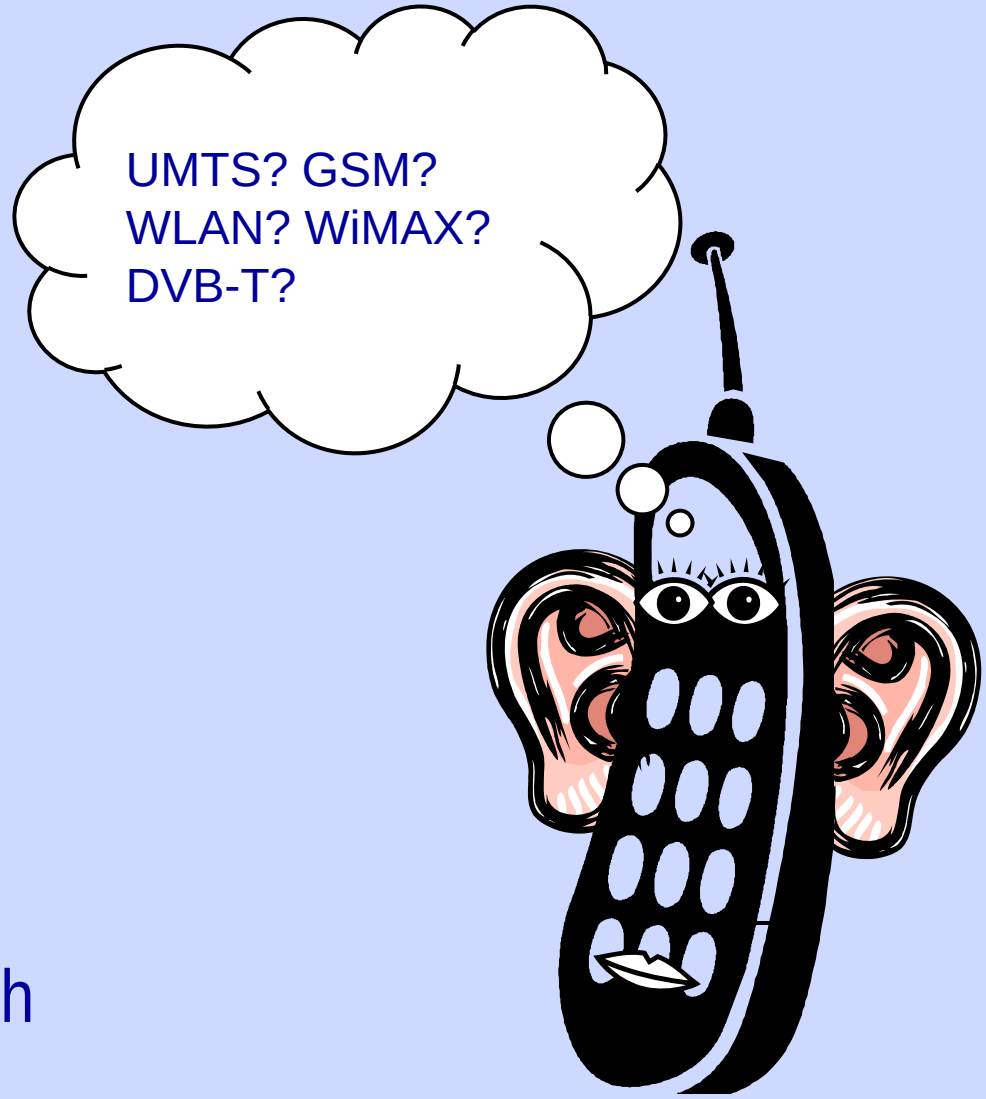
- The range of usable frequencies is limited
  - Lower frequencies require unworkably large antennas
  - Higher frequencies only propagate over very short distances

- Thus some spectrum bands are more valuable than others
  - Causes an additional squeeze at certain ‘sweet-spot’ frequencies (typically 500 MHz – 5 GHz)

By courtesy of R. Womersley

Motivation

- Flexible prototyping platform desirable
- Implementation of arbitrary communication systems
- Cognitive radio capabilities
  - Sense the environment
  - Track the changes
  - React upon findings
- Software-defined radio approach advantageous



Platform Overview – Requirements

- Rapid Prototyping Capability
- Efficient Scheduling
- Elaborate Debugging Functionality
- High Degree of Parallelization Capability
- High Modularity
- Scalability

Platform Overview – DSP

- Prototyping platform *eFalcon* hosts a powerful triple-core C6474 DSP for top-level scheduling and signal processing with elaborate debugging functionality
- DSP features:
  - 1 GHz system clock
  - 3 MB on-chip RAM
  - EDMA controller
  - Gigabit Ethernet
  - Serial RapidIO (two lanes)
  - Antenna interface (6 full-duplex OBSAI/CPRI links)
  - Turbo and Viterbi decoder
  - …

DSP	Digital Signal Processor	OBSAI	Open Base Station Architecture Initiative
RAM	Random-Access Memory	CPRI	Common Public Radio Interface
EDMA	Enhanced Direct Memory Access		

Platform Overview – FPGA

- Xilinx Virtex-5 SX50T FPGA directly attached to the DSP using high-speed serial interconnections (Serial RapidIO, OBSAI, CPRI)
- FPGA features:
  - 52,224 logic cells
  - 4.7 Mbit block RAM
  - 12 digital clock managers (DCM)
  - 12 RocketIO transceivers
  - …
- FPGA can be used as co-processor dedicated to specific signal processing tasks

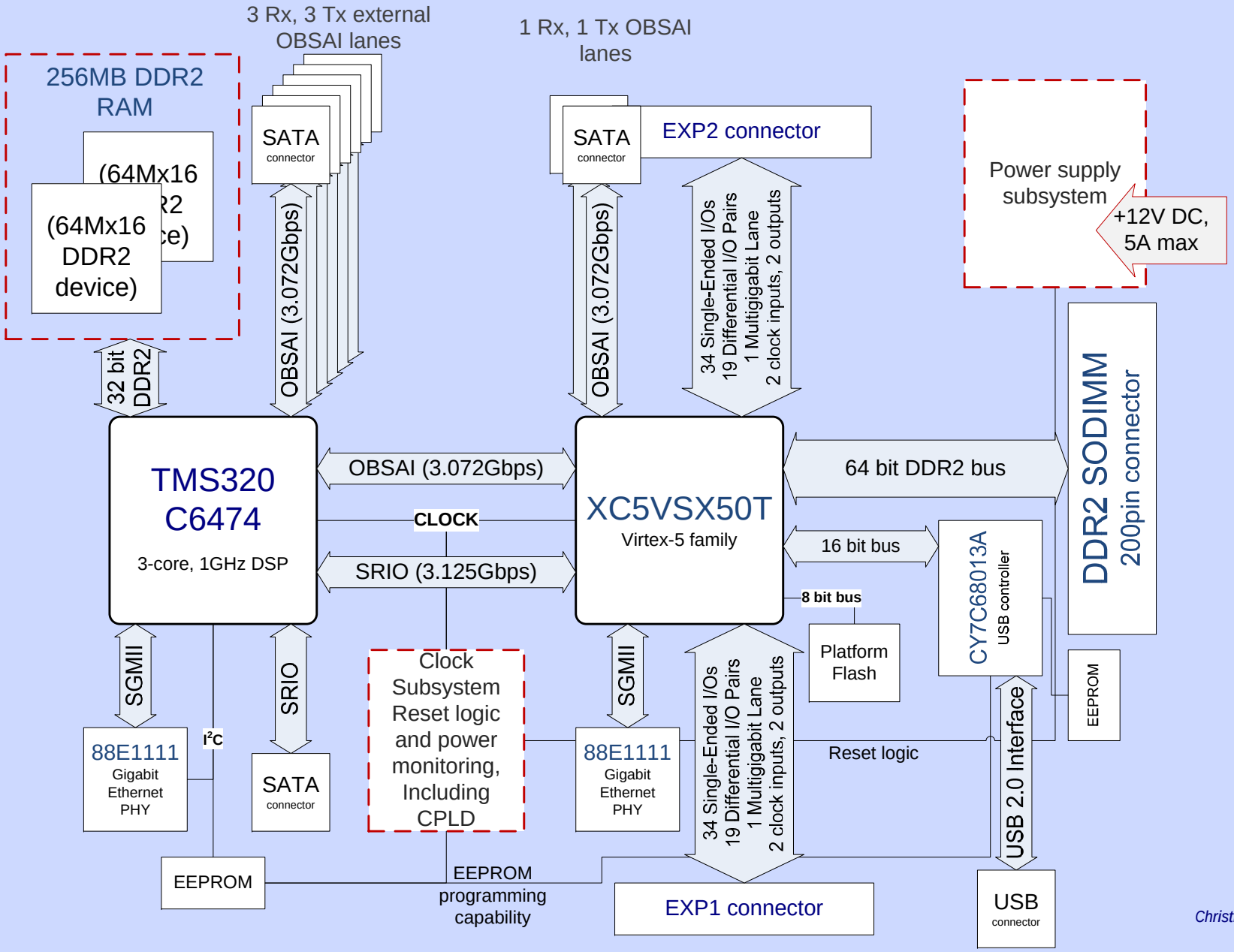
FPGA	Field-Programmable Gate Array	CPRI	Common Public Radio Interface
DSP	Digital Signal Processor	RAM	Random-Access Memory
OBSAI	Open Base Station Architecture Initiative		

Platform Overview – Additional Features

- 256 MB DDR2 RAM directly attached to the DSP
- DDR2 SODIMM connector directly attached to FPGA
- USB 2.0 controller with 8051 microcontroller connected to the FPGA
- 2 Gigabit Ethernet PHYs connected to the DSP and the FPGA
- SD memory card slot
- Avnet Full EXP connectors acting as daughter card interfaces
- Sophisticated clock subsystem

DDR	Double Data Rate	FPGA	Field-Programmable Gate Array
RAM	Random-Access Memory	USB	Universal Serial Bus
DSP	Digital Signal Processor	SD	Secure Digital
SODIMM	Small-Outline Dual In-Line Memory Module		

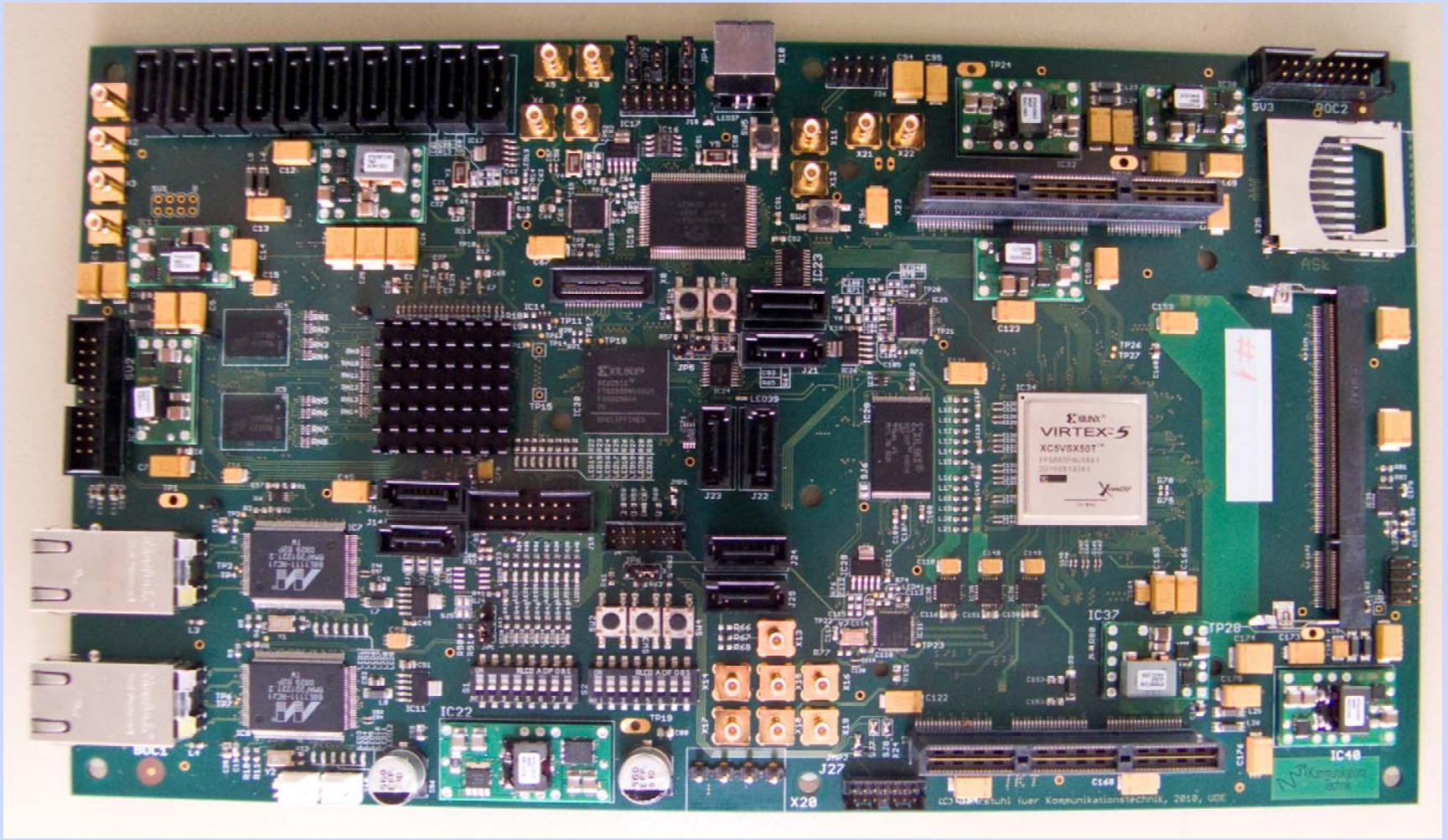
Platform Overview – Block Diagram



Scalability Aspects

- Crucial design constraint during concept phase
- *eFalcon* provides high-speed intra-board as well as inter-board communication
- Interconnection of multiple platforms with data rates beyond 1 Gbit/s possible
- Realization of multi-antenna systems possible
- Overall clock synchronization possible by coaxial connectors

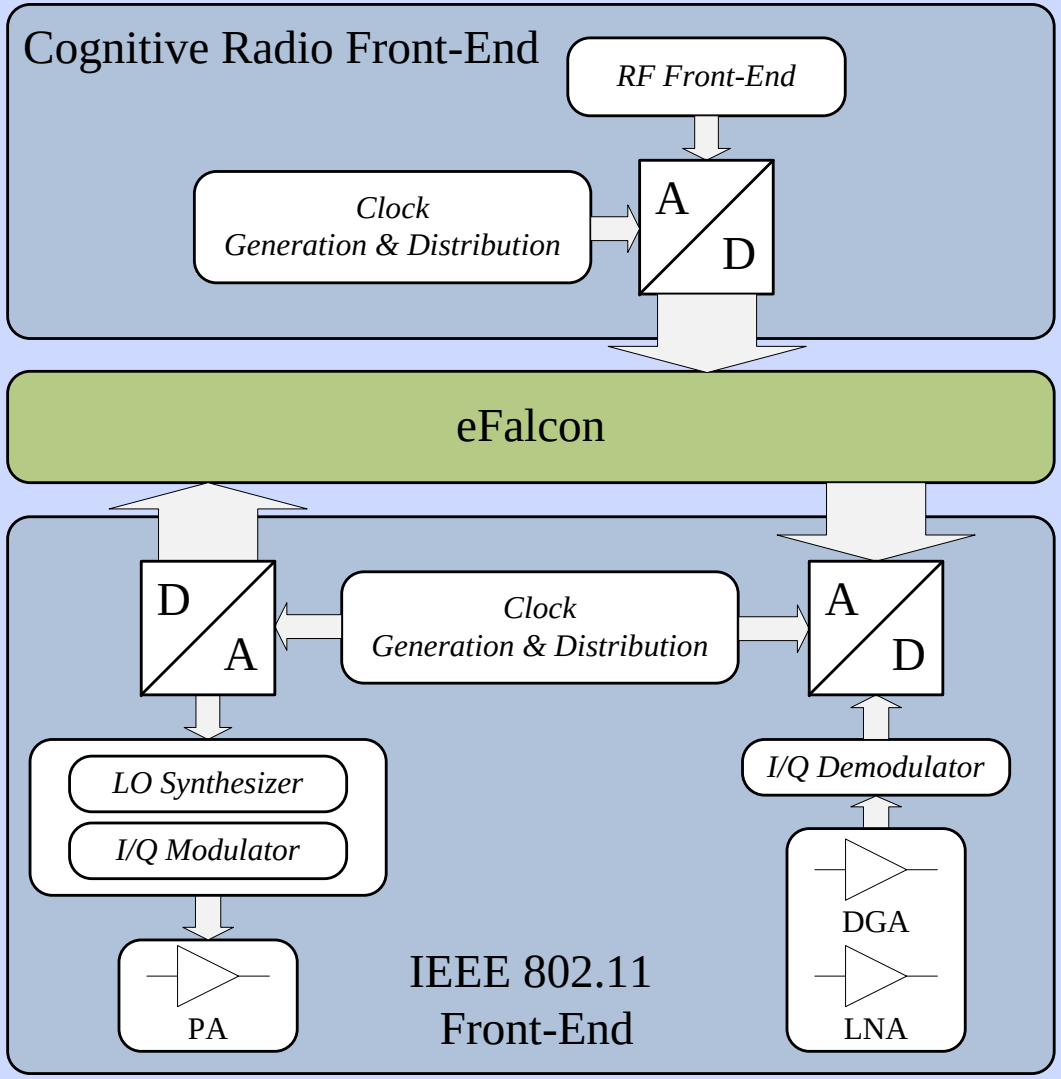
Platform Realization



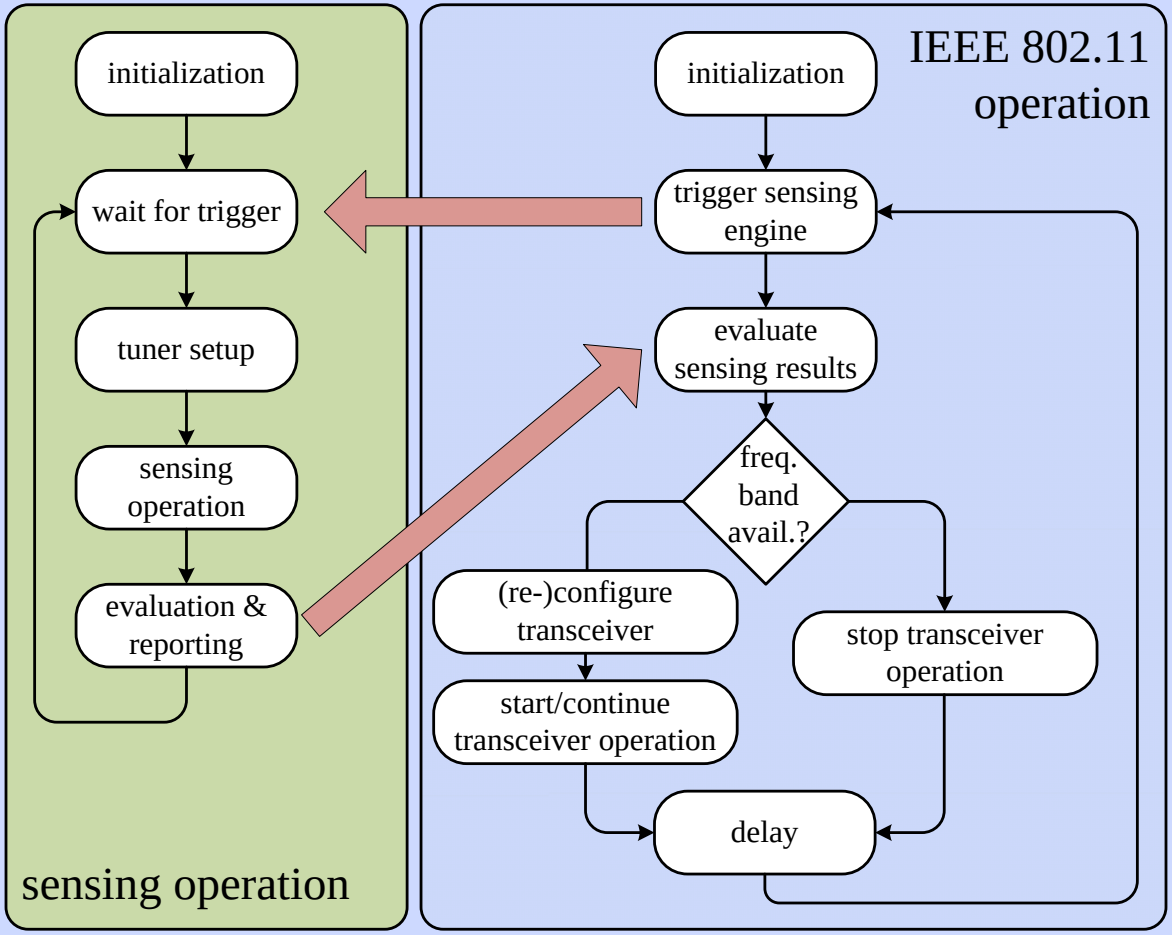
Cognitive Radio System Implementation

- Non-occupied frequency ranges in the UHF band (TV white space)
- Can be used for secondary communication systems
- Here:
  - Primary system: CMMB
  - Secondary system: IEEE 802.11
- Sensing approach based on autocorrelation algorithms

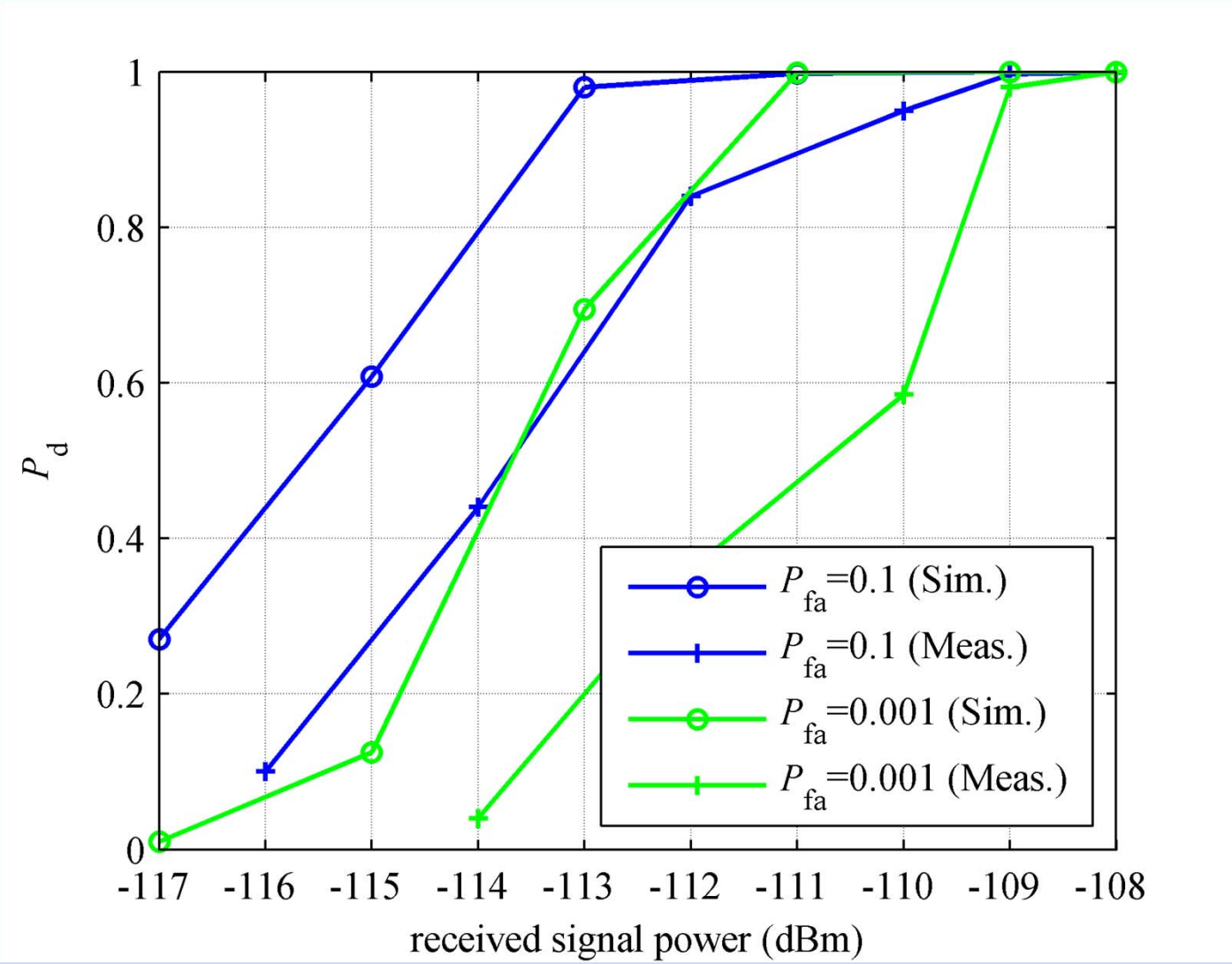
Cognitive Radio System Implementation



Cognitive Radio System Flow Diagram



Sensing Results



A Software-Defined Radio Prototyping Platform for Cognitive Radio Applications

Thank you for your attention!