

A Real-Time Multi-Path Fading Channel Emulator Developed for LTE Testing

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1: Texas Tech University, 2: Innovative Integration

Design Goals



- Perform specified LTE conformance tests
- Design for long-term reuse
- Compact, simple, and easy to use

Setting the Stage



- Downlink LTE receiver development
- Software simulations only go so far.
- In the process....we had to also develop an LTE transmitter!
- Testing your receiver with a "golden" reference signal source has limited use

A Typical OFDM System Model





Impairments:

- AWGN: faint (noisy) signal
- Frequency shift: errors in RF electronics (TX and RX)
- Channel: Asynchronous startup time, multiple paths, mobility
- Sample Clock Offset

Our OFDM System Model





Repartitioning of the system:

• The transmitter and receiver are placed in two separate pieces of hardware and operate asynchronously.

- The transmitter must be capable of producing LTE signals
- The user must be able to program various signal impairments for desired tests

LTE Signal Generator





Host PC Software

- Generates low-rate baseband signal (repetitive)
- Provides "golden" signal to the hardware
- Software signal generation adds flexibility X5-TX Firmware
- Run-time configurable core does the "heavy lifting"
- Run-time programmability is ideal for R&D development cycle

LTE Signal Generator





Channel Emulator:

- Must conform to the LTE specified channels
- Must be capable of emulating a "fading" channel
- Must be very programmable and customizable to maximize reuse and value

LTE Specifications



ITU channel models [1]	ETU (extended typical urban)		EVA (extended vehicular A)		EPA (extended pedestrian A)	
tap index	delay (ns)	power (dB)	delay (ns)	power (dB)	delay (ns)	power (dB)
1	0	-1	0	0	0	0
2	50	-1	30	-1.5	30	-1
3	120	-1	150	-1.4	70	-2
4	200	0	310	-3.6	80	-3
5	230	0	370	-0.6	110	-8
6	500	0	710	-9.1	190	-17.2
7	1600	-3	1090	-7.0	410	-20.8
8	2300	-5	1730	-12.0	-	-
9	5000	-7	2510	-16.9	-	-

ITU Channel models [1] :

- Provide statistical references for various channel conditions
- Each channel model is specified as a power-delay profile (PDP)
- In LTE testing, each PDP can be used with a 5, 70, or 300 Hz [1] maximum Doppler frequency to simulate various mobility scenarios.
- Each path uses a Jakes, or "Classical" Doppler spectrum

Dynamic Multi-Path Fading Channel



- The radiated signal bounces off of objects in the channel as it propagates
- The receiver hears echoes as the delayed paths arrive
- As the receiver moves throughout the channel, the relative intensity of each path varies. The rate of variation depends on the mobile's velocity and the wavelength of the carrier.



2D Ray Model



• Assume there are no direct line-of-sight paths, only reflected ones

ТΧ

- "Diffuse" channels can be modeled with discrete paths
- Path delays are constant

RX

2D Ray Model





2D Ray Model





Tapped Delay Line Model



- Each path in the channel is multiplied by a complex coefficient
- Individual paths are delayed by the amount specified in the PDP
- The delayed and attenuated copies all sum together at the receiver
- Convolution!! [2,3]



- The minimum tap delay spacing determines the rate of the channel filter
- The channel coefficients must be updated at the operating rate of the filter.

Channel Emulator "Unit Cell"





Jakes Process [3]



- Each channel path gain can be modeled by a Jakes process [2]
- Each path coefficient in the emulator is generated by an i.i.d. stochastic Jakes process, which depends on the carrier wavelength and the mobile's velocity
- The Jakes spectrum defines the probability distribution function of the Doppler shift



Path Coefficient Generator



- To generate a Jakes process, WGN is shaped with a special Jakes filter
- The Jakes filter shapes the WGN spectrum to approximate the "bath tub" shape





1

• The upsampling factor determines the final Doppler frequency by shrinking the relative passband of the Jakes filter



0

Normalized Frequency (x rad/sample)

0.2



• The desired Doppler frequency range determines the required upsampling factors



$$L = \text{round} \left(\frac{f_s}{f_{\text{max}} f_d} \right) \qquad \begin{array}{l} f_{\text{max}} = 5 \text{ Hz} \\ L = 25,706,941 \end{array} \qquad \begin{array}{l} f_{\text{max}} = 70 \text{ Hz} \\ L = 1,836,210 \end{array} \qquad \begin{array}{l} f_{\text{max}} = 300 \text{ Hz} \\ L = 428,449 \end{array}$$



• Upsampler is partitioned into fixed and variable stages



Doppler resolution decreased to ~.01 Hz





Design Goals

- Minimize resource consumption my maximizing resource sharing
 - Saves hardware multipliers and slices
 - Place the most complex components at the lowest rate
- Minimize filter lengths
 - Saves BRAMs required to store filter coefficients
 - Use special filter designs
- Minimize reduction of Doppler resolution
 - fixed upsampler rate must not be too high
- Maximize range of available Doppler frequencies











- > 80 dB stop-band attenuation
- fast roll-off
- MATLAB double-precision floating point results shown here





- 10x magnification along the frequency axis shows Jakes response
- > 80 dB stop-band attenuation
- Total coefficient storage is less than the upsampling factor!!



Filter	Filter Length	Optimized Length
Jakes shaping filter	125	63
2x half-band upsampler	59	16
4x 1/f taper upsampler	90	45
32x reduced length upsampler	139	70
total:	413	194





• Linear interpolation relies on only two points to compute the interpolated values

 $s[n] = \frac{1}{N} (x[m]n + x[m-1](1-n))$ $n = [0,1,\dots,N-1]$ $N = \operatorname{round}\left(\frac{L}{256}\right)$



- Fixed-point FPGA hardware results (not simulation real results)
- Extremely high-quality frequency response



Variable Delay Element





Resource Consumption: Unit Cell



- Post MAP resource usage
 - Xilinx Virtex5 SX95T FPGA
 - XST MAP Xilinx tool version 13.2

	Elements Used/Available	Ratio
Occupied Slices	857/14,720	5%
BRAM	6/244	2%
DSP48E	21/640	3%



Resource Consumption: Entire Channel Emulator (9 paths)



- Post Synthesis resource usage
 - Xilinx Virtex5 SX95T FPGA
 - XST version 13.2

	Elements Used/Available	Ratio
Slice Registers	22,379/58,880	38%
BRAM	45/244	18%
DSP48E	209/640	32%



Results: EPA Model



• Results from FPGA hardware (100 MHz sampling rate)



Results: EPA Model





Results: EVA Model





Results: EVA Model





Results: Instantaneous PDP





Conclusions:



- Highly programmable channel emulator core
- Capable of LTE conformance tests and custom tests for R&D
- Low cost
- High reusability potential (expandable to MIMO)
- Small FPGA resource consumption
- Expandable to higher order models using modular design
 - ✓ Perform specified LTE conformance tests
 - \checkmark Design for long-term reuse
 - \checkmark Compact, simple, and easy to use





[1] 3GPP TS 36.141 V8.9.0: "Base Station (BS) conformance testing", December 2009.

[2] M. Jeruchim, P. Balaban, K. Shanmugan, Simulation of Communication Systems: Modeling, Methodologies, and Techniques, Kluwer, New York, 2000

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[4] W.C. Jakes, Microwave Mobile Communications, Wiley, New York, 1974

[5] F. Harris. "Resampling Filters", in Multirate Signal Processing for Communications Systems, Upper Saddle River, NJ: Prentice Hall PTR, 2004, ch. 7, sec. 6

