Adaptable Architectures for Advanced Space-Based Communication Systems

Vincent J. Kovarik Jr.
S. Fenton McDonald
Melbourne, FL
{vkovarik,fmcdonal}@harris.com

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Presentation Outline

- Background and Motivation
- SDR Architecture
- Software Radio Configuration and Control
- High-Performance Signal Processing Architecture
- Space-Deployment Challenges and Mitigation
- Conclusion

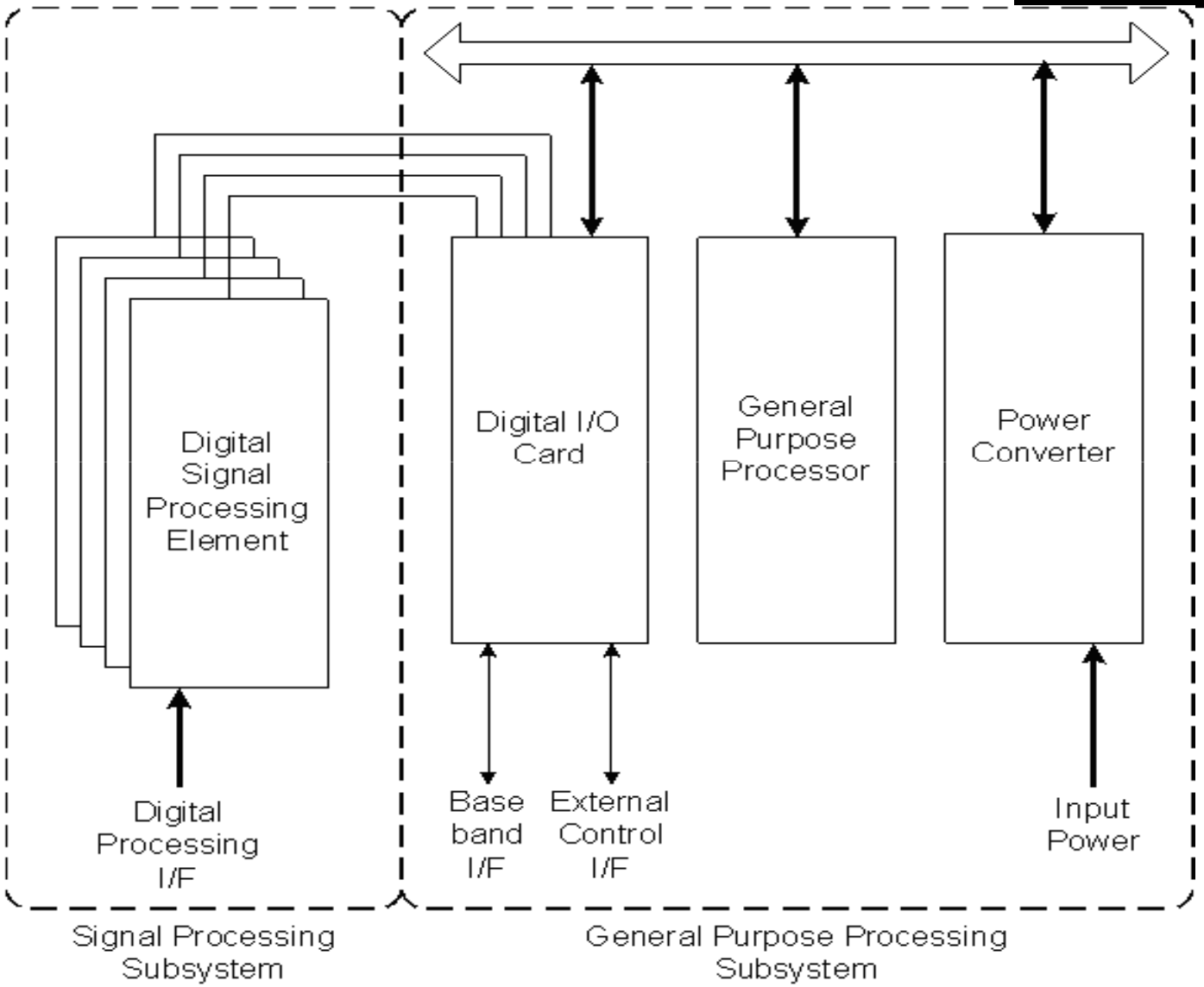
Background and Motivation

- Software reconfigurable radio and communications systems have been evolving for several decades.
- Commercial applications of software reconfigurable systems have been in use for some time.
- Harris has been developing signal processing technology suitable for space deployment for several years.
- Through collaboration with NASA on the CoNNeCT program is providing an opportunity to test a high-performance, reconfigurable radio system in-situ on the International Space Station (ISS).

SDR Architecture

- A bank of reconfigurable modems provide processing for multiple waveforms
  - Each modem in the bank is individually powered
  - For scenarios with one waveform, power can be saved by enabling only one modem
- General Purpose Processor controls the modem operations
  - Includes loading waveforms
  - Uses COTS offerings
- Digital I/O card interfaces with vehicle
  - “Unique” card for each solution
- Backplane connected modules can be block redundant
  - Modems are N-of-M redundant
- RF electronics can be separated from radio and placed close to aperture.
- The result is a highly available system that can process multiple waveforms.

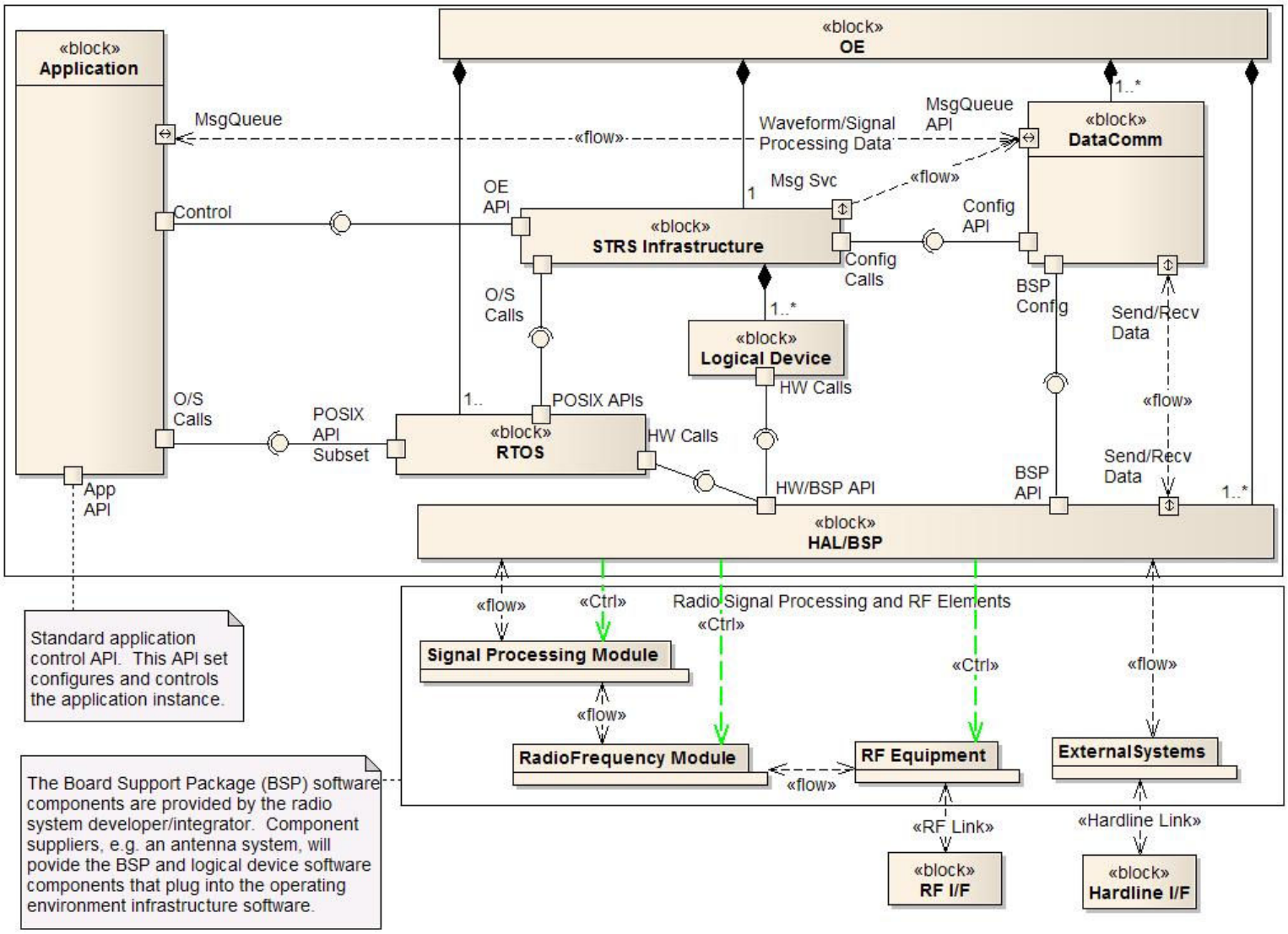
Standards-Based SDR Architecture



Software Control Architecture

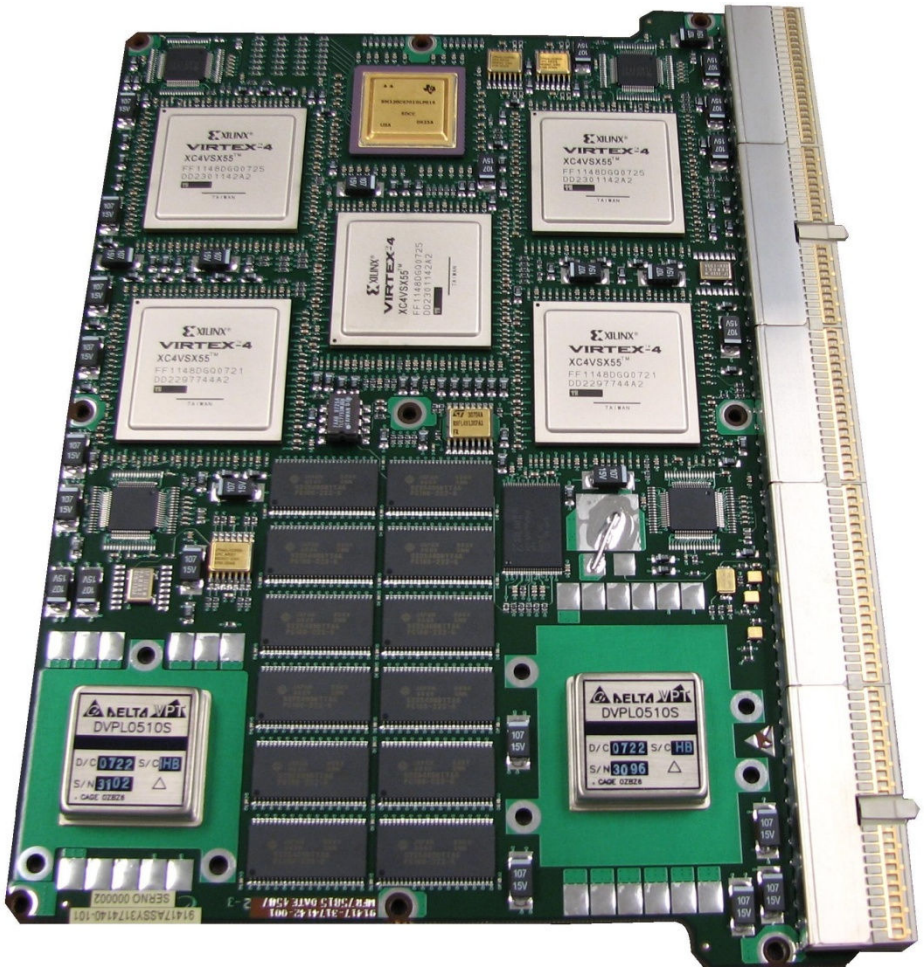
- Multiple standards have evolved for the management of software reconfigurable radio systems:
  - The *Software Communications Architecture* (SCA) developed in conjunction with the Joint Tactical Radio System (JTRS) program.
  - The *PIM and PSM for Software Radio Components* developed by the Object Management Group (OMG)
  - The *Space Telecommunications Radio System* (STRS) developed by NASA.
- The CoNNeCT program is using the NASA STRS specification for the control interfaces to the radio system.

Software Control Architecture

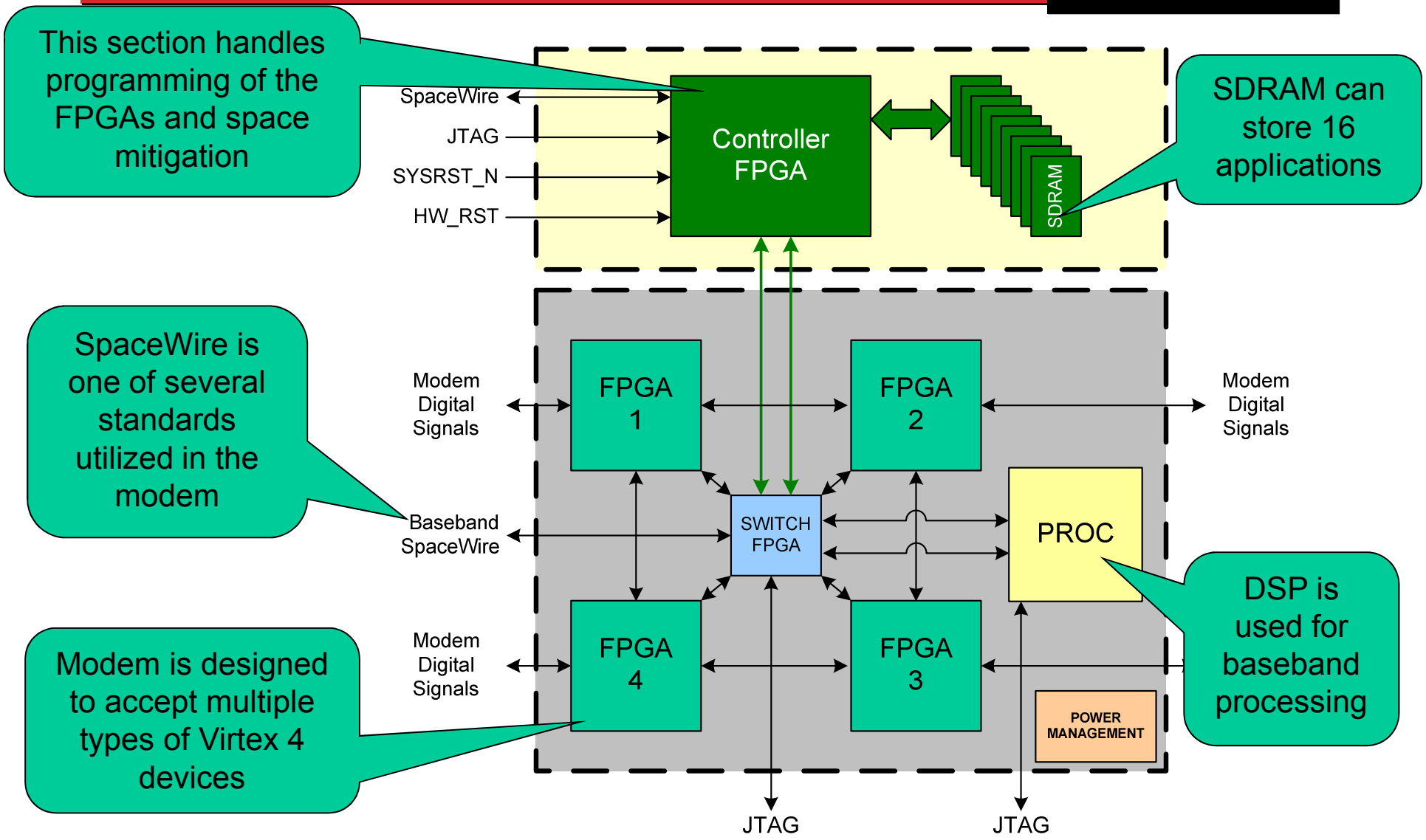


Signal Processing Section

- Harris' Programmable Modem products utilize FPGA technology which allows a single hardware platform to implement multiple waveforms
- Harris has invested in moving this technology from ground and avionic solutions to Space missions.
- A functional prototype is already in use for testing and waveform development.



Overview of the V4 Architecture



Waveform Hardware Abstraction

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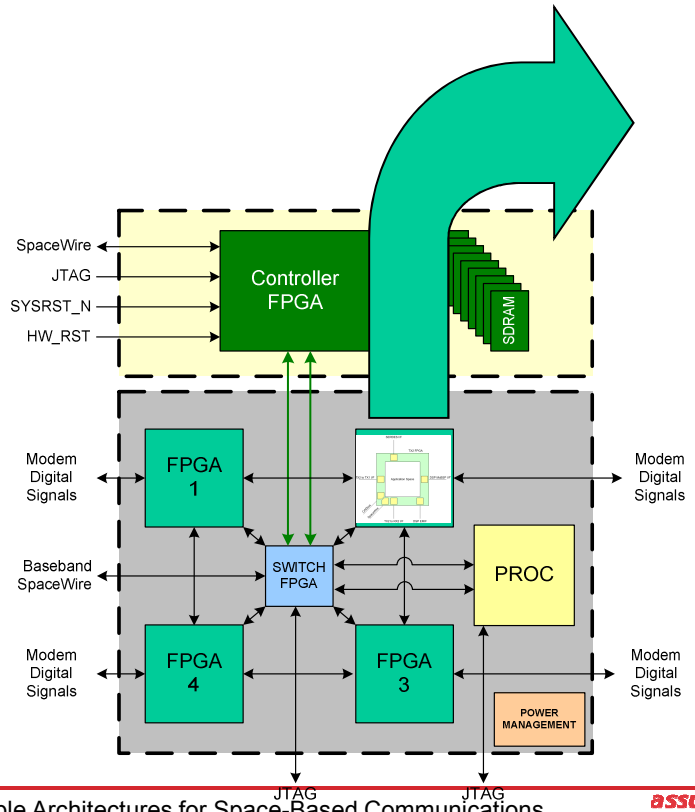
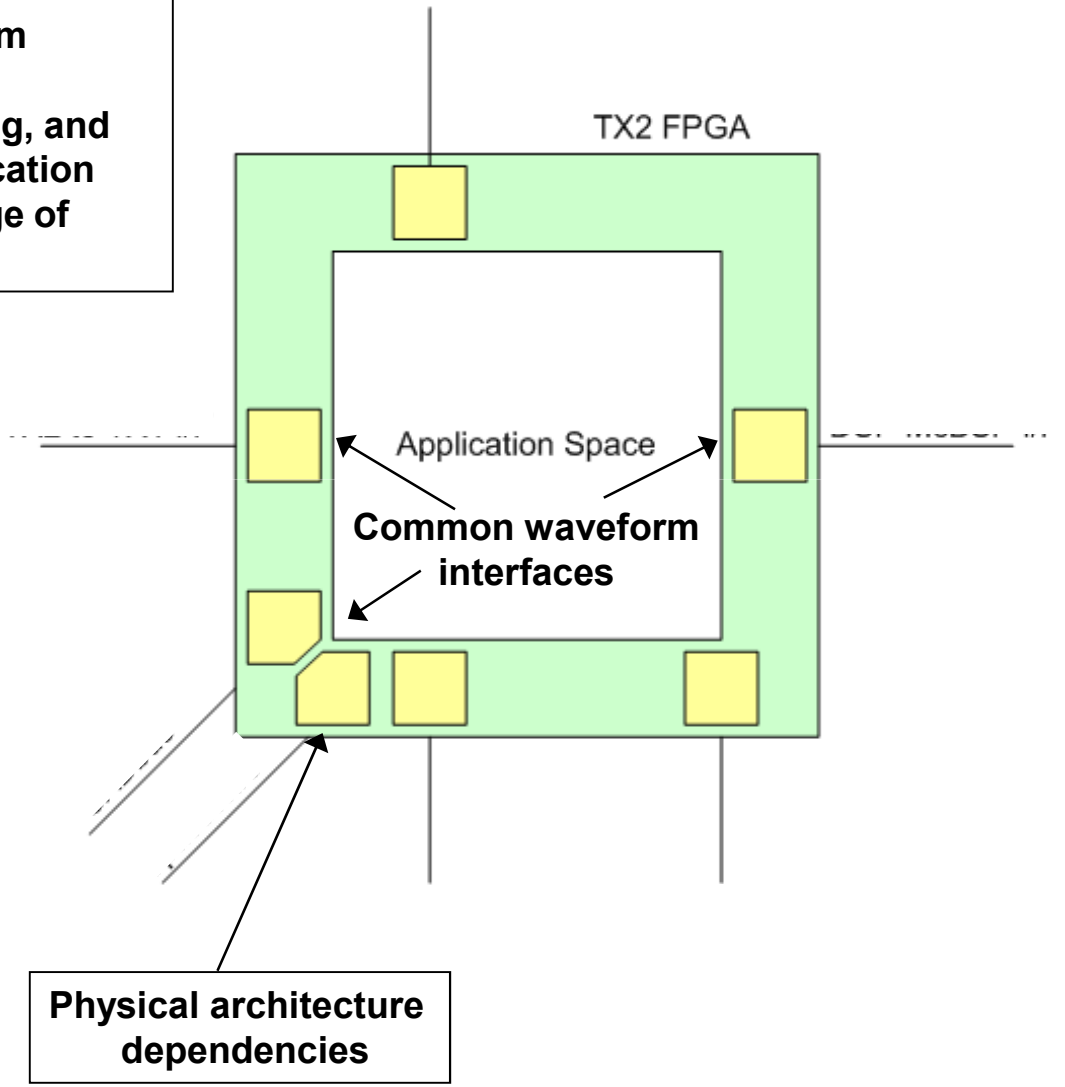
- A toolkit is being created to assist programmers in developing FPGA applications
- In this system, the application developer is given a configurable code set where each interface can be selectively included
  - Removing unused interfaces increases overall gate capacity
- Each interface is designed for space mitigation and will be certified to cause no harm to the overall system
  - This certification is handled through range and protocol checking
  - An ICD will be delivered with toolset to define the application interface
- Multi-FPGA simulation models will be provided that help validate the user's application in a simulated modem environment
  - Includes all commanding interfaces
- Demonstrated Module Wrapper in April 2008
  - Ported an existing OFDM transmit waveform operating at 54 Mbps to the modem
  - Porting of waveform took less than 2 weeks.

Module Wrapper Concept

- The wrapper abstracts the physical dependencies away from the waveform implementation.
- This facilitates reconfiguration, porting, and enhancements by not requiring application developers to have detailed knowledge of physical dependencies.





Space Deployment Problems

- Reconfigurable systems technology has been successfully applied to the terrestrial domain.
- Significant issues must be addressed to successfully deploy the same capability in space, e.g.
  - Size, Weight and Power (SWAP) constraints
  - Radiation effects
  - Long-term deployment
  - Remote access

Mitigating Single Event Upsets (SEUs)

- The Functionality of a Xilinx Vertex 4 is stored in it's Configuration Memory,
  - *This is what makes a Flip-Flop and routes signals to the Flip-Flop*
  - SEU can change the functionality (No longer a Flip-Flop)
  - Can open wires between gates (~90% transistors are used for routing)
  - A change to this Configuration memory can be detected/corrected using Readback, Compare, and Repair.
    - Configuration Memory Can be Read & Rewritten without effecting device operation.
- The results of the application are handled by the configured logic
  - *Makes sure the value in the Flip-Flop is correct*
  - Triple Modular Redundancy of all logic resources, including I/O, feedback paths, throughput logic, and special resources (DLL's) can mitigate an upset in the application.

Single Event Upset (SEU) Testing

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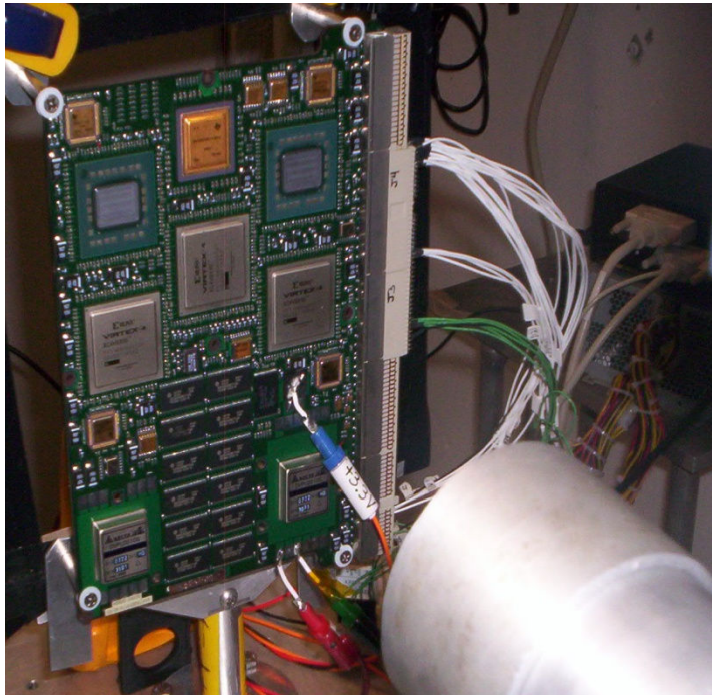
- In 2008 the Space Modem was tested for Single Event Upset mitigation at the Texas A&M Cyclotron facility.
- V4 modem was initially tested in a simulated solar flair environment, but not enough errors were produce. So, the flux rate was increased by ~10x
- Four conditions were tested



Test Condition	Error Improvement
Non-TMR without Scrubber	Normalized to 1
Non-TMR with Scrubber	167 to 1 reduction in errors
TMR without scrubber	10% increase in errors
TMR with scrubber	2500 to 1 reduction in errors

V4 Space Modem has been successfully tested for space mitigations

Conclusion

- Harris has been actively developing a Space Qualified Software Defined Radio
- Current V4 Modem design provides high-performance, adaptability, and space-deployment qualification
- Management software is being developed that is STRS compliant
  - Space qualified SDR implementation leverages existing baseline applications
- Additional application areas and capabilities are being investigated for insertion of this technology