STATE VARIABLE WIDEBAND TUNABLE FILTER

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ABSTRACT

Wideband RF front end is susceptible to narrowband interferers that can impair the performance of the receiver. Currently there are no tunable filters that can be swept across bandwidths greater than 1 GHz. The paper proposes an innovative state variable filter which can be placed at the receiver front end covering frequency up to 10 GHz. The technology enables developing multiple filters which can be independently applied to the bands of operation. Alternatively, they can be brought in close proximity to each other in order to change the filtering characteristic. The state variable wideband tunable filter is digitally controlled by an eternal micro-controller or DSP.

1. INTRODUCTION

Software defined radio (SDR) has been considered as a solution to dynamically reconfigurable functionalities in the presence of a number of different access technologies [1]. For example, a software defined smartphone with a frequency range from 400 MHz to 6 GHz will require an analog-to-digital converter (ADC) with sampling rate of 11 Gsps to satisfy the Nyquist criteria [2,3]. This frequency range will accommodate all existing and future cellular, GPS, Bluetooth, WiFi, WiMAX and LTE bands. Such an ADC does not exist now and, if it did, the power consumption would be unacceptably high for portable applications [4]. The classical wideband architecture consists of multiple receiver front ends, each with a band-select surface acoustic wave (SAW) filter. The channel selection is done in the digital domain, usually by the sigma-delta (Σ-Δ) ADC [5,6]. This architecture is cost effective and implementable, but it has several deficiencies. One of them is incapability of adaptive frequency allocations. This problem is exasperated by non-harmonized and fragmented nature of worldwide frequency allocation. A new receiver front end has to be added in anticipation of new frequency allocation – a time consuming and expensive engineering exercise. Next generation wireless services range from voice to HDTV streaming. Therefore, the bandwidth can vary from 4 KHz to potentially over 20 MHz [7]. In a frequency congested environment, this scenario can introduce interferers in the receiver's downconverted *I* and *Q* baseband channels. Presence of these interferers has a profound impact on the dynamic range of the ADC. Varying bandwidths in *I* and *Q* baseband channels requires adaptive anti-aliasing filters. Currently no elegant solution exists to notch these interferers and dynamically vary the bandwidth of the anti-aliasing filter.

In this paper, we propose a CMOS based state variable filter whose response can be digitally controlled. This technology offers a solution to the problems identified earlier and enables the development of a CMOS receiver that can be provisioned to select any channel from 400 MHz to 6 GHz.

2. STATE VARIABLE FILTER

In order to realize the programmable analog channel select filters, a state variable approach is employed [8]. State variable filters were chosen due to their controllability and observability with relatively less complexity in system implementation. Consider an *n*-th order transfer function, given by

$$T_{mn}(s) = \frac{b_m s^m + b_{m-1} s^{m-1} + ... + b_0}{s^n + a_{n-1} s^{n-1} + ... + a_0}, \quad (n \geq m) \qquad (1)$$

The above equation can be decomposed by partial fraction expansion into the sum of the first-order forms in Eq. (2), with each *i*-th form represented by a pole (p_i) and a residue (R_i). These values can be real or complex, with complex terms appearing with their conjugates.

$$T_{mn}(s) = \sum_{i=1}^{n} \frac{R_i}{s - p_i} \qquad (2)$$

The idea is that the overall transfer function $T_{mn}(s)$ in Eq. (1) can be realized by each term in Eq. (2) separately. The real pole/residue pairs can be realized by the first-order canonical block, as shown in Fig. 1. For the complex pole residue pairs, the conjugate pairs can be combined, which leads to a second-order system in Eq. (3). Fig. 2 illustrates the second-order state variable form.

$$T(s) = \frac{R_i}{s - p_i} + \frac{R_i^*}{s - p_i^*} = \frac{b_2 s^2 + b_1 s + b_0}{s^2 + a_1 s + a_0} \qquad (3)$$

where all the coefficients (a_i's and b_i's) are real hence realizable. As a result, any n-th order transfer function can be represented by combination of the first- and second-order canonical blocks. In other words, the overall transfer function $T(s)$ can be realized by summing the outputs of the first- and second-order, as presented in Fig. 3.

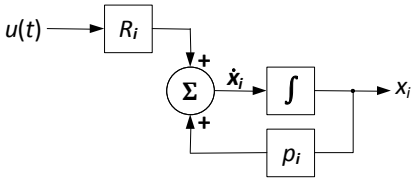
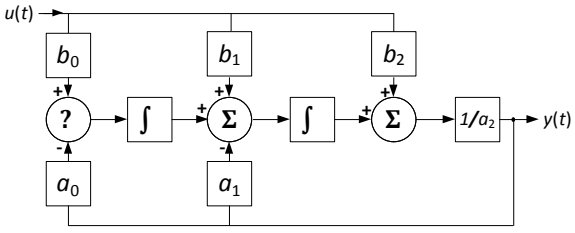
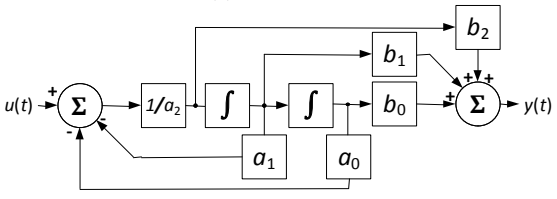


Figure 1 First-order state variable form



(a) Observer form



(b) Canonical form

Figure 2 Second-order state variable forms

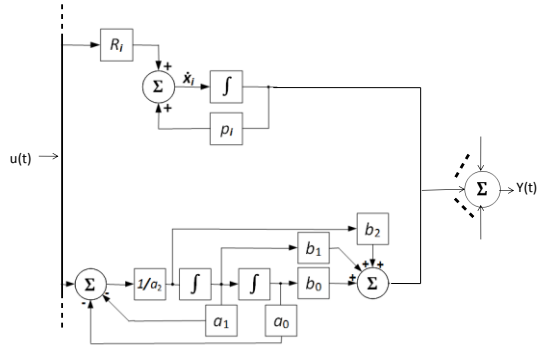
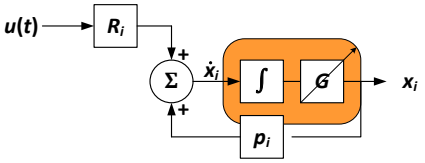


Figure 3 Realization of the overall transfer function in Eq. (2)

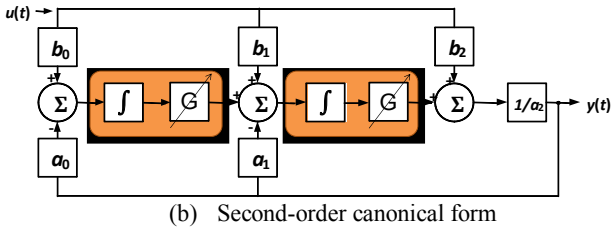
Therefore, the system in Fig. 3 can implement any desired filter. The coefficients (a_i's and b_i's) determine the characteristics of filters that include shape, bandwidth, and center frequency. These coefficients can be determined and optimized under software control. Note that the signal processing in the path is purely analog and is thus performance is not encumbered by the constraints of ADC and other digital circuitry.

3. FREQUENCY AGILITIES

It can be shown that, by appending a gain stage (G) to the integrator in the canonical blocks above, it is possible to reposition the center frequency of the filter over GHz of bandwidth to a specified location in the frequency band without altering other filter characteristics. This "frequency agility" combined with the state variable approach described in the previous section allows for the provisioning of any arbitrary filter of specifiable bandwidth and center frequency. The frequency-agile first- and second-order canonical blocks are shown in Fig. 4.



(a) First-order canonical form



(b) Second-order canonical form

Figure 4 Frequency-agile blocks

The analysis behind frequency agility is that, in the Laplace domain, the integrator behaves as $1/s$ and the gain stage simply as G. Thus, the integrator-gain stage, shown in the shaded blocks in Fig. 4 behaves as G/s. The gain stage essentially acts as a frequency scale as $T(s)$ is replaced by $T(s/G)$.

4. PROGRAMMABLE CHANNEL SELECTION FILTER

The main idea is to start with a prototype lowpass filter which has a cutoff at, say, f_{c0} Hz. Suppose this filter has n poles, p_i (i = 1, …, n) and the corresponding residues are R_i (i = 1, …, n). The transfer function of such a lowpass filter can be expressed in the form of Eq. (2). The corresponding impulse response is given by

$$h(t) = \sum_{i=1}^{n} R_i \exp(p_i t). \tag{4}$$

Now let f_c and W be the center frequency and bandwidth of the desired channel selection filter, respectively. As presented in Eq. (5), the transfer function is a lowpass filter with a cutoff frequency of $W/2$ Hz.

$$T_1(s) = T\left(\frac{s}{W/2f_{c0}}\right) \tag{5}$$

Let $h_1(t)$ be the impulse response corresponding to $T_1(s)$. With $\alpha = W/2f_{c0}$, it can be shown that

$$h_1(t) = \sum_{i=1}^{n} \alpha R_i \cdot \exp(\alpha p_i t). \tag{6}$$

Now, consider a "modulated" version of such a filter, that is, a filter whose impulse response is defined by,

$$h_{CS}(t) = h_1(t) \cdot \cos(2\pi f_c t) \tag{7}$$

Clearly Eq. (7) represents a bandpass filter centered at f_c and with a bandwidth of W Hz, i.e., the desired channel selection filter. Using Euler's formula, the equation can be rewritten as,

$$\begin{aligned} h_{CS}(t) = &\sum_{i=1}^{n} \frac{\alpha R_i}{2} \exp\left[(\alpha p_i + j2\pi f_c)t\right] \\ &+ \sum_{i=1}^{n} \frac{\alpha R_i}{2} \exp\left[(\alpha p_i - j2\pi f_c)t\right] \end{aligned} \tag{8}$$

We can see that this filter has $2n$ poles of the form $\alpha p_i \pm j2\pi f_c$ with corresponding residues $\alpha R_i/2$, which can be implemented using the state variable structure, described in the previous sections.

5. EXAMPLE

Let the desired channel selection filter has the following specifications:

- center frequency of 2 GHz
- bandwidth of 10 MHz
- passband ripple of 0.1 dB
- stopband attenuation of 40 dB

We can start with a 7th-order lowpass elliptic filter that has a cutoff frequency of 1 Hz and the same passband ripple and stopband attenuation. Its poles and residues can be easily obtained, for example, as presented in [9]. Fig. 5 shows its magnitude response whereas Fig. 6 shows the pole plot. Following the derivation in Sec. 4, poles of the desired channel selection filter can be easily obtained and they are shown in Fig. 7 and Fig. 8 (zoomed-in view). The corresponding magnitude response is presented in Fig. 9.

With the technique described in Sec. 3, this filter can be easily swept across the frequency range of interest by varying the gain block as shown in Fig. 4, provided the integrator has sufficient gain (greater than 0 dB). For example, Fig. 10 shows an integrator implemented in 65nm SOI technology. This integrator behaves as K/s in the range of interest (from 400 MHz to 6 GHz), with $K = 1.16\times10^{11}$ rad/s. The gain value can be preset to 0.2 for the above channel selection filter. The corresponding coefficients are listed in Table 1. With such a setup, Fig. 11 to Fig. 13 shows the magnitude responses of the system when the gain is set to 0.05, 0.5, and 1.0, respectively (without changing the coefficients). They correspond to channel selection filters centered at 500 MHz, 5 GHz, and 10 GHz, respectively.

Table 1 Coefficients of the 7th-order elliptic channel selection filter with gain value preset to 0.2

block#	*b1*	*b0*	*a1*	*a0*
1	0.02427822	-0.01857155	0.00007827	0.28959110
2	0.02427822	0.01866828	0.00007827	0.29255610
3	0.06474789	0.10032385	0.00035387	0.28968241
4	0.06474789	-0.10078147	0.00035387	0.29246440
5	-0.55428748	-0.14218417	0.00100573	0.29005181
6	-0.55428748	0.14212537	0.00100573	0.29209391
7	1.00000000	0.00080119	0.00160237	0.29107235

6. CONCLUSION

The theory and analyses described in this paper have extensive applicability to software defined radio. The programmable channel selection filter detailed in the

previous sections removes the need for redundant fixed bandpass filtering at the receiver front end. When realized in submicron CMOS and combined with a wideband synthesizer [8], this technology allows for filtering and down-conversion of signals of arbitrary bandwidth and center frequency in the range of 400 MHz to 6 GHz, which covers current and future cellular, GPS, Bluetooth, WiFi, WiMAX and LTE bands. Such a CMOS implementation will be extremely power efficient and very low cost.

7. REFERENCES

[1] S. Zhong, C. Dolwin, and R. Burgess, "A software defined radio proof-of-concept demonstration platform," *Proc. SDR 2006 Tech. Conf. and Prod. Exposition*, 2006.

[2] A. Berg, *Is the Smartphone Dead?* WirelessWeek, May 2009.

[3] B. Farhang-Boroujeny, and G. Mathew, "Nyquist filters with robust performance against timing jitter," *IEEE Trans. Signal Proc.*, vol. 46, pp. 3427-3431, Dec. 1998.

[4] P. B. Kenington, "Power Consumption of A/D Converter for Software Radio Application," *IEEE Trans. on Vehicular Tech.*, vol. 49, no. 2, Mar. 2000.

[5] W. Kester, *Data Conversion Handbook*, Analog Devices Inc. Engineering, 2004.

[6] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, Wiley-IEEE Press, 2005.

[7] P. Sangam, "Wireless broadband evolution," *Presentation made at Interop*, Las Vegas, May 2009.

[8] D. Gupta, et. al., "Interference detection and rejection in ultra-wideband RFID systems," *IEEE Int'l Conf. on Ultra-Wideband*, Hannover, Germany, Sept. 2008.

[9] A. Williams and F. Taylor, *Electronic Filter Design Handbook, 4th Ed.*, McGraw-Hill, Inc., 2006.

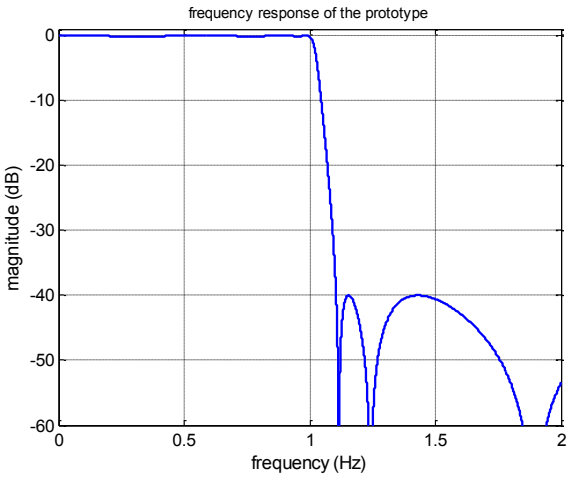


Figure 5 Magnitude response of the prototype LPF

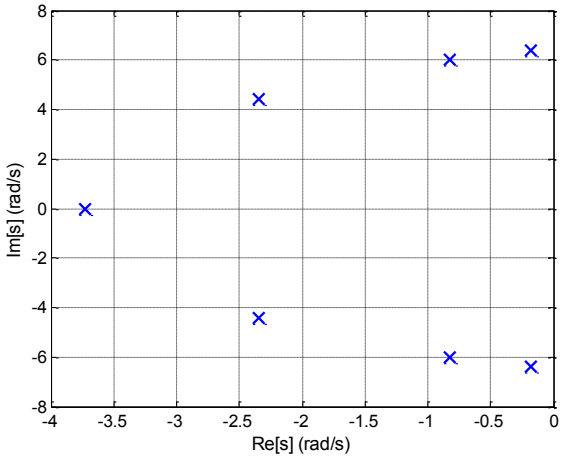


Figure 6 Pole plot of the prototype LPF

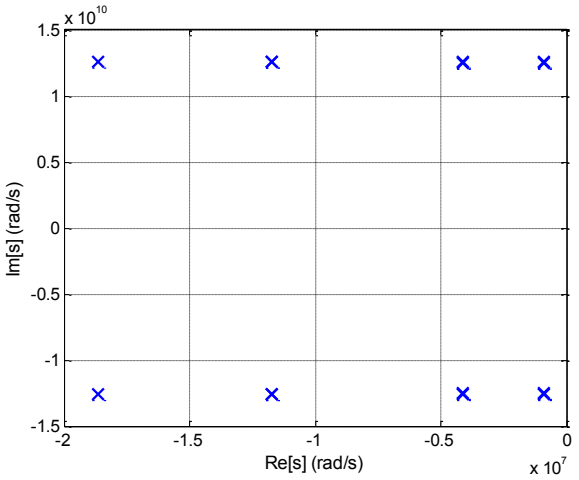


Figure 7 Pole plot of a channel selection filter centered at 2 GHz

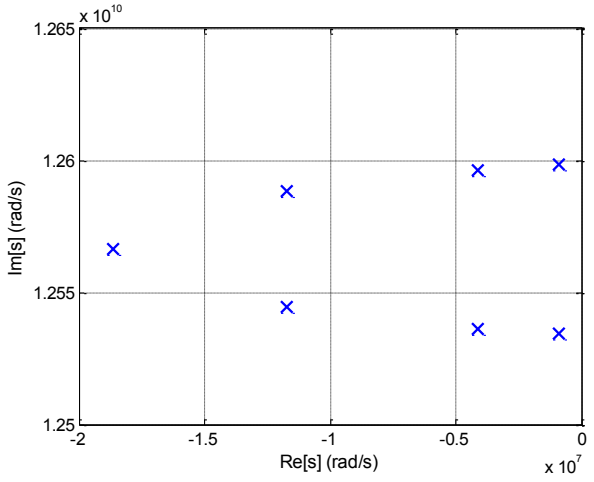


Figure 8 Zoomed-in view of Fig. Figure 7

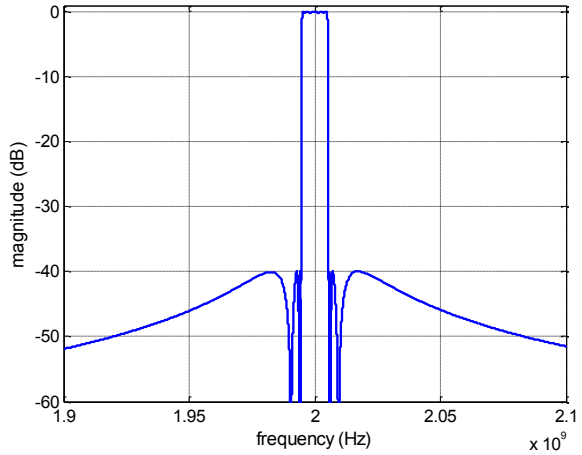


Figure 9 Magnitude response of a channel selection filter centered at 2 GHz

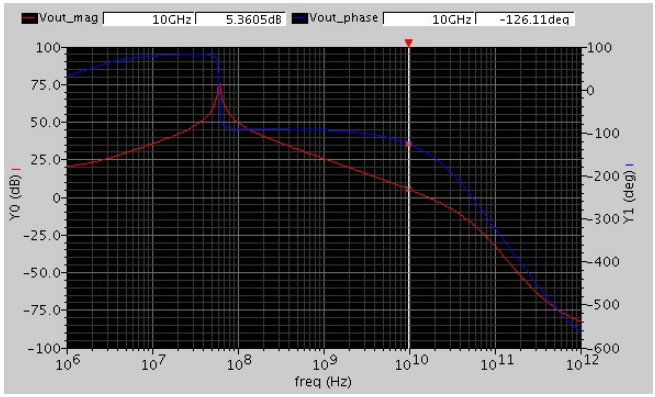


Figure 10 Frequency response of an integrator implemented in 65nm SOI technology

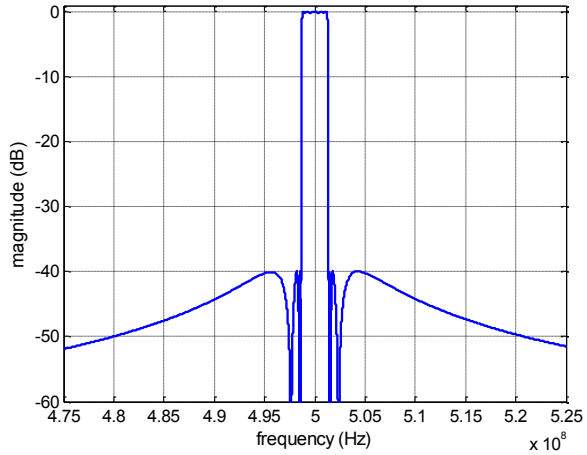


Figure 11 Magnitude response of the channel selection filter with $G = 0.05$ (centered at 500 MHz)

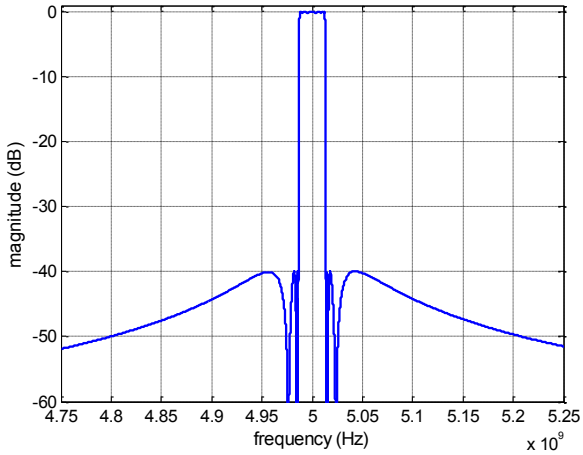


Figure 12 Magnitude response of the channel selection filter with $G = 0.5$ (centered at 5 GHz)

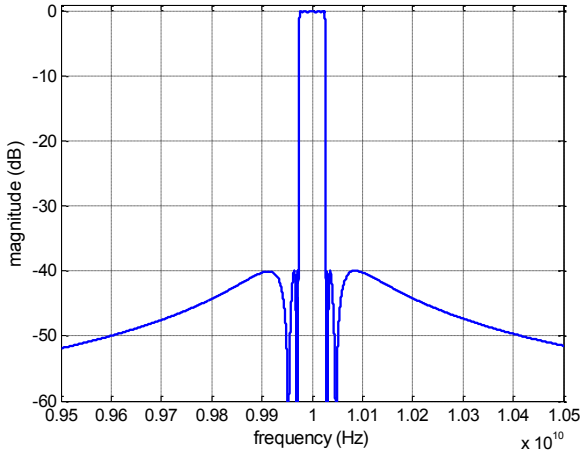


Figure 13 Magnitude response of the channel selection filter with $G = 1.0$ (centered at 10 GHz)