AN "RF AWARE" SOFTWARE DEFINED RADIO DESIGN AND VERIFICATION METHODOLOGY

Frank Ditore, Greg Jue, David Leiss
Agilent Technologies Inc.

ABSTRACT

Design goals and development schedules make simulation an essential tool in the development of new communication systems and SDR waveforms. For today's radios, this means the simulation must be able to model the mixed-domain design of the waveform PHY so that baseband impairments can be examined together with accurate RF impairments modeled both behaviorally and at the circuit level. Additionally, links between waveform simulation and physical test can greatly facilitate the implementation of the simulated waveform design in hardware.

In this paper we will explore an improved waveform design and verification methodology that combines simulation and modeling of baseband algorithms together with the RF block and circuit models. We will also discuss the implementation and verification of baseband algorithms in FPGA using this methodology along with combining measurement domain impairments of the FPGA with RF block level simulations.

1. INTRODUCTION

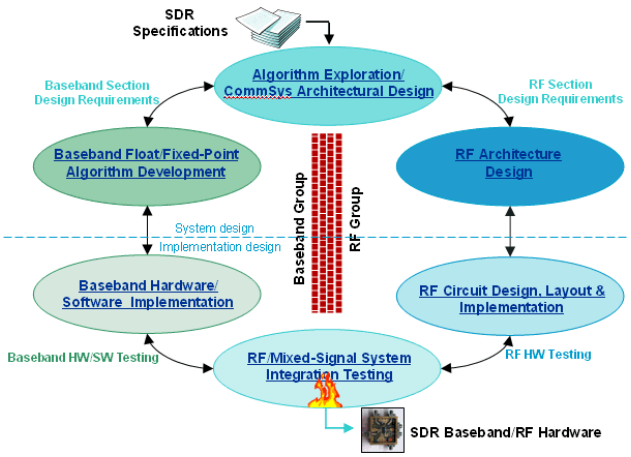
Today's Software-Defined Radio (SDR) physical layer development poses a multitude of challenges, as a result of the RF/mixed-signal nature of SDR designs. These challenges include:

- RF and baseband hardware teams may be using disconnected design and verification tools, making it difficult to collaborate and introducing system integration risks.
- RF engineers require baseband physical layer waveforms to begin RF designs (for example, Mobile WiMAX™), which can delay the RF design process.
- It can be difficult to evaluate baseband algorithms with RF field scenarios (for example, multipath fading, RF interferers, and so on) without building specialized RF hardware or real-world field-testing.
- Dependencies between the baseband and RF sections make it difficult to diagnose and isolate issues found during system integration.
- Disconnected design and test flow introduces schedule and integration risks when transitioning from simulation to hardware testing.

This paper discusses how an "RF-aware" SDR design and verification methodology can to help address these issues.

2. DISCONNECTED BASEBAND/RF DESIGN AND TEST METHODOLOGIES

SDR development projects may involve several design teams working in parallel to meet a hardware deliverable schedule objective. Figure 1 is an example of an FPGA design team and an RF design team, both working in parallel with different design and verification tools, design and test methodologies, and often using significantly different terminology when trying to communicate concepts and concerns with one another. These differences are significant and can result in a "divide" in how these two



teams interface with one another and can introduce inefficiencies and integration risks in the design process.

Figure1 – The baseband/RF "divide."

3. COMBINING FPGAs AND RF IN AN INTEGRATED RF/MIXED-SIGNAL SIMULATION ENVIRONMENT

The ability to simulate baseband and RF designs together in an integrated Electronic System Level (ESL) simulation environment can help mitigate risks and improve design efficiencies by closing the "divide" between the baseband and RF design teams. Bringing these two disparate design methodologies together can also help identify potential system integration issues early in the design cycle, where they are easier to resolve.

FPGA engineers writing HDL code typically use HDL simulators to develop and test their code. The design is text-based and the FPGA engineer typically uses static test vectors to verify the input/output functionality of the digital design. Design performance simulation or optimization is typically not evaluated using dynamic test vectors that mimic real-world signaling scenarios.

Conversely, RF engineers designing RF systems and circuits typically use RF system and circuit simulators for their designs. The designs are schematic-based and the RF engineer is typically evaluating dc bias, linear or power-dependent S-parameters, spectral performance, RF power and linearity (for example, 1 dB compression, 3rd order intercept), and modulated signal performance such as Error Vector Magnitude (EVM) and Bit Error Rate (BER). RF engineers don't often consider the interaction between their designs with other baseband signaling or control functions, leaving this type of evaluation for final hardware integration.

These differences between the FPGA and RF domains highlight the need for a more integrated approach to SDR RF/mixed-signal system verification.

RF/mixed-signal Electronic System Level (ESL) simulators, such as the one shown below, enable RF designs and HDL code to be co-simulated together in a single integrated simulation environment to verify or optimize the system-level performance.

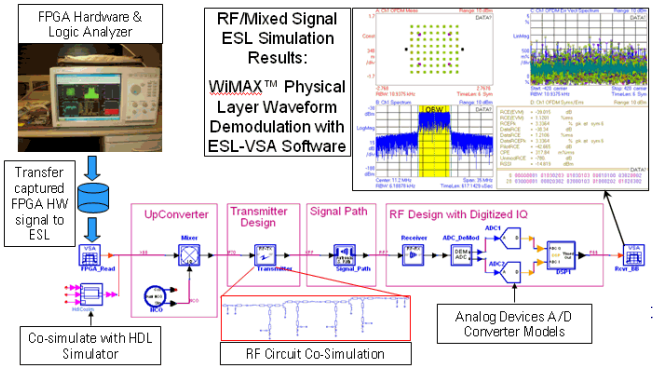


Figure2 - Integrated RF/Mixed Signal ESL system simulation with HDL and RF circuit co-simulation, and VSA software.

With this approach, FPGA engineers can use their preferred HDL simulators and design methodologies for development while utilizing these same simulators for simulation of system integration via this higher-level framework. Similarly RF engineers can use schematic-based simulation tools for development and retain the ability to instantiate their RF designs in this same higher level framework. The System Engineer or System Architect can then integrate the baseband and RF designs together for system-level verification by co-simulating the HDL and RF together in the RF/mixed-signal ESL environment.

If the FPGA has already been implemented, the FPGA hardware output signal can instead be captured with a Logic Analyzer and brought into the ESL simulation environment as a simulation signal source, rather than co-simulating with the HDL code.

The SDR RF/mixed-signal simulation design in Figure 2 is an example that consists of an RF upconverter/transmitter, channel model, and RF downconverter/receiver. The analog IQ is digitized with Analog Devices Inc. (ADI) analog-to-digital (ADC) converter simulation models. The simulation results are being measured and analyzed with a lab quality Vector Signal Analyzer (VSA) software application that is linked in the ESL simulation environment. This enables the SDR's RF/mixed-signal performance to be evaluated with instrument-like functionality in the ESL simulation environment, and helps to minimize unwanted surprises in transitioning from design-to-test. The VSA simulation measurement results show the Mobile WiMAX™ demodulation results of the physical layer waveform. Note that the simulation measurement results include both baseband and RF design impairments being modeled.

4. COTS WAVEFORMS

It can be useful for the ESL tool to include a library of Commercial-Off-The-Shelf (COTS) physical-layer waveforms to support parallel RF/baseband SDR development and performance verification. This enables the RF design and verification process to proceed independently of the baseband design process, which can help overcome bottlenecks and schedule dependencies.

For example, if designing to the IEEE 802.16e standard, an ESL COTS waveform source could be used to accelerate the RF design process, so that it can progress in parallel with the baseband design process. An example is shown in Figure 3, where a WiMAX™ waveform source is passed into an RF receiver design, which downconverts and demodulates the input signal. The I and Q are digitized with Analog Devices ADC simulation models, and passed into the COTS WiMAX baseband receiver to measure the simulated BER performance of the receiver design.

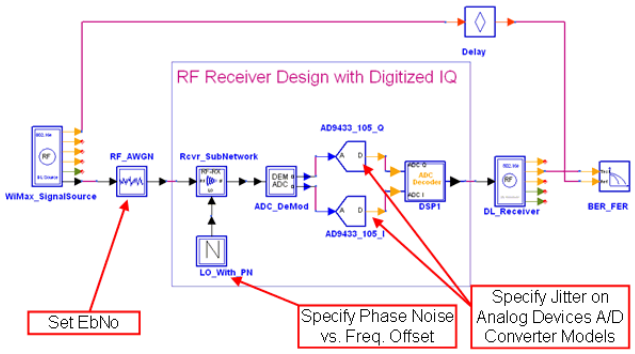


Figure 3 - WiMAX™ COTS waveform for SDR RF receiver design.

In this simulation the Eb/No is set with an AWGN element at the input of the receiver design. The phase noise of the LO, used to downconvert the RF signal, as well as the ADC jitter are swept. The results of the two simulations are shown below.

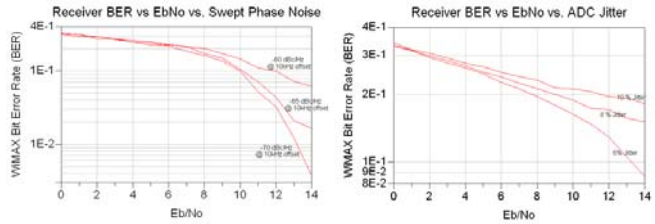


Figure 4 - SDR RF Receiver Simulation Results- BER versus Phase Noise (left) and BER versus ADC Jitter (right)..

The left plot in Figure 4 shows the 64 QAM WiMAX™ BER results versus swept LO phase noise at -60 dBc/Hz, -65 dBc/Hz, and -70 dBc/Hz at a 10 kHz frequency offset.

The right plot in Figure 4 shows the 64 QAM WiMAX™ BER results versus swept analog-to-digital converter (ADC) model jitter at 6%, 8%, and 10% jitter, where jitter corresponds to percent jitter of the 44.8-MHz clock period.

RF Receiver interoperability with other COTS waveforms can be conveniently be verified by replacing the WiMAX™ COTS ESL source/receiver with other existing COTS ESL libraries for LTE, WCDMA, WLAN, GSM/EDGE, and so on.

Similarly, having access to multiple COTS waveforms gives the design engineer (both baseband and RF) the ability to create complex and varied interference, jamming, and threat waveforms.

5. SDR INTEGRATION TESTING

SDR testing presents its own set of challenges, and can further highlight the divide between FPGA and RF engineers. Integration issues found during system-level testing can be difficult to isolate and diagnose. An example is an SDR reciever which is not meeting it's sensitivity specification. It can be unclear whether the problem is a baseband issue or an RF issue. Performance issues that are dependent on both baseband and RF are difficult to isolate, and can lead to a process breakdown between baseband and RF teams unless there is a methodology to help diagnose issues.

Before discussing a methodology to diagnose integration issues in the testing phase, however, it is useful to discuss how system integration risks can be mitigated early in the design phase where they are easier and more efficient to resolve.

Figure 2 shows an example of mitigating risk by using Vector Spectrum Anlyzer (VSA) instrumentation software in the ESL simulation design tool. This can help minimize unwanted surprises arising from differences and uncertainties between ESL simulation and test instrumentation measurement algorithm discrepancies. The VSA software being used in the ESL simulation is also used as the interface front end for logic analyzers, RF signal analyzers, and oscilloscopes, providing consistent measurement algorithms and test continuity as the SDR development transitions from design to hardware test.

Another example of mitigating risk in the design cycle is shown in Figure 3, where the RF receiver design is evaluated indepent of the baseband design by using ESL COTS waveform sources and baseband receivers. The COTS sources and receivers perform the necessary coding/decoding to evaluate the RF receivers coded BER performance, independent of the baseband design.

This approach can be extended for SDR hardware testing, allowing RF hardware verification to be performed indepedently of baseband hardware. Simulated COTS waveform and receiver capability provides the baseband coding/decoding functionality necessary to perform coded BER measurements on RF/mixed-signal hardware as illustrated in Figure 5.

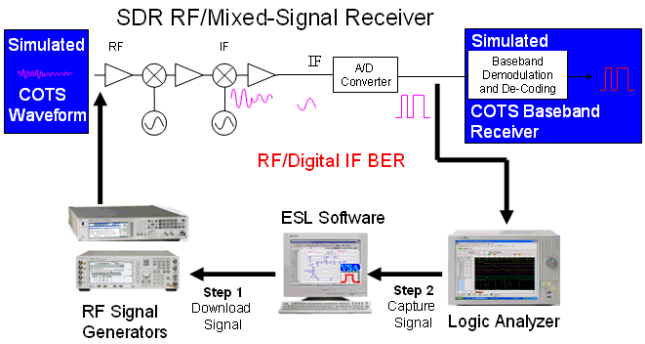


Figure 5 - Using ESL COTS waveform sources and receivers to test SDR RF/mixed-signal receiver hardware.

Using simulated ESL COTS capability with test instrumentation enables RF/mixed-signal hardware to be tested indepently of baseband hardware/firmware, and enables system integration issues to be isolated and diagnosed. There are a number of references available on the benefits and techical considerations in combining simulation and test. [1-5]

Conversely, it can be useful to use simulated ESL capability to represent RF functionality for RF/mixed-signal FPGA hardware testing.

An example is shown in Figure 6, where ESL RF simulation is being used inside of a logic analyzer to configure an "RF-Aware" FPGA test setup. Note that the ESL simulator has been installed in the logic analyzer as a separate application example and does not ship with the logic analyzer.

The WiMAX™ physical-layer waveform implemented in the FPGA is being being captured by the logic analyzer and is transferred into the ESL simulation environment in the logic analyzer for RF simulation processing. The RF simulation in the logic analyzer introduces a narrowband QPSK RF interferer to the WiMAX™ waveform to analyze interference effects. The interferer's amplitude can be seen as the red trace in the spectrogram (upper measurement). The narrowband QPSK interferer can also be observed in the spectrum plot (lower measurement), where it is superimposed on the wider bandwidth WiMAX™ spectrum. The interfering signal's power level and RF frequency can be varied to quickly evaluate the effects of both in-band and and out-of-band interference on the receiver's performance.

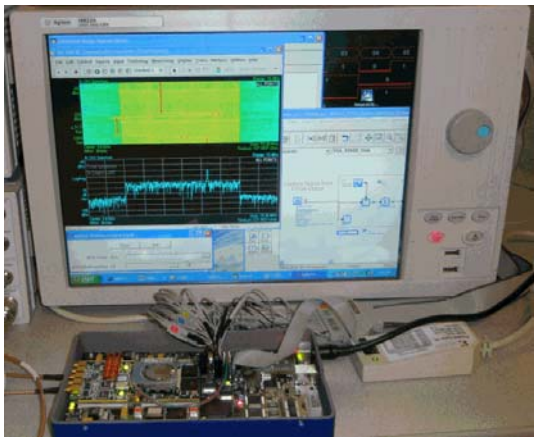


Figure 6 - “RF-Aware” FPGA test setup using RF ESL simulation inside the logic analyzer.

Another example of using an “RF-Aware” FPGA test setup is isolating and diagonsing an SDR receiver sensitivity issue by simulating the entire RF portion of the SDR design as an application on a logic analyzer, while simultaneously testing the FPGA connected hardware. The two separate technologies can be tested together while at the same time the waveform can be evaluated at the various points of the signal path to determine exactly where the problem is occuring.

6. SUMMARY

In this article we have discussed an improved SDR waveform design and verification methodology that combines RF and baseband modeling together in a single integrated ESL simulation environment for system-level verification. This integrated approach can serve as a catalyst for improved communications and collaboration between baseband and RF design teams. We have shown how ESL COTS waveform libraries can be used to help mitigate system integration risks early in the design cycle, and can help verify RF interoperability with various COTS waveforms. Lastly, we showed how combining ESL simulation and test instrumentation together can help in the system integration testing phase by using simulated COTS waveform to represent baseband functionality, and by using ESL RF simulation capability for “RF-Aware” FPGA testing.

10. REFERENCES

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