JITTER ANALYSIS OF TIME INTERLEAVED ADC/DAC SYSTEMS FOR SOFTWARE DEFINED RADIO (SDR) WITH PN SEQUENCE

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ABSTRACT

In the case of time interleaved ADCs (round robin sampling with multiple ADCs), timing jitter can create harmonics in the sampled signal. One potential way to deal with this is to intentionally jitter the sampling instances using a pseudo-random sequence to jitter the timing. The result is a signal that's non-uniformly sampled which could then be run through a simple filter/interpolating algorithm to reconstruct it without the added noise. This may lead to a method for compensating mismatches in the ADC array without the need for precise calibration of the individual ADC timing delays. A special ADC/DAC structure suitable for high-sample rate SDR based on time-interleaving, implementation issues, limitations, impairments and possible solution using PN sequence is presented. It is found that using PN sequence to mimic the jitter along with the uses of interpolator/filtering reduces harmonics.

1. INTRODUCTION

A software-defined radio (SDR) system is a radio communication system which uses software for the modulation and demodulation of radio signals. The hardware of a software-defined radio (SDR) typically consists of a super heterodyne RF front end which converts RF signals from and to analog IF signals, and analog to digital converter (ADC) and digital to analog converters (DAC) which are used to convert a digitized IF signal from and to analog form, respectively [1]. As SDR is suppose to accommodate multiple air interface, hardware used in the SDR requires some flexibility. They should be capable of handling different sample rates and resolutions, different dynamic ranges due to interference and noise. Designing appropriate ADC/DAC is very important for SDR as ADC/DAC block is sensitive as well as costly and making it adaptive to different scenario requires some serious thought. The focus of this paper is to explore a special ADC/DAC structure suitable for high-sample rate SDR based on time-interleaving, implementation issues, limitations, impairments and possible solution using PN sequence. A simulation based study is performed to analyze the jitter and possible reduction of harmonics using PN sequence.

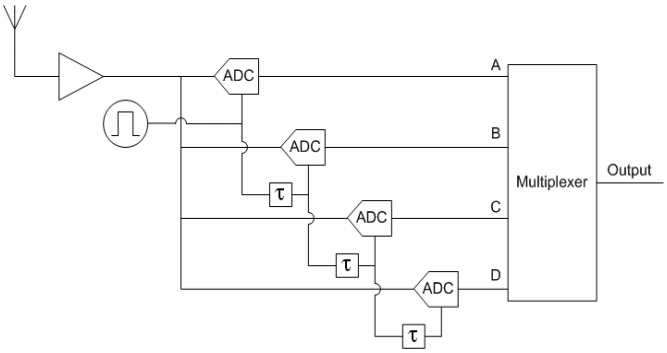

Figure 1: Time Interleaved Converter Array

2. TIME INTERLEAVED ADC ARRAYS

Time interleaving is a cost effective method to meet the demand for a converter with higher sampling rate. In [2], the concept of time interleaved array is first presented. Figure 1 shows schematic representation of a time interleaved converter array. In time interleaved converter approach, a number of lower cost converters with interleaved sampling times are used as if they are effectively a single converter operating at much higher sampling rate [2]. The time-interleaved ADC system works as follows:

i) The input signal is inserted to all the parallel ADCs.

ii) Each ADC works with a sampling period of MT_s, where M is the total number of ADCs present in the array, and T_s is the desired sampling period.

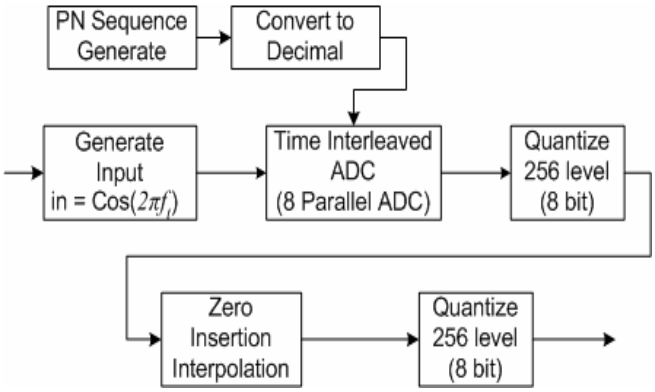

Figure 2: Block diagram of the interleaved ADC system

iii) The clock signal to the *i*th ADC is delayed with iT_s. This gives an overall sampling period of T_s.

Time interleaved converter array is a generic solution and this type of array can be used with any type of A/D converter. In practice, this is not generally used for narrowband signals as it creates spurious harmonics.

3. MISMATCHES OF TIME-INTERLEAVED ADC SYSTEMS

Time-interleaving an existing group of low-speed ADCs can multiply the sampling speed of a system, but it becomes a tricky and complex chore at higher sampling rate. Time-interleaved ADCs require precise control of ADC timing and consistent gain across the converters. The drawback with the time-interleaved ADC system is that, due to the manufacturing process, all the ADCs are not identical and mismatch errors occur in the system. Three kinds of mismatch errors occur which are timing mismatch, gain mismatch, and offset mismatch. In this paper, we will limit ourselves to timing mismatch only.

4. TIMING MISMATCH

The delay times of the clock between the different ADCs are not equal. This means that the signal will be periodically but nonuniformly sampled [6]. Two types of clock timing errors are found in time-interleaved ADCs – timing skew (systematic error) and timing jitter (random error). While timing jitter is unavoidable and random, timing skew can be modeled and compensated. For a full-scale-amplitude sinusoidal input signal, the maximum suggested signal-to-noise ratio (SNR) due to timing error can be written as

$$SNR_{dB(max)} = 20 \log_{10} [1/(2 \pi \ f_{in} \ \sigma_{jitter})]$$

Here f_{in} and σ_{jitter} respectively represent the input frequency and standard deviation. In the time domain, the envelope of the error signal is periodic with a period of M/f_s and shifted 90 degrees compared to the gain mismatch. In the frequency domain, noise signal is periodic with a period of M/f_s and noise spectrum peak can be written as

$$f_{noise} = f_{in} + (k/M)f_s \qquad \text{where } k = 1, 2, 3, \ldots$$

Here f_{in} and f_s respectively represent the input frequency and sampling frequency. Note that in time skew case, output signal power is inverse proportional with input frequency and total signal power and error at output is constant [3].

5. LITERATURE SURVEY ON ESTIMATION AND COMPENSATION OF TIMING ERROR

In this section, based on extensive literature survey, different approaches to deal with timing jitter are presented. In [4], a generic representation of digital spectrum for non-uniformly sampled signals is derived. Four special cases of sinusoid signal are presented in details. From the derivation, it is found that the spectrum of a non-uniformly sampled sinusoid has uniformly spaced line spectra and the power of all spectral components is summed up to one. It is also shown that the signal to noise ratio (SNR) found for this case has a closed form expression. In [4], this mathematical representation is also used to analyze the harmonic distortion introduced in time-interleaved ADC/DAC due to time-base error.

A robust sampling time offset estimation algorithm for time interleaved converters is presented in [5]. This estimation is based on analysis presented in [4] for non-uniformly sampled signals. Based on this time offset estimator a new waveform digitizer is presented. In the proposed scheme, input signal is digitized by digitizer and windowed by a Blackman-Harris window which is then followed by a DFT operation. The resulting DFT points are then normalized and their angles are extracted. A division of theses DFT points by test frequency results the timing offsets. The timing offsets then can be fed into the adjustable delay units to compensate timing jitter.

In [6], another method for estimating and compensating timing mismatch error in time interleaved ADC is presented. Unlike other Algorithms, this estimation method is blind and requires a prior knowledge of the input signal. It also requires that the input signal is band limited to the fold over frequency of the complete ADC system. It is noted that the method is continuous process and can estimate the error while the ADC is running. The method is adaptive to slow changes in the time errors.

6. JITTER ANALYSIS WITH PN SEQUENCE

Timing jitter creates harmonics in the sampled signal. One potential way to deal with this is to intentionally jitter the

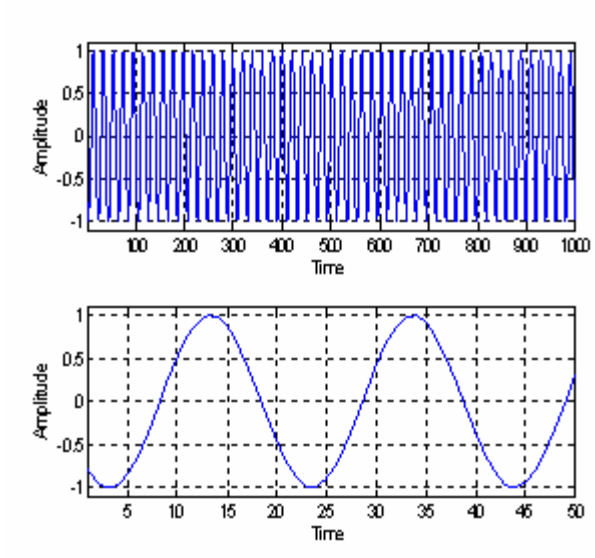

Figure 3: Input signal and zoomed version of input signal in time domain

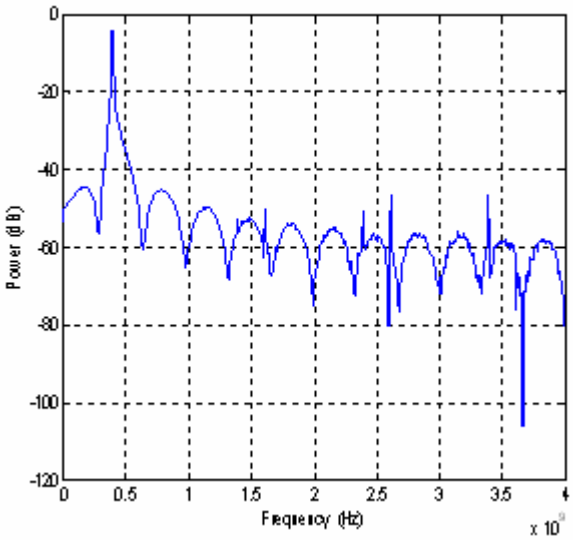

Figure 4: power spectral density (psd) of output of time-interleaved adc with jitter = 0 and skew (t_{adc}) = 0.1 shows harmonics

sampling instances using a pseudo-random sequence to jitter the timing. This will create a signal that is non-uniformly sampled. This non-uniformly sampled signal can be passed through a simple filter/interpolating algorithm to (hopefully) to reconstruct it without the added noise. This may lead to a method for compensating for mismatches in the ADC array without the need for precise calibration of the individual ADC timing delays.

7. PROPOSED SYSTEM ARCHITECTURE

In this section, the architecture of the time interleaved ADC system is presented. Figure 2 shows a block diagram of the system architecture.

Generate Input: A simple sinusoidal input is generated and fed to the time interleaved ADC.

Time interleaved ADC: Total 8 parallel digitizers are used in the system that digitize the signal. Timing jitter and timing skew can be controlled and are user selectable. The output of one ADC out of 8 is shown below.

$$V_{out} = G_x A \cos [\, 2\pi f_{in}\{(8m + n)\, T_s t + t_{adc} + t_{jitter}\}]$$

where G is the gain of ADC, A is sample amplitude, t_{adc} is timing skew and t_{jitter} is timing jitter.

Quantizer: Uniform quantizer is used here. The level of the quantizer is user selectable.

Interpolator: Interpolation is a process where the sample rate is increased. Zero insertion interpolator is used here which generates total 4 samples from one sample and thus increase the sample rate [1].

Filter: A root raised cosine (RRC) filter is implemented with a roll-off factor of 0.5.

PN Sequence Generator: A maximum length PN sequence generator was used whose length is variable or user selectable.

Binary to Decimal Converter: This block converts binary PN sequences to decimal value.

8. SIMULATION METHODOLOGY

A time interleaved ADC system is simulated in this study by varying different parameters. Total 8 parallel ADCs are used in the time-interleaved ADC structure with sample period $T_s = (1/8)*10^{-9}$. The input is a simple sinusoid with frequency of 393 MHz. A maximal length PN sequence with $L = 2^{15}-1$ is used to generate the pseudo-random jitter. PN sequence is converted to decimal value and multiplied by 10^{-12} before fed into ADCs. The quantizer has 256 levels (8 bit implementation).

At first the simulation of time interleaved ADC is performed without any mismatch, i. e. Jitter $t_{jitter} = 0$ and skew $t_{adc} = 0$.

Then the simulation of time interleaved ADC is performed with a specific timing skew, i. e. Jitter $t_{jitter} = 0$ and skew $t_{adc} = 0.1$ or 10%.

At last the simulation of time interleaved ADC is performed with a specific timing skew and with pseudo-random sequence, i. e. Jitter t_{jitter} = PN sequence and skew $t_{adc} = 0.1$ or 10%.

Distortion and harmonics are observed at the ADC output and at the Interpolator/Filter output.

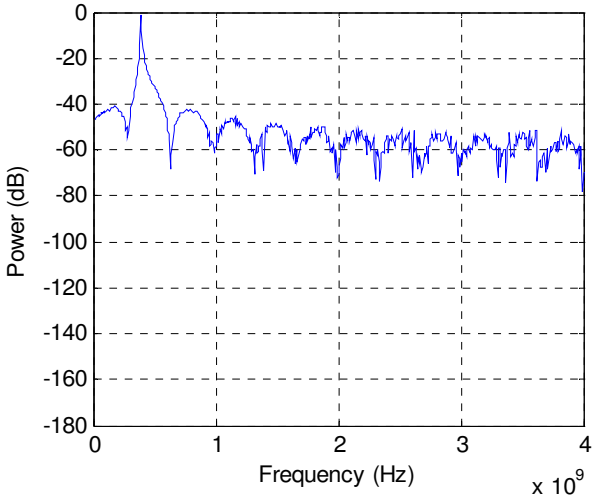

Figure 5: Power spectral density (PSD) of output of time-interleaved ADC with pseudo-random jitter and skew (t_adc) = 0.1 shows harmonics.

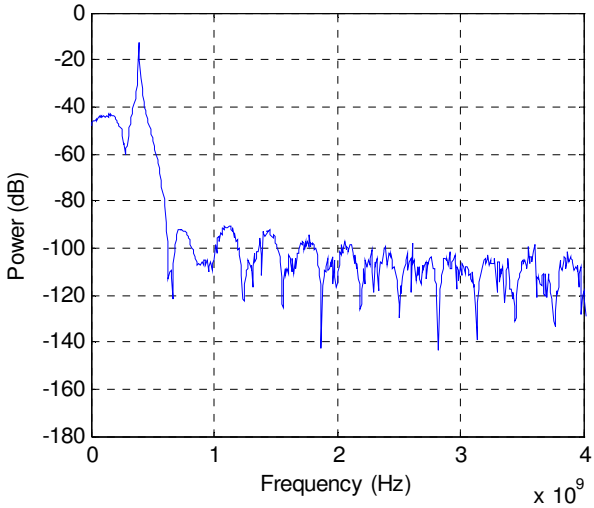

Figure 6: Power spectral density (PSD) of output of interpolator and RRC filter with pseudo-random jitter and skew (t_adc) = 0.1 shows harmonics with significant improvement.

9. RESULTS AND ANALYSIS

After simulating the time interleaved ADC, the jitter is analyzed and a reduction in the harmonics caused by this jitter is observed. Figure 3 shows the input signal which is a simple sine wave without any distortion or harmonics'. This input signal is then passed through time interleaved ADC and quantizer. Figure 4 shows the power spectral density (PSD) of output of quantizer and time-interleaved ADC with no jitter and 10% skew. It is noted that skew introduced harmonics'.

PN sequence based timing jitter is one way to analyze jitter. PN sequence is generated and inserted in ADC as pseudorandom jitter and the effect of using this PN sequence is then analyzed. Figure 5 shows the power spectral density (PSD) of the output of quantizer and time-interleaved ADC with pseudo-random jitter and 10% skew. This figure shows harmonics along with jitter as expected.

This distorted signal is passed through an interpolator and a low pass filter to cut off some distortion. Figure 6 shows the output of the filter which clearly shows reduction of harmonics' and distortion.

10. CONCLUSSION

The discussion presented in this paper provided insights into the time-interleaved ADC technique, covered the pros and cons of such designs, and provided valuable theory on the successful interleaving of multiple ADCs in a high-speed data-acquisition system. It is found that parallel processing can introduce higher noise and distortion. The types of noise and distortions and their effect are discussed. Interestingly these mismatches follow some specific pattern and can be determined and removed. Few innovative methods to compensate timing mismatch such as jitters are discussed.

11. REFERENCES

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