DEVELOPMENT OF AND INITIAL PERFORMANCE RESULTS FOR A SOFTWARE DEFINED ULTRA WIDEBAND RECEIVER

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ABSTRACT

The vast majority of today's Ultra Wideband (UWB) communication systems are composed of application specific hardware, and do not use SDR architectures. Several major challenges are involved in developing a UWB testbed—extremely high sampling rates, huge amounts of input/output data, tremendous amount of digital processing power, and developing broadband RF hardware. These challenges are particularly daunting when Commercially available Off-The-Shelf (COTS) components are used in the development of such a system. In this paper, we describe the development of a UWB SDR Transceiver Testbed based around an 8 GHz-8 ADC Time Interleaved Sampling array and a VirtexII-Pro FPGA. One of the primary issues with the Time Interleaved Sampling array is distortion introduced into the received signal as a result of ADC mismatches. Therefore, the paper also presents initial performance results for both narrowband and ultra wideband signals and indicate that acceptable system performance can be obtained even if the ADCs are only coarsely matched.

1. INTRODUCTION

Impulse UWB (I-UWB) signals have been an active area of research for a number of years, as these signals provide a variety of capabilities such as: precision ranging/position location, robustness to fading/interference, and the ability to capture significant amounts of multipath energy [1]. Currently, state-of-the-art UWB communication systems are composed of application-specific hardware, and do not use Software Defined Radio (SDR) architectures. The challenges involved in developing such as communication testbed—extremely high sampling rates, huge amounts of input/output data, and a tremendous amount of digital processing power—have been fairly daunting. These challenges become particularly poignant when Commercially available Off-The-Shelf (COTS) components are used in the development of such a system.

An SDR UWB receiver, however, provides tremendous flexibility over a fixed hardware implementation. Such a receiver has the capability of supporting multiple data rates, fully customizable modulation or multiple access schemes, can adapt to the propagation environment, and can operate with custom-designed waveforms. Additionally, the use of COTS components in developing a UWB SDR provides significant time and cost savings as compared to developing a custom integrated circuit.

This paper presents an overview of the development of a Software Defined UWB Communication System Testbed based around an 8-ADC/8 GHz Time Interleaved ADC array and VirtexII-Pro FPGA. The testbed is designed to operate at a maximum data rate of 100 Mbps at a range of 10 meters, has a DC – 2.2 GHz input bandwidth, and is a fully digital implementation capable of operating with a wide variety of broadband waveforms (WLAN, Bluetooth, CDMA, etc.).

This paper is organized as follows: Section 2 discusses an overview of the receiver architecture, in particular, both the RF Front End as well as the Digital Board. Section 3 presents performance results from the individual components, as well as the system as a whole. Finally, Section 4 summarizes the results in this paper and presents conclusions.

2. SYSTEM OVERVIEW

A basic block diagram of the receiver is given in Figure 1, and a detailed description is contained in [2]. Essentially, the receiver consists of an analog RF front end, the ADC array and clock distribution network, a Virtex II-Pro FPGA, and a USB 2.0 interface device. The RF front end utilizes several ultra-broadband amplifiers, attenuators, and filters and feeds the received signal to the ADCs.

2.1 RF Front End

One of the primary design objectives for the testbed was to create an extremely flexible, general-purpose system. Therefore, the RF front end consists of only the most basic elements: a transmitter/receiver switch, low noise amplifiers and filters, and a digital step attenuator. The purpose of the RF Front End is to amplify and condition the received signal (whether a UWB pulse or other waveform) for ADC

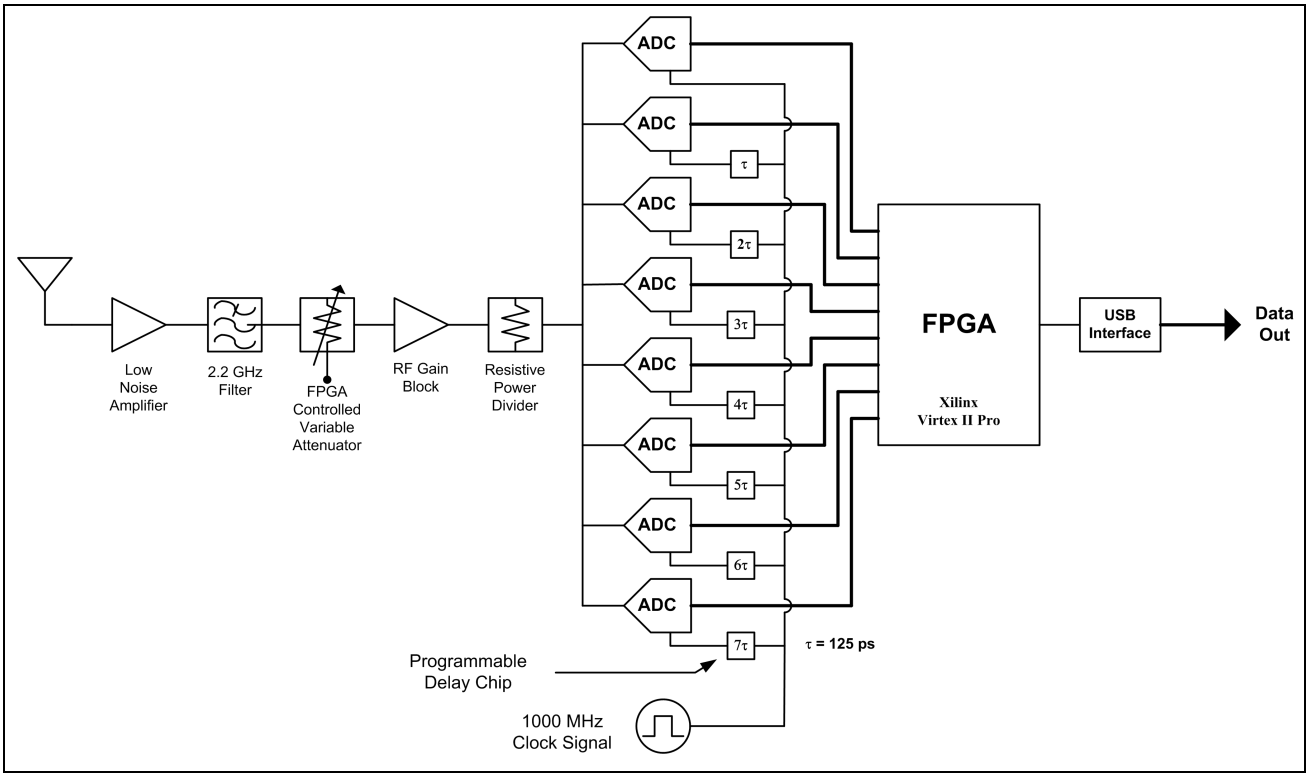


Figure 1: Block Diagram of the UWB Receiver

Table 1: Performance Summary of the RF Front End

Parameter	Predicted Performance	Actual Performance
Noise Figure	4.8 dB	9.0 dB
OIP3	25.0 dBm	25.4 dBm
Gain	40 dB	43 dB
Gain Flatness	± 2 dB	+20 / -0 dB
3 dB Bandwidth	20 – 2700 MHz	20 – 2200 MHz
Pulse Distortion	--	21 mV RMSE

conversion, while imparting as little noise or distortion as possible. To save cost and time, the RF front end was implemented with discrete COTS components, although a provision was included for a custom-designed RF board to be added at a later time. Both predicted performances (as a result of both analysis and simulations) as well as measured performance results for the RF Front End are summarized in Table 1. A primary design consideration for the RF front end was to provide enough gain to allow the receiver to operate at or near the desired 10 meter range while still preserving an approximately 40 dB dynamic range and minimizing the amount of distortion introduced into the received waveform. At a range of 10 meters, both a 2 GHz CW signal as well as a UWB signal will experience approximately 60 dB of free-space path loss [1]. The transmitter produces a UWB pulse with a peak power of +20 dBm. At the receiver, the MAX 104ADCs can tolerate a maximum input signal strength of 0 dBm, and the desired SNR of the TI ADC array is 40 dB [2]. To preserve the full dynamic range, therefore, it is important to keep the noise input to the ADCs equal to or less than -40 dBm. With a predicted noise figure of 4.8 dB, and a bandwidth of 2.7 GHz, the noise power input to the RF Front End is approximately -77 dBm, resulting in a maximum tolerable gain of around 37 dB. Unfortunately, the higher measured noise figure of 9.0 dB increases the noise power input to the receiver to -72 dB, and with 43 dB of gain, results in a noise power input to the TI ADC array of -30 dBm.

To minimize signal distortion, it was desired to maintain a flat frequency response and linear phase over the entire DC-2.2 GHz operating range of the receiver. Unfortunately, the amplifiers chosen for the RF Front End were optimized for narrowband signals, and deviated significantly from the nominal frequency response, as shown in Figure 2a. This deviation introduces the small amount of pulse distortion seen in Figure 2b.

2.2 Digital Board

One of the primary limiting factors when implementing an UWB or Ultra Broadband SDR are the extremely high sampling frequencies required to accurately reconstruct the received waveform. As an example, for a Gaussian pulse with a time duration of 500 picoseconds (resulting in a 3 dB bandwidth of approximately 2 GHz), meeting the Nyquist criteria to recover both inphase and quadrature components

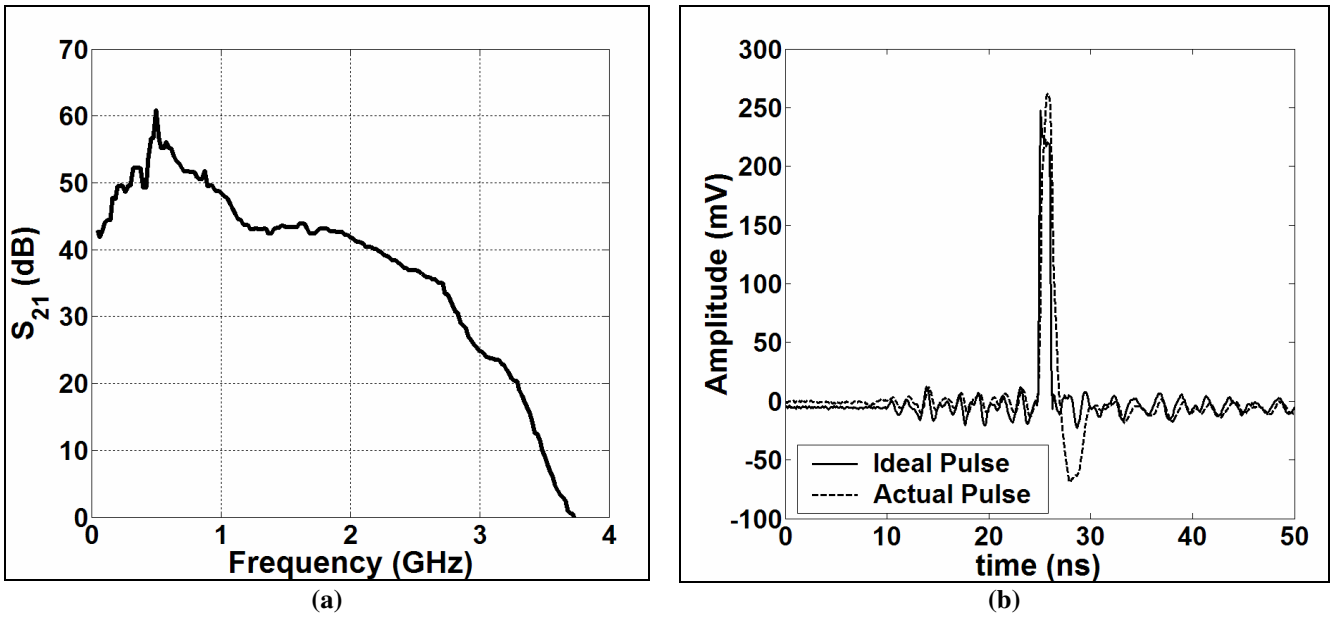


Figure 2: (a) Measured S-Parameter data from the RF Front End, and (b) Measured distortion of a UWB pulse imparted by the RF Front End—note slight amount of pulse broadening and dispersion.

requires a minimum sampling frequency of 8 GHz. Assuming 8 bits per sample, the receiver must process a 64 Gbps data stream in real time, a task only some of the most powerful ADCs, DSPs, FPGAs are capable of performing.

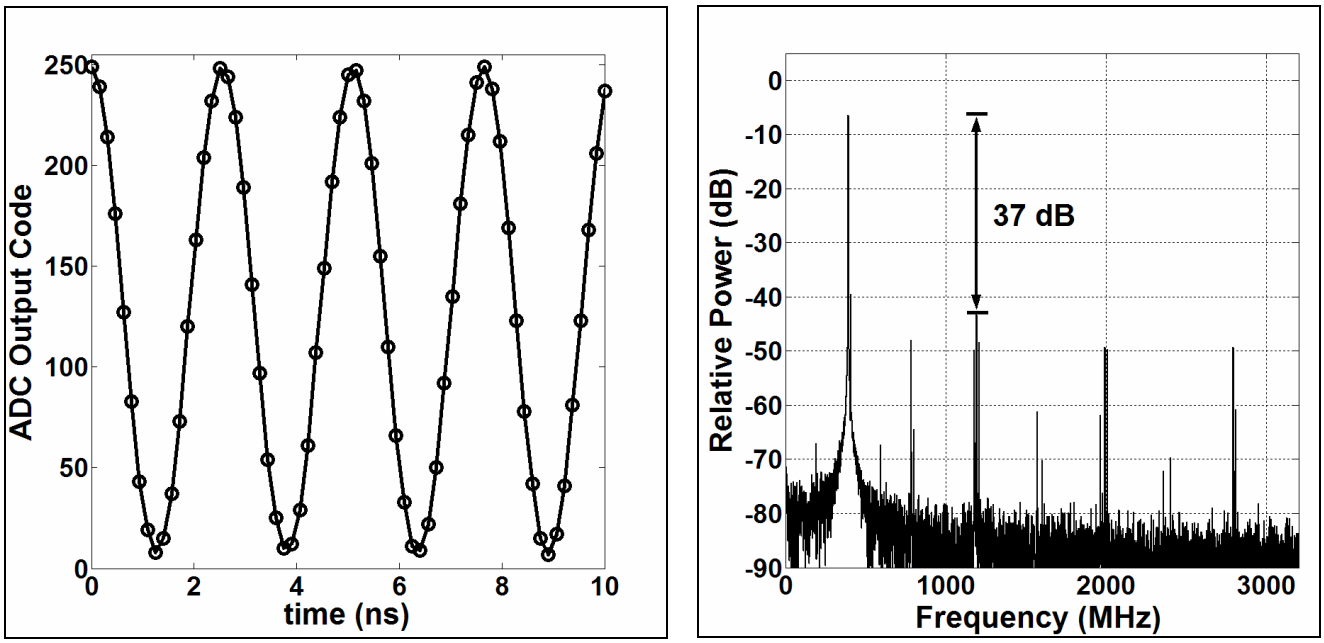
One technique that can be used to alleviate some of the difficulties involved in creating a digital UWB receiver is to make use of Time Interleaved Sampling (TI Sampling) [3-6]. TI Sampling makes use of an array of *N* lower sampling frequency ADCs to sample the received signal at different points in time in a round-robin fashion. Digital processing hardware can then de-interleave the samples, allowing the receiver to perform as if it used a single ADC operating at an effective sampling frequency of *N* times the individual ADC sampling rate. The performance of a TI Sampling array, however, is highly dependant on the precise matching of the individual ADC parameters, as mismatches can introduce significant distortion into the received signal [5, 6]. TI Sampling is advantageous in a COTS implementation as it significantly relaxes the requirements on the ADC and digital processing hardware, while hopefully maintaining the fidelity of the received signal.

The Digital Board consists of an array of $N = 8$ Maxim MAX104 ADCs, which have an analog input bandwidth of 2.2 GHz and a maximum sampling frequency of 1 GHz with 8 bits of quantization. Because the performance of the TI-Sampling technique is highly dependant on sampling the received signal at precisely spaced intervals [5, 6], ADC clock distribution was performed via a series of ON Semiconductor 10EP195 programmable delay chips, each of which has a delay resolution of ±10 picoseconds. A FOX Oscillator RFV300 low-jitter oscillator, along with careful attention to the design of the clock distribution network, resulted in an overall clock jitter of less than 10 picoseconds RMS.

The ADC samples are input to a Xilinx VirtexII-Pro FPGA for digital processing. The FPGA de-interleaves the ADC samples, performs data demodulation, along with any desired signal processing algorithms. Inputting ADC samples, deinterleaving them, and performing simple matched filter demodulation requires approximately 40% of the VirtexII-Pro P70's resources. Three RS-232 connections and one High-Speed USB connection interface the FPGA with a host computer.

3. PERFORMANCE RESULTS

Successful implementation of the UWB SDR Receiver requires very precise control over the ADC gain, offset, and–in particular–the timing mismatches. To evaluate the operation of the TI ADC array, the programmable clock delay chips for the ADCs were adjusted to provide an effective sampling frequency of 6.4 GHz, and an 800 MHz signal was input to the Digital Board. The 800 MHz clock signals were used in lieu of the full 1 GHz clock signals in order to speed the development and build time of the FPGA code [7]. Only a very coarse calibration of ADC timing offsets was performed, and no effort was made to compensate for gain or offset mismatches. An FPGA bitstream was then downloaded to the board which latched in data from the individual ADCs and stored them in BRAMs; a PowerPC program then read the data from the BRAMS, de-interleaved the ADC samples, and then transmitted the data to a host PC which saved it in a file.



(a) (b)

Figure 3: Time-Interleaved output of the Digital Board for a 393 MHz CW input at an effective sampling frequency of 6.4 GHz. (a) De-interleaved time domain output, and (b) Frequency spectrum of the de-interleaved output.

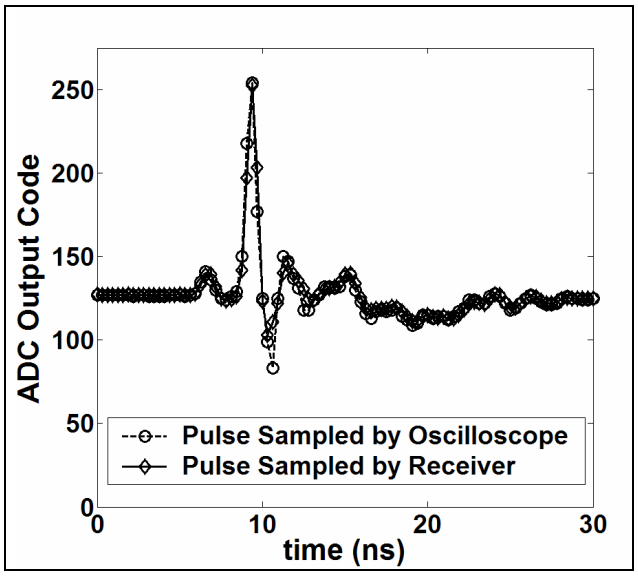


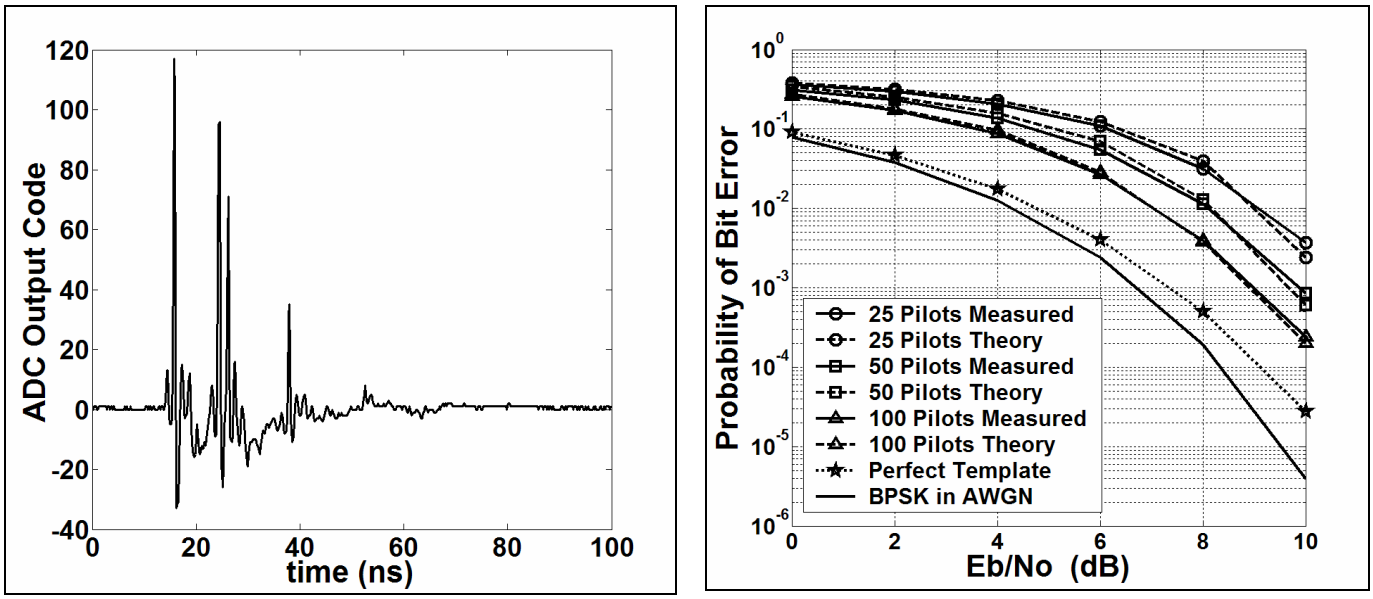
Figure 4: Comparison of a UWB pulse sampled by a Tektronix oscilloscope and the same UWB pulse sampled by the Digital Board. The sampling frequency for both the oscilloscope and receiver was set at 6.4 GHz. Note that the two pulses are nearly identical in both shape and time duration.

3.1 Reconstruction of CW Signals

For the first test, several CW signals at different frequencies were input to the digital board. An example waveform at 393 MHz, along with its spectrum, is shown in Figure 3. In the signal spectrum, note that several spurious signals are present. These spurs are primarily the result of slight imperfections in the ADC clock delays, which manifest as a distortion of the time domain signal as seen in the figures, as explained in [6, 8-9], however, the system still achieves nearly 40 dB of Spurious Free Dynamic Range.

3.2 Reconstruction of a UWB Signal

The second test for the UWB SDR Receiver was to see how accurately it could capture and reconstruct a UWB pulse generated by a simple MSSI pulser available in the MPRG lab. The pulser output was adjusted so that it would drive the full-scale ADC input range and was input to the Digital Board. For comparison purposes, the same UWB pulse was also digitized using a Tektronix TDS580D at a 10 GHz sampling frequency, and then resampled in Matlab to match the 6.4 GHz effective sampling frequency of the Digital Board. The voltage recorded by the oscilloscope was converted into an equivalent ADC output code level, based on the measured analog input range of the ADCs of ±250 mV. Both signals are plotted together in Figure 4. Note that the two pulses are nearly identical in both shape and time duration. The root mean square error between the two signals was computed to be 1.9% of the maximum pulse



(a) (b)

Figure 5: (a) Example received waveform as recorded by the UWB SDR Digital Board for the 10 MHz / 10 Mbps BER test, and (b) Bit Error Rate curves for various numbers of pilots using the Pilot Based Matched Filter Receiver and 2-PAM Modulation. The pulse/ data rate is 10 MHz / 10 Mbps, and the received signal consists of a LOS plus 3 multipath signals in AWGN.

amplitude, meaning that there is a negligible difference between the two pulses. Additionally, this experiment was performed for a large number of pulses over a duration of several months. It was found that the ADC mismatches did not vary significantly over this time duration, implying that not only are ADC mismatches non-time varying, but the proposed pilot-based matched filter is likely to be successful in mitigating the effects of ADC mismatches.

3.3 System Performance

The final test of the UWB SDR Receiver was to evaluate the bit error rate (BER) performance of the system as a whole. Impulse UWB transmissions generally operate in rich multipath environments, and may encounter significant time-varying pulse distortion; additionally, for the UWB SDR receiver, mismatches in the TI ADC array may introduce some distortion into the received waveform. Thus, implementing a traditional matched filter receiver (where *a priori* knowledge of the received pulse shape is required) is extremely challenging.

Fortunately, a pilot-based or transmitted reference receiver can be utilized to partially compensate for pulse distortion [10]. Essentially, N_P pilot pulses are added either at the beginning or the end of a data frame; these pulses are recorded by the receiver and then averaged together to form a template of the received signal. The pilot-based template can then be used as a noisy template for a matched filter operation.

To investigate the performance of the receiver, a simple test setup was created which consisted of a commercially available UWB pulse generator and a wireless channel emulator. The UWB pulse generator was configured to output an 800 picosecond duration UWB pulse at a 10 MHz pulse repetition frequency using pulse amplitude modulation. The output of the pulse generator was connected to the wireless channel emulator which created a line-of-sight pulse plus three multipath signals. The output of the channel emulator was then connected to the RF Front End of the UWB receiver, and the gain was set such that the received pulse amplitude equaled the full-scale input range of the MAX104 ADCs.

To more accurately evaluate the performance of the pilot-based matched filter approach, it was decided to use the receiver to capture the "raw" data bits and then perform demodulation in Matlab. The average energy per "raw" symbol was calculated, and AWGN was added in Matlab to vary the E_b/N_o. This approach allowed us to evaluate the pilot-based matched filter free from implementation specific effects such as synchronization error, clock jitter, or logic errors internal to the FPGA that may be specific to a particular receiver architecture. The BER results, along with the theoretical predicted values for a UWB pilot-based matched filter based on the expressions in [11], are shown in Figure 5. Looking at the figure, it can be seen that the measured BER values essentially match the theoretical predicted curve throughout the range of E_b/N_o evaluated.

Also plotted in the figure are the results from a test that was run using a "perfect" (i.e. noise-free) matched filter template composed of the average of all recorded pulses. Note that the curve from the "perfect" matched filter template does not exactly match the BPSK curve (which is the result that would be expected from the "perfect" matched filter template), but falls about 1 dB off the BPSK curve. The reason for the discrepancy is that ADC mismatches are introduced into all pulses independently; averaging the pulses to form a single template will reduce the impact of the mismatches but will not eliminate them completely. However, the fact that the perfect matched filter curve falls so close to the AWGN limit indicates that even with a relatively coarse calibration, the TI ADC array is introducing only a minimal amount of distortion into the received signal.

4. CONCLUSIONS

Systems that employ Impulse Ultra Wideband signals have been an important research area for a number of years. At the current time, nearly all commercially available UWB systems have been developed using custom-designed application specific hardware.

The UWB SDR testbed presented in this paper was developed with general-purpose commercially available off-the-shelf components, to ensure that users had full control over nearly all aspects of the receiver architecture and communication link. Additionally, the receiver is capable of supporting nearly any other form of broadband communications. To achieve such aggressive design goals, the receiver is based around a time-interleaved array of ADCs—allowing the receiver to perform as if it used a single 8 GHz effective sampling frequency with approximately 40 dB Spurious Free Dynamic Range (or roughly 6.5 – 7.0 Effective Number of Bits of quantization). While the TI Sampling process introduces distortion into the received signal, this distortion can be partially compensated for via the use of a pilot-based matched filter receiver architecture. Measured BER results showed excellent agreement with the theoretical predicted results, even though only a coarse system calibration was performed. As a result, the software defined ultra wideband receiver provides a platform that researchers can use to evaluate receiver algorithms, architectures, and theoretical models or simulation results.

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