LOW POWER SOFTWARE DEFINED RADIO DESIGN USING FPGAS

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1. ABSTRACT

Field Programmable Gate Arrays (FPGAs) are used to perform many tasks on a Software Defined Radio (SDR). To meet the performance and density needs of the newest SDR waveforms, FPGAs must be built using the latest silicon technology. The latest generation of 90nm FPGAs can meet the performance and density requirements, but power is a concern. In order to minimize the overall system power the impact the three types of power consumption (static, dynamic, and interface) needed to be evaluated. Static power consumption has become a leading factor when designing SDR systems. This paper will explore tradeoffs in system partitioning that result in the lowest overall power consumption. Areas to be evaluated include FPGA design techniques; FPGA and processor partitioning; interface standards; and multiple FPGA partitioning.

2. BACKGROUND

Power consumption of FPGAs is generally separated into three (3) categories: Dynamic power, static power, and interface (I/O) power. These power components are generally governed by the silicon process technology that is used to manufacture the FPGA. Traditionally, these three power components have maintained constant percentages of the FPGA's total power. In 130 nm and larger silicon processes, dynamic power has dominated the total power. In the current generation of 90 nm FPGAs, static power is becoming a more dominant power component. This fact must be considered when developing waveforms for these new technologies. This paper addresses low power design by challenging traditional design techniques.

3. POWER DEFINITION

Dynamic power is defined as the power consumed when signals are active (i.e. switching). This power is governed by the following equation:

$$P_{dynamic} = \left[\frac{1}{2}CV^2 + Q_{ShortCircuit}V\right] f \cdot activity$$

Where:

$P_{dynamic}$: Dynamic power consumption
CV^2: Capacitance charging component
$Q_{ShortCircuit}V$ = Short circuit charge during switching
f: Switching frequency
activity: Switching activity rate (i.e. toggle rate)

As can be seen above, the dominate factor in dynamic power is the frequency and toggle rate.

The static power is defined as the power consumed when no signal activity occurs (i.e. no switching). Static power is related to the size and configuration of the transistors that constitute the FPGA fabric. In an ideal world, CMOS transistors only draw power when switching. All static power in FPGAs is related to leakage of current inside the transistor. This is why static power is often synonymous with the term *leakage power*. There are three major components to static power:

1. Sub-threshold leakage from Source to Drain
2. Gate leakage
3. Reverse bias junction leakage

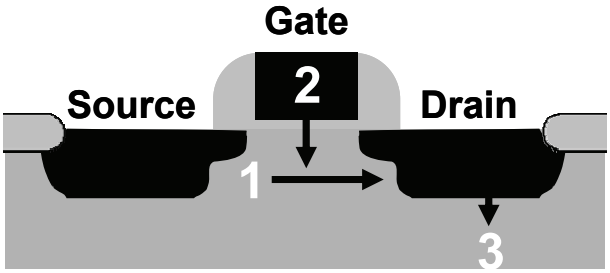


Figure 1: Transistor Leakage Contribution

Of these, '1' is the most dominant component to static power consumption. It should also be noted that static power is generally a product of silicon area. Thus, the smaller the FPGA, the less static power consumed. This fact will be exploited later in the paper.

The interface power is the power which is consumed by the I/O interfaces. The factors governing I/O power are similar to those of dynamic power consumption.

As with all architectures built on advanced processes, the contribution of the three power components has changed with new processes. With new process technology there is always a tradeoff in static power consumption versus performance. This is clearly shown in the tables below. In Table 1, the distribution of power is shown for performance optimized FPGA (Altera's Stratix family) at two process technologies. Table 2, shows the same information for the power optimized (Altera's Cyclone family) family. These tables represent the extreme cases of designs that use the maximum capabilities of the largest FPGAs in the families. As seen in the later

examples, static power is a dominant factor for handheld radio applications.

Table 1: Altera Performance Optimized FPGA (Stratix Family)

Power Component	Percentage at 130 nm	Percentage at 90 nm
Dynamic Power	81 %	66 %
Static Power	7 %	28 %
I/O Power	12 %	6 %

Table 2: Altera Power Optimized FPGA (Cyclone Family)

Power Component	Percentage at 130 nm	Percentage at 90 nm
Dynamic Power	54 %	64 %
Static Power	2 %	12 %
I/O Power	42 %	24 %

4. EXAMPLE WAVEFORM

The distribution of power in the above tables is a broad generalization. To understand the effects of these three power components, an example is needed. As an example a hypothetical waveform with the following characteristics will be used:

- Orthogonal Frequency Division Multiplexing (OFDM)
- Forward error correction (FEC) using Convolutional Coding
- Band-pass sampling (80 MSPS)
- Symbol rates of 10 MSPS
- User data rate of 10 Mbits/sec
- Duty cycle as follows:
  - 20 % Transmit
  - 20 % Receive
  - 60 % Standby

Figure 2 shows a block diagram of the example waveform. Obviously, there are components missing from the block diagram that would need to exist in a real waveform (Carrier/symbol recovery, interference cancellation, etc.). For the purposes of the following investigation, the discussion is limited to the blocks represented by the block diagram.

5. IMPLEMENTATION TRADEOFFS

When looking at the implementation of the example waveform, the goals must be defined. As the title of the paper suggests, the implementation goal is clearly the lowest power design.

5.1. Flat Implementation

At first it may seem that the lowest power implementation would be one that uses the lowest dynamic power. Implementing the design for lowest dynamic power requires that each block be designed to use lowest possible clock speed. In the case of the example waveform, the blocks would be operating at the data rate. These rates are shown as the top numbers in Figure 2. Table 3, lists the data rate and dynamic power consumption of each block. Using this *flat* implementation, it can be seen that the lower the data rate, the lower the dynamic power. However, dynamic power is only a part of the story. The resources required for the blocks in Table 3 will use an Altera Cyclone II FPGA with 70,000 logic elements. A breakdown of power consumption for the flat design implemented in a 2C70 is shown in Table 5.

Table 3: Dynamic Power for Flat Design

Block	Data Rate	Dynamic Power @ 85°C
Tx Digital Mixer	80 MSPS	134 mW
Interpolating FIR	80-MSPS	104 mW
Tx Channel FIR	20 MSPS	20 mW
IFFT	10 MSPS	21 mW
Convolution Encoder	10 MSPS	1 mW
Rx Digital Mixer	80 MSPS	134 mW
Decimating FIR	80-MSPS	104 mW
Rx Channel FIR	20 MSPS	20 mW
FFT	10 MSPS	21 mW
Viterbi Decoder	10 MSPS	14 mW

5.2. TDM Implementation

In Table 5, it can be seen that the flat implementation uses more static power than dynamic power. Static power does not contribute the overall computational efficiency of the waveform. A better approach would be to use the FPGA resources at their maximum capacity. This would minimize the number of design resources. A smaller design would allow the use of a smaller FPGA. The smaller FPGA would use much less static power.

Generally, digital designs can reduce area by re-using hardware resources. This comes at the expense of increased clock rate. This technique is generally referred to as *time-division multiplexing* (TDM). The blocks of the example waveform are ideally suited to take advantage of TDM techniques. Table 4 shows the data rate and dynamic power consumption of the example waveform implemented using TDM techniques. Notice that the clock rate of the all of the blocks is 160 MHz. This is a comfortable clock rate for Altera's Cyclone II FPGAs. The table also shows no need for separate transmit (Tx) and

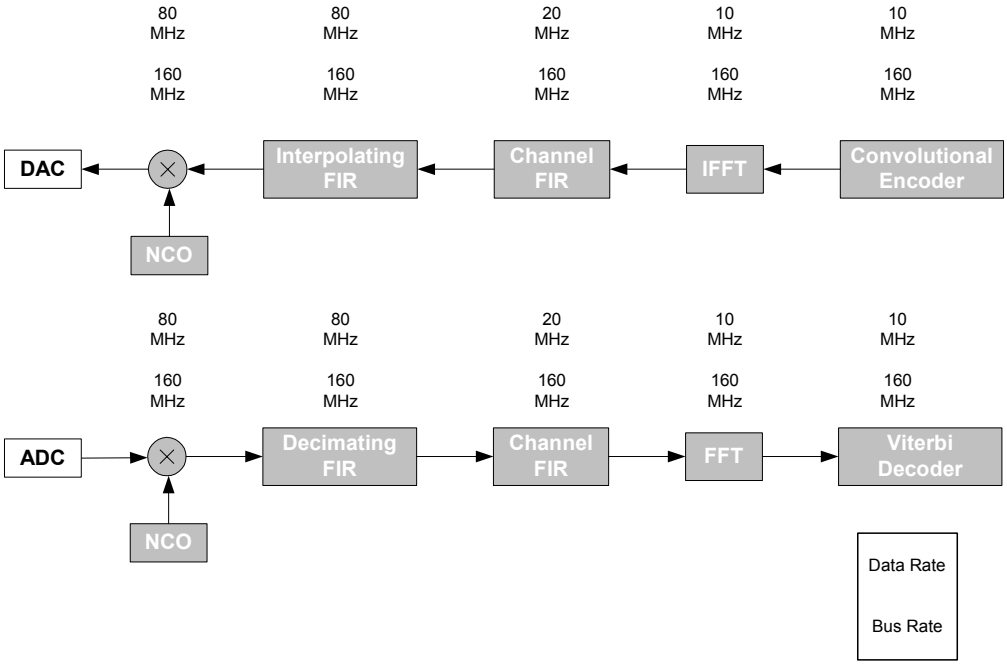


Figure 2: Example Waveform Block Diagram

receive (Rx) digital mixers. The digital mixers can also use TDM techniques to share between different paths in the waveform processing.

The 2C20 FPGA has a 3.8x reduction in static power. The dynamic power utilization of the TDM design is higher than the flat design. But when factoring in the static power, the total power is reduced by 30%.

Table 4: Dynamic Power for TDM Design

Block	Clock Rate	Dynamic Power @ 85°C
Tx Digital Mixer	160 MHz	134 mW
Interpolating FIR	160 MHz	56.46 mW
Tx Channel FIR	160 MHz	49.93 mW
IFFT	160 MHz	108.10 mW
Convolution Encoder	160 MHz	6.22 mW
Rx Digital Mixer	160 MHz	0 mW
Decimating FIR	160 MHz	56.46 mW
Rx Channel FIR	160 MHz	49.93 mW
FFT	160 MHz	108.10 mW
Viterbi Decoder	160 MHz	74.22 mW

5.3. Duty Cycle Effects

The previous sections compared the total power for a flat implementation and a TDM implementation of the example waveform. The TDM technique can reduce total power by 30%. If the duty cycle of the waveform is also included in the analysis, the power savings are even greater. The example waveform's duty cycle gives more weight to the static power of the FPGA. Using the 20/20/60 (Tx/Rx/Standby percentage) as outline in Section 4, Table 5 shows a power reduction of 53%. This is a significant power reduction for portable devices. The power savings translates directly into extended battery life.

In Table 5, a breakdown of the power for the TDM design is given. This version of the design can fit into a 20,000 logic element FPGA (Altera's Cyclone II, 2C20).

Table 5: Power Comparison of Design Implementation

Power	Flat Design (using 2C70) @ 85°C	TDM Design (using 2C20) @ 85°C
Dynamic Power	573 mW	643 mW
Static Power	606 mW	158 mW
Total Power	1181 mW	801 mW
Duty Cycle Power (Full Duplex)	478 mW	223 mW

6. INTERFACE CONSIDERATIONS

The previous sections outlined design techniques to tradeoff dynamic and static power. The interface power must also be considered. The choice of interface standard has a direct bearing on the power used. Table 6 shows the

interface power required to transmit 16 Gbps of data out of an FPGA using various interface standards. It is not surprising that using low voltage, low drive interfaces uses less power.

Table 6: Interface Power for 16 Gbps Throughput

Interface Standard	Number of pins	Power @ 85°C
3.3V, 24 mA	200	700 mW
LVDS (400 MHz)	20	662 mW
2.5V, 16 mA	200	443 mW
1.8V, 6 mA	200	205 mW

7. SUMMARY

Traditionally, waveform implementations reduced power consumption by focusing on a reduction of dynamic power. Dynamic power is directly related to clock speed. So, one approach is an implementation that uses minimum clock speed. Using current and future generations of FPGAs, static power has become a dominant source of the total power. This paper has been shown that tradition ways of reducing power in waveform implementation needs to be challenged. The focus of waveform implementations must now consider the number of resources consumed by a design. Static power can be reduced by reducing the number resources used to implement a waveform. The reduction of resources can be achieved by increasing the clock speed and re-using resources.

8. REFERENCES

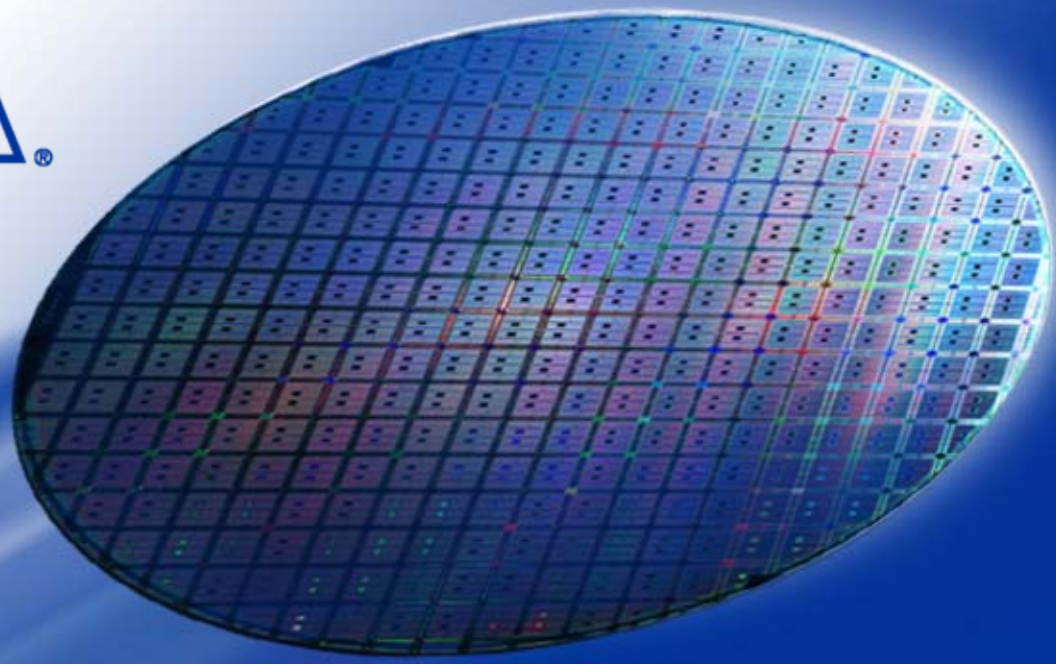
[1] Altera Corporation, Stratix II Data Sheet, www.altera.com

[2] Altera Corporation, Stratix Data Sheet, www.altera.com

[3] Altera Corporation, Cyclone II Data Sheet, www.altera.com

[4] Altera Corporation, Cyclone Data Sheet, www.altera.com

[5] Barry Pangrle, Shekhar Kapoor, *Leakage power at 90nm and below*, www.intel.com/technology/silicon/power/transistor.htm



Low-Power Software-Defined Radio Design Using FPGAs

Joel Seely

Agenda

- Overview
- FPGA Power
- Example Waveform
- Implementation Study
- Summary

Overview

- Software-Defined Radio Digital Components
  - General Purpose Processors (GPPs)
  - Digital Signal Processors (DSPs)
  - Field-Programmable Gate Arrays (FPGAs)
- GPPs & DSPs Used for Legacy Waveforms
- FPGAs Required for Future Waveforms

FPGA Power Overview

- GPPs & DSPs Have Many Low-Power Modes
  - Software Must Be Designed to Use These Modes
  - No Great Effect on Software Architecture
- FPGA Have Low-Power Capabilities
  - Heavily Design Dependent
  - Greatly Affects Hardware Architecture
  - Tradeoffs for Dynamic, Static & Interface Power Consumption

Components of FPGA Power

- Dynamic Power
  - Switching Power
- Static Power
  - Device Leakage With No Activity
- Interface (I/O) Power
  - External Communication
  - Switching Power
  - Interface Standard

Dynamic Power

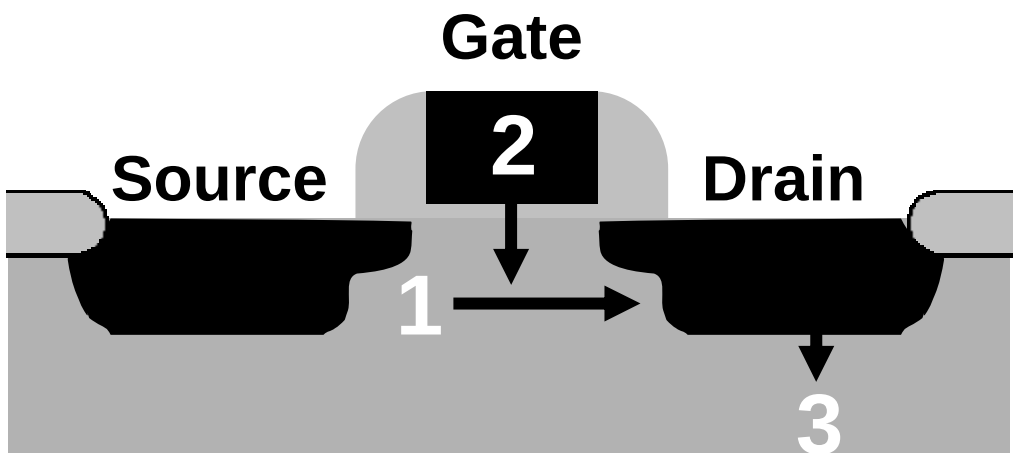
- Dominent Factors
  - Switching Frequency
  - Switching Activity (Toggle Rate)
- Relatively Constant With Silicon Process Technologies
- Relatively Constant With Process Variations

$$P_{dynamic} = \left[\frac{1}{2} CV^2 + Q_{ShortCircuit} V \right] f \cdot activity$$

$P_{dynamic}$:	Dynamic Power Consumption
CV^2:	Capacitance Charging Component
$Q_{ShortCircuit}V$:	Short Circuit Charge During Switching
f:	Switching Frequency
activity:	Switching Activity Rate (i.e., Toggle Rate)

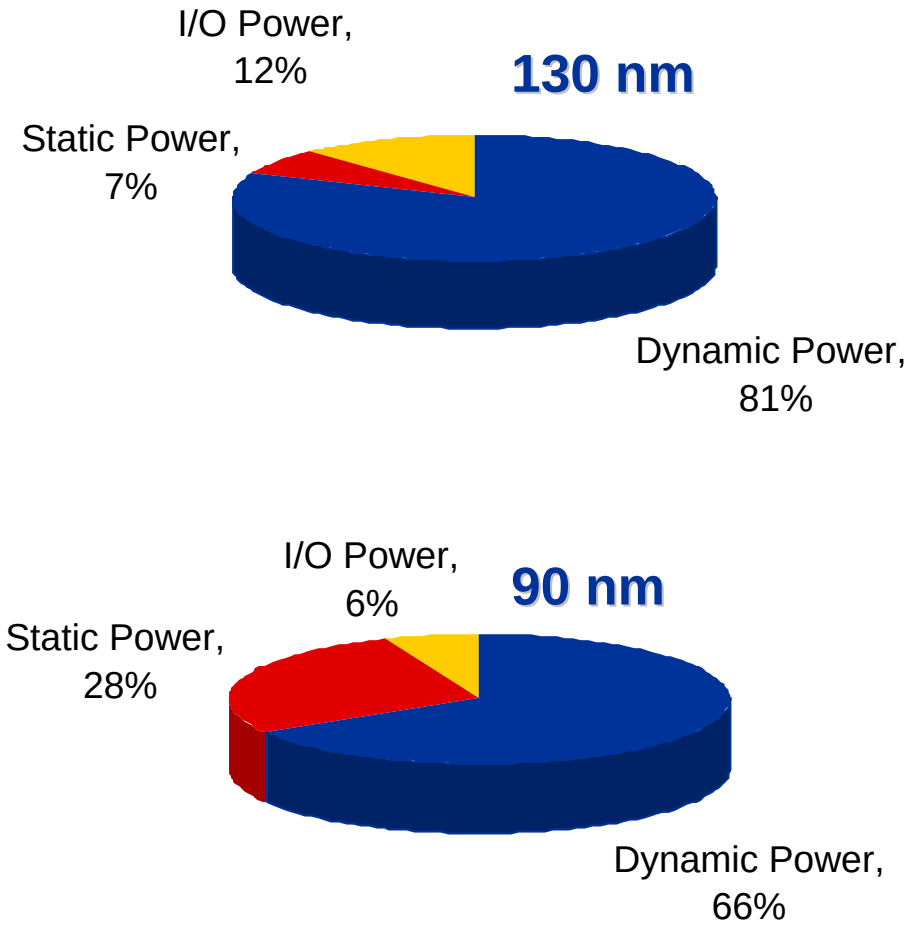
Static Power

- Increasing With Smaller Processes Technologies
- Significant Impact Due to Process Variation



1. Sub-Threshold Leakage From Source to Drain of Off Transistors
   - Main Leakage Component
   - Increases Rapidly With Temperature
   - ***Highly Dependent on Process Variation***
2. Gate Leakage (Smaller but Increasing at 65 nm, esp. at Lower Temperature)
3. Reverse-Biased Junction Leakage (Very Small)

Power Components by Process



- Static Power Becoming a Dominant Component
- 4x Increase in Percentage
- Factor in Variations
  - Process
  - Temperature

- Performance-Optimized Family

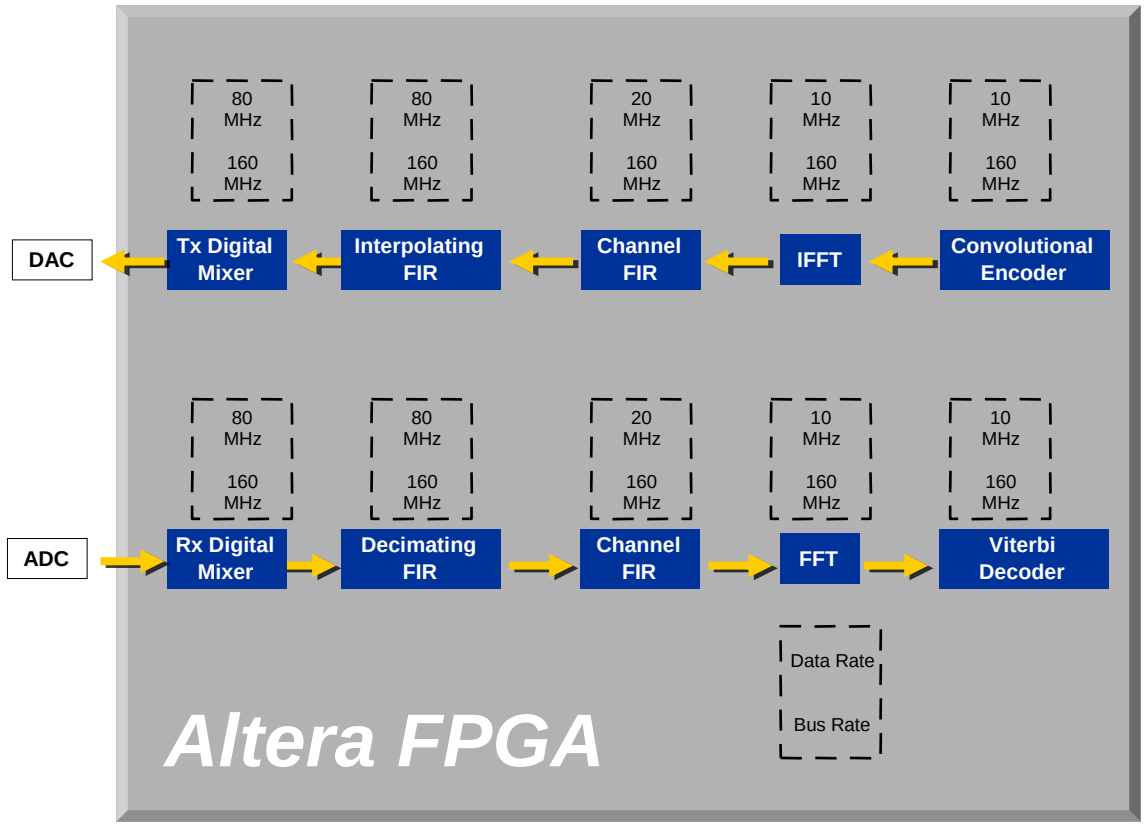
- Worst-Case Process Variation

Example Waveform

- Orthogonal Frequency Division Multiplexing (OFDM)
- Forward Error Correction (FEC) Using Convolutional Coding
- Band-Pass Sampling (80 MSPS)
- Symbol Rates of 10 MSPS
- User Data Rate of 10 Mbps
- Duty Cycle as Follows:
  - 20% Transmit
  - 20% Receive
  - 60% Standby

Example Waveform

- Top Number: Required Data Rate
- Bottom Number: Maximum Operating Frequency



Implementation Choices

- Flat
  - Design for Lowest Clock Rate
  - Large Design Area
- Time-Division Multiplex (TDM)
  - Design for Maximum Clock Rate
  - Small Design Area
- Choosing a Power-Efficient Implementation
  - Not Just a Dynamic Power Consideration

Implementation – Dynamic Power

Flat vs. TDM Design

- Use Less Dynamic Power
- Use More FPGA Resources

Flat Design

Block	Clock Rate	Dynamic Power @ 85°C
Tx Digital Mixer	80 MHz	134 mW
Interpolating FIR	80 MHz	104 mW
Tx Channel FIR	20 MHz	20 mW
IFFT	10 MHz	21 mW
Convolutional Encoder	10 MHz	1 mW

TDM Design

Block	Clock Rate	Dynamic Power @ 85°C
Tx Digital Mixer	160 MHz	134 mW
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IFFT	160 MHz	108.10 mW
Convolutional Encoder	160 MHz	6.22 mW

Implementation – Total Power

- Static Power is Half of the Total Power
- TDM Implementation Uses 30% Less Total Power
  - Use Smaller FPGA, Less Transistor Leakage
- Duty Cycle (20% Tx, 20% Rx, 60% Standby)
  - Static Power Has Larger Effect
  - TDM Implementation Uses 53% Less Power

Power	Flat Design (Using EP2C70) @ 85°C	TDM Design (Using EP2C20) @ 85°C
Dynamic Power	573 mW	643 mW
Static Power	606 mW	158 mW
Total Power	1181 mW	801 mW
Duty Cycle Power	478 mW	223 mW

Summary

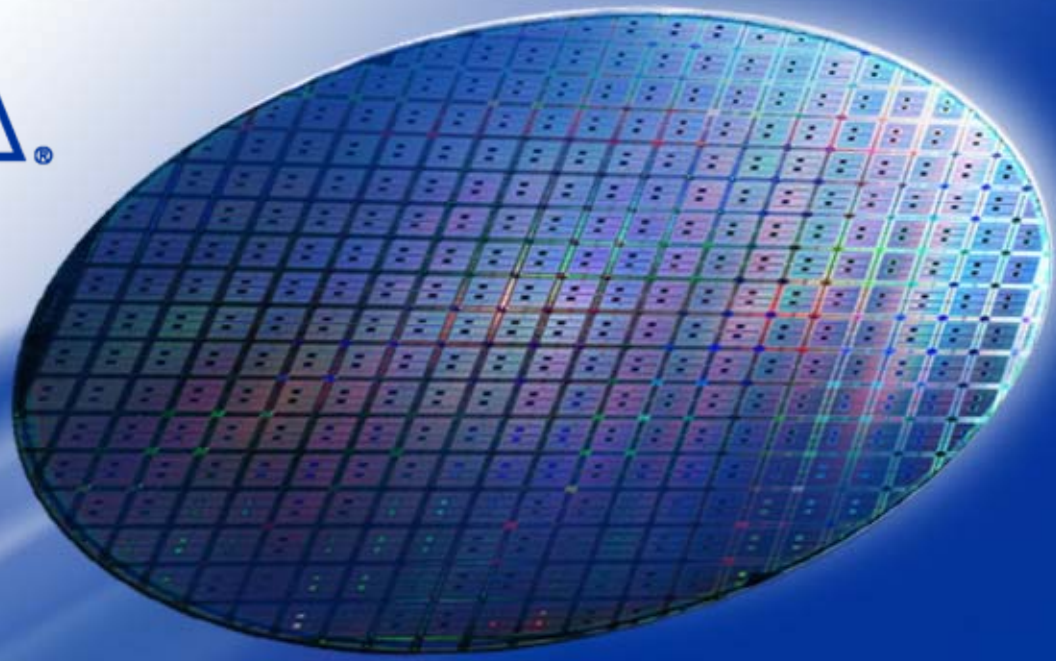
- Silicon Process is Changing the Rules for Low-Power FPGA Design
- Static Power is Becoming a Dominant Factor
- Upfront Implementation Choices Need to Consider Static Power
- Time-Division Multiplex Design

Reduce FPGA Resources

→ Reduce Number of Transistors

→ Reduced Static Power

ALTERA



Thank You

Joel Seely