DTX: A REVOLUTIONARY DIGITAL TRANSMITTER TECHNOLOGY TO PROVIDE MULTI-MODE/MULTI-BAND CAPABILITY

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ABSTRACT

This paper introduces a novel wide-band polar digital transmitter (DTx). The design integrates several functions, including I/Q to polar conversion, phase modulation, amplitude modulation, phase/amplitude combining, and RF power amplification . The basic functionality and advantages of the DTx are presented. In addition, measured results for cdma2000 and GSM/Edge cellular technology are provided to demonstrate the performance capabilities of the proposed DTx architecture as a multi-mode-multi-band transmitter, which is an essential advantage from the software defined radio applicability standpoint.

INTRODUCTION

Emerging 2.5G, 3G and WLAN standards have adopted linear modulation schemes, forcing transmitters to maintain linearity throughout the lineup. These wide bandwidth transmitter products have both aggressive power efficiency and low cost requirements that are challenging the limits of today's architectures. To date, the preferred choice for these transmitters has been the analog I/Q up-conversion architecture. Preserving the signal quality and linearity throughout the I/Q transmitter requires analog circuits that drain significant current. . Furthermore, it is difficult f6r such architectures to meet stringent requirements such as low cost, small form factor, and multi-mode multi-band operation.. In recognizing the limitations of traditional I/Q architectures, it has become important to investigate the potential for polar-based transmitter architectures as an alternative [1]. This has resulted in the development of the polar-based Digital Power Amplifier (DPA) and its associated Digital Transmitter (DTx) architecture, which will be presented in this paper.

POLAR TRANSMITTER FUNDAMENTALS

Although several wireless and cellular standards employ MPSK-type modulation schemes, few of these standards qualify as true polar modulation schemes, for which there is no amplitude modulation in the final RF carrier transmitted over the channel, i.e., a constant envelope carrier. An example of a modulation scheme that map directly into a polar architecture is the GSM GMSK modulation. In order to transmit a non-constant-envelope signal via a polar transmitter, the I/Q base-band output must be converted from the I/Q (rectangular) coordinates to the corresponding polar (r,θ) coordinates. Figure 1 illustrates the spatial relationship between the polar and the rectangular coordinates. The mathematical relationship between a polar and a rectangular point can be expressed as:

$$(r,\theta) = (\sqrt{I^2 + Q^2}, \tan^{-1}\left(\frac{Q}{I}\right))$$

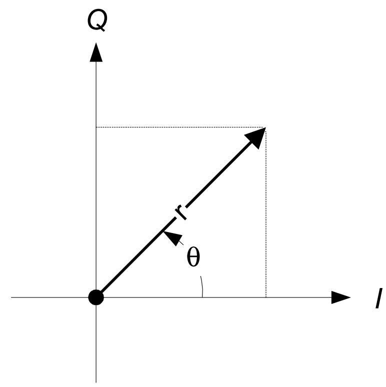

Figure 1: Rectangular/Polar Conversion.

The implementation of this conversion can be computationally burdensome given the need to implement the square-root function, the division operation, and arctangent operation. However, one well-known method that efficiently and accurately implements the rectangular-to-polar conversion with low complexity is the COordinate Rotation DIgital Computer (CORDIC) algorithm [2]. The CORDIC algorithm accomplishes the conversion without multipliers or table lookups. Instead, an iterative shift and add performs the conversion. This yields a substantial reduction in conversion complexity and cost.

Since rectangular-to-polar transformation is a non-linear operation, the resulting magnitude and phase signals of

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linear modulation schemes are of larger bandwidths than that of the source I/Q signals. Hence, one fundamental challenge of realizing a polar transmitter is to be able to accommodate the larger bandwidth requirement of the phase and amplitude signals, such that the reconstructed I/Q signals are of a satisfactory quality. It has been observed that for many modulation schemes, the phase signal would require approximately 3~9 times the source I/Q bandwidth, while the amplitude signal would require approximately 1~7 times the source I/Q bandwidth.

Another challenge for polar transmission is the alignment of the phase and magnitude components prior to recombining them to form a fully modulated signal. This is because the phase and amplitude signals travel through separate circuit paths and encounter different processing delays. Hence, tight control over the delay mismatch between the amplitude and phase signals is required in order to construct the modulated carrier signal with sufficient fidelity.

THE DIGITAL TRANSMITTER ARCHITECTURE

Figure 2 depicts a high level abstraction of the Digital Transmitter architecture, which consists of two modules, namely, the Digital Modulator (DM) module and the Digital Power Amplifier (DPA) module.

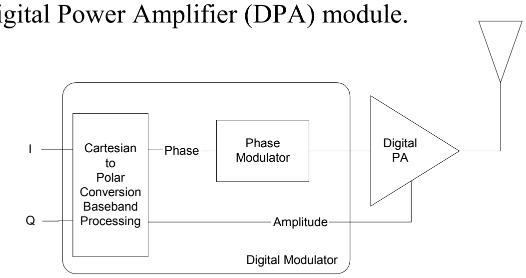

Figure 2: The DTx Digital Polar Modulator Block Diagram

The DM module converts the native digital baseband I/Q signals from the Cartesian domain to the polar domain. This digital interface eliminates the need for baseband D/A converters and reconstruction filters. This block also performs the signal processing to meet spectral mask requirements and compensate for AM/AM and AM/PM distortions. The phase information is passed through a phase modulator, yielding an on-channel, phase-modulated carrier. The phase-modulated carrier is fed into the Digital Power Amplifier (DPA), along with the amplitude modulation information. The two signals are combined to generate a fully- modulated carrier, with the required output power signal level. The combining of the magnitude and phase signals takes place at the final output stage of the DPA, allowing the earlier stages of the DPA to operate in compression. . This digital transmitter approach can also be re-configured for multi-band/multi-mode operation: The DTx is tunable through an off-channel synthesizer to support different bands. There is no band-specific hardware and therefore the DTx can be configured for different frequency bands and modulation schemes by simply re-configuring clock frequencies and filtering coefficients to support the desired standards. Finally, power control; an important issue in the design of CDMA transmitters, is accomplished with multiple VGA stages operating in the transmit chain. Because the DTx is a direct conversion, polar-based approach, it follows that all the gain control must take place at RF frequencies.

THE DIGITAL PHASE MODULATOR

Description

The phase modulator section of the digital transmitter consists of a sigma delta (SDM) fractional-N PLL. Phase modulation is performed by passing the base-band phase-signal through the SDM and modulating the N-divider's count, as depicted in Figure 3. The modulation of the N-divider then modulates the output frequency of the PLL, providing a digital modulation path. Because of the PLL loop bandwidth constraints, driven by receive-channel noise specifications; a pre-emphasis approach is used to extend the modulation bandwidth of the system. Finally, the VCO is operated at 2 times the channel frequency to provide isolation from the radiated transmitter output.

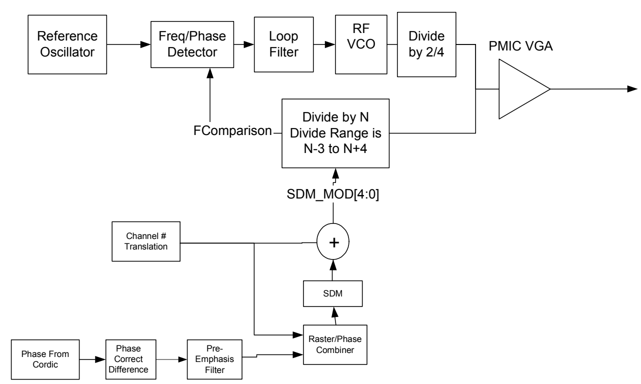

Figure 3: The Phase Modulator (PM) Module.

Operation

There are many different potential design approaches for a phase modulator, ranging from an IQ modulator in a translational loop, to a DDS approach. Our approach has been chosen because of it provides a predominantly digital circuit-level implementation solution, with a direct RF output. The most significant issue with this approach is the fact that the modulation bandwidth is limited by the closed loop bandwidth of the PLL. Because of trade-offs between receive channel noise, the sigma delta modulator noise, and the spurious components, the loop filter bandwidth cannot be moved out far enough to accommodate the wide phase bandwidth of the phase component. Thus, a pre-emphasis scheme is needed in order to compensate for the limited bandwidth of the PLL loop.

THE DIGITAL POWER AMPLIFIER

Description

The Digital Power Amplifier combines multi-band RF power amplification, efficient power control, wideband amplitude modulation, and phase/amplitude combination in a single module. The DPA consists of circuit approaches that convert any digital amplitude to modulated RF waveforms at the desired RF transmit power. Within the DPA, the digitized envelope and phase modulated RF carrier are combined to produce a fully modulated high power RF transmission. A pictorial illustration of the DAP is shown in Figure 4.

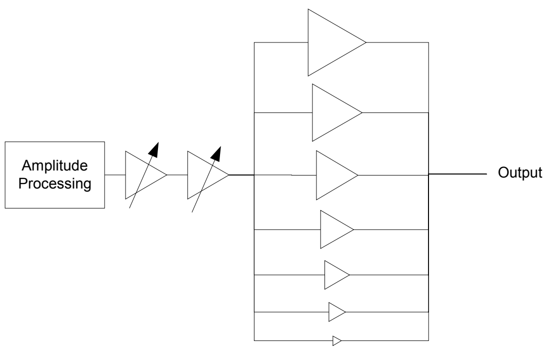

Figure 4: Digital Power Amplifier (DPA) Block Diagram.

Operation

The DPA consists of 2 VGA stages to provide for output power control, followed by multiple parallel gain stages, each controlled by a control bit. With 7 bits of control, there are 128 discrete gain steps possible. Current combining in the output achieves the desired output power, which varies depending on the desired modulation.

Characteristics

When used in conjunction with the Digital Transmitter, the Digital Power Amplifier offers several advantages:

- *The DPA is capable of wideband amplitude modulation*. Amplitude bandwidths associated with all the major modulation schemes are readily accommodated (envelope bandwidths of 10MHz and beyond).
- *Performing amplitude modulation at the last stage of the DPA gives reduced current drain over the transmit power control range*. The final stage of the DPA is biased into Class-B or Class-C operation. Additionally, the driver stages are operated non-linearly for efficiency, consuming very low quiescent current (<30mA).
- *The DPA facilitates efficient power control at all levels of RF power*. A dynamic range of 55dB is realized under CDMA modulation. This is possible because the gain is applied to a constant-envelope waveform that contains only phase information. The phase is insensitive to distortion and, consequently, the DPA stages are biased to operate non-linearly for efficiency over the power control range. Additional power control dynamic range can be obtained through the phase path stages, to satisfy the CDMA requirement of ~ 80dB of power control dynamic range.

Digital Optimization

The DPA has the advantage that its AM/AM and AM/PM non-linearity can be corrected in digital baseband. To correct for non-linearity, the digital amplitude states are mapped to provide the required RF output current. Figure 5 provides a simplified pictorial illustration of how to digitally correct AM/AM and AM/PM distortion effects in the DPA.

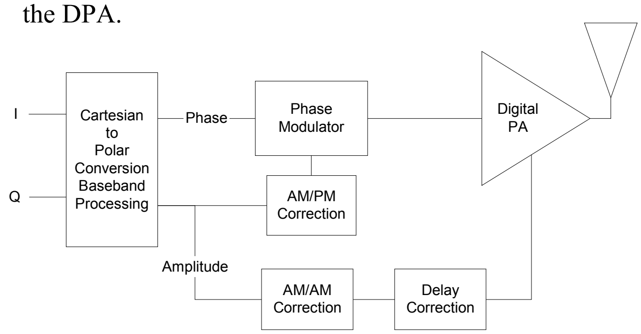

Figure 5: AM/AM and AM/PM Correction.

In addition, the DPA allows for high degree of control and tradeoff between clipping[2] and digital optimization.

Measured Results

The first Digital Power Amplifier IC was designed primarily for CDMA2000 operation in the Cellular and PCS bands. The prototype Digital Power Amplifier was designed with seven bits of digital amplitude resolution meaning that it had 128 possible states (0 to 2^7-1). The microphotograph of the GaAs HBT DPA that covers both cellular and PCS bands is presented in Figure 6. Also, Table 1 summarizes the measured performance of the prototype DPA under CDMA2000 modulation in both the cellular and PCS bands. The measured noise at 45MHz and 80MHz offsets is –132dBm/Hz and –135dBm/Hz respectively.

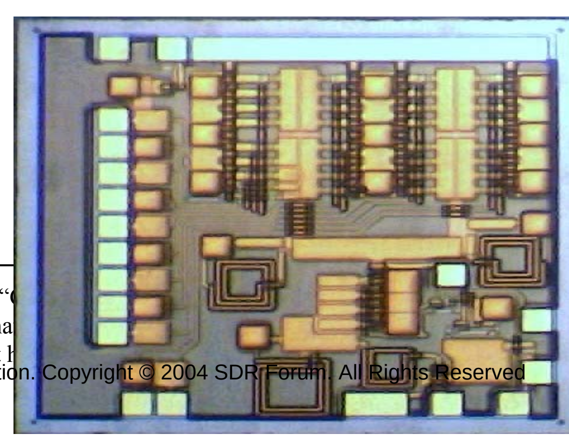

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Figure 6: Microphtograph of the Dual-Band CDMA DPA.

Measurement	Value
Main Channel Power	27.30 dBm
ACPR 1 Upper	-46.20 dB
ACPR 1 Lower	-46.50 dB
ACPR 2 Upper	-67.40 dB
ACPR 2 Lower	-67.40 dB
Rho	0.995
PAE	39.60 %

Table 1: Measured Performance of the Prototype DPA Under CDMA2000 Modulation.

Figure 7 shows the measured performance of the DPA, before and after digital optimization. At high power levels digital optimization is easily applied to correct for amplitude and phase non-linearity, hence, optimizing the performance and pushing the limits of the DPA capability. The improvements in the DPA characteristics are also clear from the results in Figure 7.

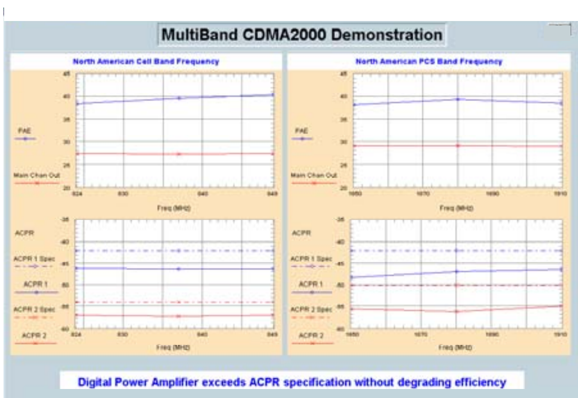

Figure 7: Measured Performance of the DPA Before and After Digital Optimization.

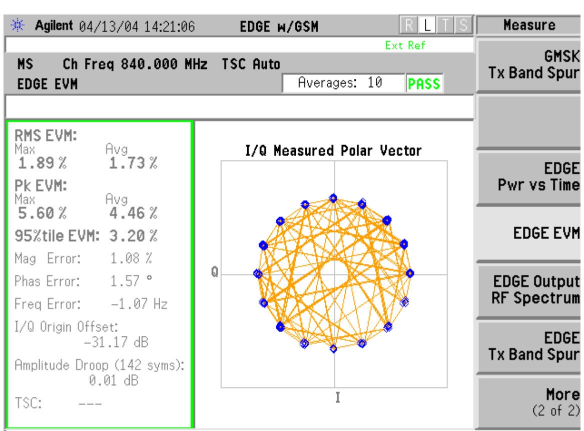

Figure 8: EDGE Measured Constellation Plot.

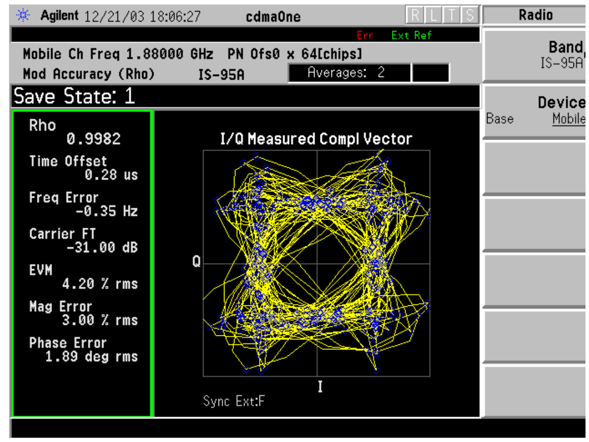

Figure 9: CDMA Measured Constellation Plot.

Figure 8 and Figure 9 show the measured constellation plots for EDGE and CDMA2000, respectively.

CONCLUSION

This paper presents the novel wideband Digital Power Amplifier (DPA) and the associated Digital Transmitter Architecture (DTx). When used within the Digital Transmitter, the Digital Power Amplifier offers several important benefits for transmitter integration and power consumption while enabling seamless control for multiband and multimode devices in a single circuit enabling software defined transmitters. The first Digital Power Amplifier prototype has been fabricated in GaAs HBT, with 7-bit resolution, operating at 0.9GHz and 1.9GHz, and has shown to meet all the CDMA2000 performance specifications.

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