Wideband Modem Design Using FPGAs

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1. ABSTRACT

New waveform requirements are pushing the limits of traditional modem design techniques. Fortunately, modern Digital-to-Analog Converter (DAC) and Analog-to-Digital Converter (ADC) can achieve sampling rates in the GHz range. These new DACs and ADCs allow designers to directly synthesize channels that have bandwidths of more than 500 MHz+; allowing either wideband or multi-channel modems to be implemented entirely in the digital domain. This eases the requirements on the Radio Frequency (RF) portion of the radio design. To fully utilize the available bandwidth of the DACs and ADCs, new techniques in modem design must be considered. Using a combination of polyphase decomposition and sub-sampling, the FPGA-based modem can provide waveform processing for the entire Nyquist bandwidth of the DAC/ADC. This paper outlines the concepts involved in implementing a wideband digital modem.

2. BACKGROUND

Traditionally, frequency translation (i.e. up-conversion) has been performed by analog components. Analog components such as voltage controlled oscillators (VCO) and mixers are used to approximate the mathematical expressions of the up-conversion process. Careful design practices must be used to insure the operation of analog components over power, voltage, and temperature. In addition to the normal difficulties involved in analog design, the fact that the analog circuit is only an approximation also introduces unwanted effects in the up-converted signal.

With the current generation of digital signal processors (DSP) and FPGAs, it is possible to perform some level of frequency translation in the all-digital domain. The fundamental limitation of digital up-conversion is dependent on the clock speed of the digital device. For example, Altera's Stratix II FPGAs have typical internal clock speeds of 300 MHz. Even at this high clock rate, the Nyquist criteria states that the maximum digital bandwidth would be in the range of 150 MHz. Clearly, this is not useable as a direct up-conversion solution.

Currently, modems employ a mixed analog/digital architecture for up-conversion. Figure 1 shows a block diagram of a typical modem using this mixed architecture. In this scheme the FPGA performs the variable up-conversion, while the analog section performs a fixed up-conversion. The remainder of this paper describes a method to eliminate the analog up-conversion section.

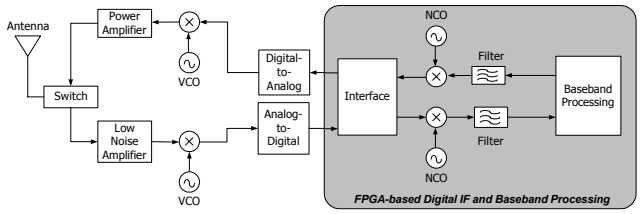

Figure 1: Mixed Analog/Digital Modem

3. FPGA OVERVIEW

Before describing the operation of the polyphase modem, an overview of the relevant features of FPGAs is presented. The current generation of FPGAs contains many system level features. In addition to look-up tables (LUTs) and registers, FPGAs contain: arithmetic operators, phase locked loops (PLL), high-speed I/O, and memory. Table 1 shows the features of Altera's Stratix II FPGA family [1] as an example of the rich feature set that can be found in today's advanced FPGAs.

Table 1: Stratix II Family

Device	Equivalent Logic Elements	Total Memory Bits	18x18 Multiplier	PLLs
EP2S15	15,600	419,328	48	6
EP2S30	33,880	1,369,728	64	6
EP2S60	60,440	2,544,192	144	12
EP2S90	90,960	4,520,448	192	12
EP2S130	132,540	6,747,840	252	12
EP2S180	179,400	9,383,040	384	12

4. POLYPHASE DIGITAL UP CONVERTOR

A straightforward implementation of a FPGA-based digital upconvertor will only yield design with sampling rates of ~300 MHz. Table 2 shows the clock speeds of some common digital modem components that can be implemented in a high-density FPGA.

Table 2: Common Modem Component Clock Rates

Component	Maximum Speed
FIR Filter	339 MHz
NCO	404 MHz
FFT (256 point)	314 MHz

With these clock speeds, FPGAs can easily synthesize signals with bandwidths of 150MHz+.

Current generation of DACs have sampling rates greater than 1GHz ([2], [3]). FPGAs have low voltage differential signaling (LVDS) interfaces that are capable of supplying signals at the GHz rates needed by the DACs. In order to take advantage of the available bandwidth of these new DACs, traditional FPGA modem design is not sufficient. The following sections look at three (3) ways to achieve these sampling rates.

4.1. Aliasing Approach

A traditional method of supplying higher sampling rates is to upsample the signal by means of zero-stuffing. This is an easy, low-overhead method of increasing the sampling frequency. From sampling theory ([4], [5]), it is known that this method of upsampling introduces aliasing. Usually, aliasing is an unwanted by-product; but for our purposes this is actually a benefit. Figure 2 shows the spectrum for an upsampled modem. As seen in this example, the output of the DAC can be bandpass-filtered (using an analog filter) to obtain the desired frequency. This method allows the narrow bandwidth (typically less than 150 MHz) of the FPGA to be translated to any frequency in the Nyquist bandwidth of the DAC (0 – 500 MHz+). Two problems exist when using the upsampling method:

1. The generated signal bandwidth is limited to the Nyquist rate of the FPGA.
2. The analog bandpass filter has a very high center frequency to bandwidth ration; which makes realization very difficult.

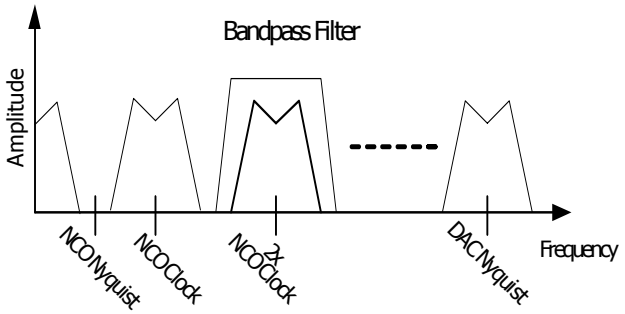

Figure 2: Upsampled Spectrum

4.2. Polyphase Approach

Another method for generating signals at the DAC sampling rates is to use polyphase decomposition. This is a method commonly used in creating interpolating polyphase FIR filters. Figure 3 shows an example of polyphase decomposition for an FIR filter. The same principle can be applied to the digital upconverter. A polyphase upconverter is shown in Figure 4.

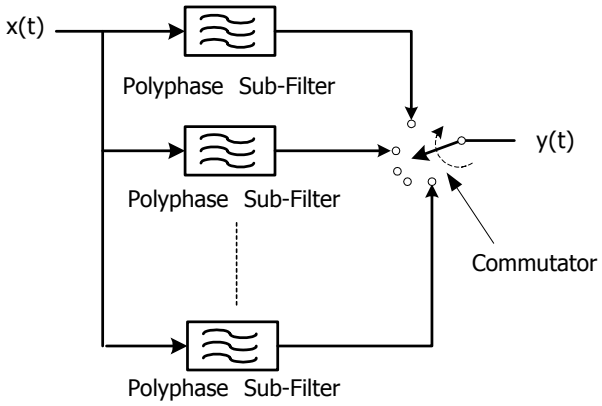

Figure 3: FIR Polyphase Decomposition

In Figure 4, each of the *sub-DUC* (a sub-DUC is defined as the polyphase component of the Digital Up Converter) consists of a polyphase sub-filter, a Numerically Controlled Oscillator (NCO) and a mixer. The sub-filters are created using standard filter decomposition [5]. The NCO in each sub-DUC is set to the same frequency, but each has a different initial phase.

The outputs of the sub-DUCs are connected to the input of the LVDS serializer. Similar to the commutator in a polyphase interpolation filter, the serializer runs at N-times the rate of the sub-DUCs. The outputs of the LVDS serializer are connected directly to the high-speed DAC.

The calculation of the initial phase of the sub-DUC NCOs uses the following formula:

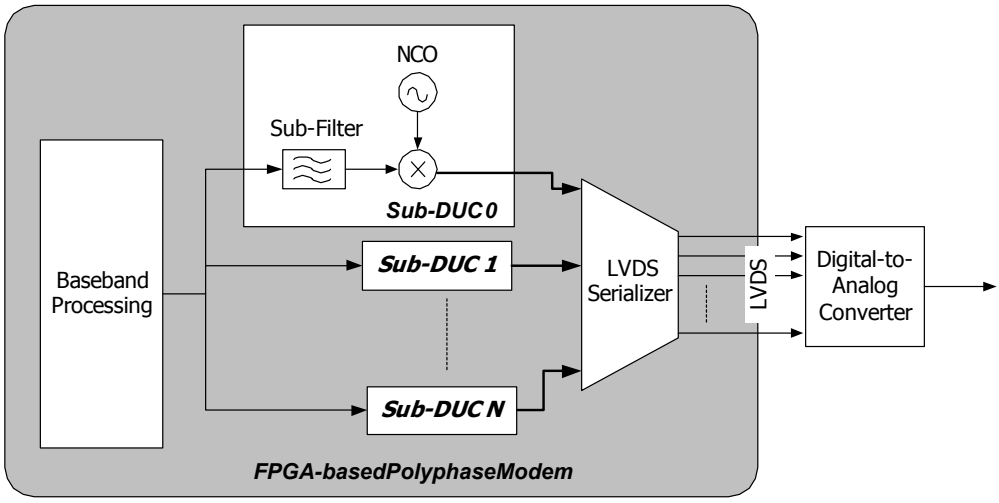

Figure 4: Polyphase Modem

$$\phi_N = \frac{360 * F_{gen}}{F_{s\_nco} * N} \quad \textbf{(Equation 1)}$$

Where:

N is the number of polyphase (i.e. sub-DDCs)

Φ_N is the phase offset on the N^{th} NCO in degrees

F_{gen} is the generated output frequency

F_{s_nco} is the sample rate of NCOs

Figure 5 shows the resulting spectrum of performing up-conversion using the polyphase approach. Notice that there a no aliasing products in the spectrum. However, this approach limits the output frequency to the Nyquist rate of the sub-DDC.

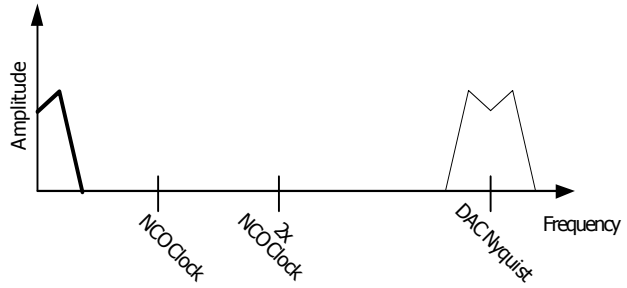

Figure 5: Frequency Spectrum of Polyphase Approach

4.3. Aliasing Polyphase Approach

In order to take advantage of the bandwidth, the polyphase NCO must be capable of generating frequencies up to the Nyquist rate of the DAC. The previous two approaches were limited in both bandwidth and generated frequency. A combination of the previous two approaches results in a design that supports the entire Nyquist bandwidth of the DAC.

The structure of the aliasing polyphase modem is identical to the one shown in Figure 4. The only difference being the initial phase of the sub-DUC NCOs.

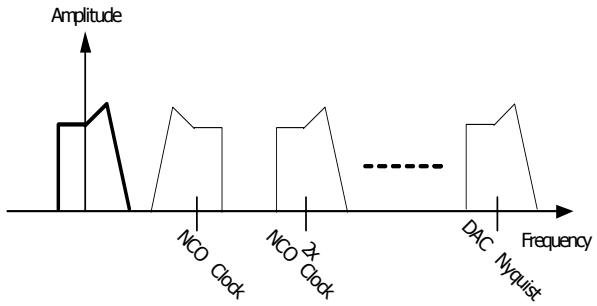

Figure 6: Spectral Inversion Caused by Aliasing

The concept is to create only one alias spectrum at the output of the DAC. This is accomplished by setting the polyphase components (the sub-DUCs) so they have the correct phase offset for the *aliased* spectrum, not the primary spectrum. One caveat is that aliasing causes an inversion of the spectrum. As seen in Figure 6, the

spectral inversion only happens for the odd aliases of the spectrum. For this case, the initial phases of the sub-DUC NCOs need to account for this inversion.

To compensate for the spectral inversion of the odd aliases, the following trigonometric identity is used

$$-\sin(\theta+\phi)=\sin(-\theta-\phi) \quad \textbf{(Equation 2)}$$

For the initial phase of each NCO, the equation is:

$$\phi_N = \frac{360 * F_{gen}}{F_{s\_dac} * N} \quad \text{(Equation 3)}$$

Where:

N is the number of sub-DUCs
F_{s_dac} is the clock speed of the DAC
F_{gen} is the desired output frequency

To determine the frequency setting of the NCOs, the aliased frequency must be determined. The following equation is used to determine the aliased frequency.

$$F_{a\_gen} = \begin{cases} F_{gen} & \text{for } F_{gen} < F_{s\_nco}/2 \\ F_{gen} - (F_{s\_nco} * alias) & \text{for } F_{gen} > F_{s\_nco}/2 \end{cases}$$

Where:

F_{a_gen} is alias frequency setting for the NCO
F_{gen} is the desired output frequency
alias is the Nyquist zone number

5. PERFORMANCE CONSIDERATIONS

The resulting output from the aliased polyphase modem is show in Figure 7. Notice that the other alias components are present, but attenuated.

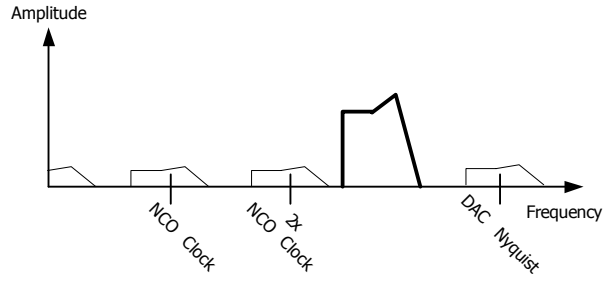

Figure 7: Aliasing Polyphase Modem Spectrum

A number of factors affect the attenuation of these components, including:

- NCO output bit width
- NCO accumulator precision
- Number of sub-DUCs used in design
- DAC spurious free dynamic range (SFDR)
- DAC intermodulation distortion

Simulations show that reasonable bit widths (~18-bits) are sufficient to suppress the unwanted alias components by 70 dBc.

6. CONCLUSION

The new generation of high-speed DACs has opened up the possibility to create direct digital up-converters. FPGAs are well suited for interfacing to these new DACs, but new modem implementations are needed. This paper demonstrated that a direct up-conversion modem can be designed using polyphase techniques along with aliasing. These techniques build on the traditional implementation of FPGA-based modems and multi-rate signal processing.

7. REFERENCES

[1] Altera Corporation, Stratix II Data Sheet, www.altera.com

[2] Analog Devices, AD9736 Data Sheet, www.analog.com

[3] Fujitsu Microelectronics, MB86064 Data Sheet, www.fujitsu.com

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[5] N.J. Fliege, *Multirate Digital Signal Processing*, John Wiley & Sons, Copyright 1994