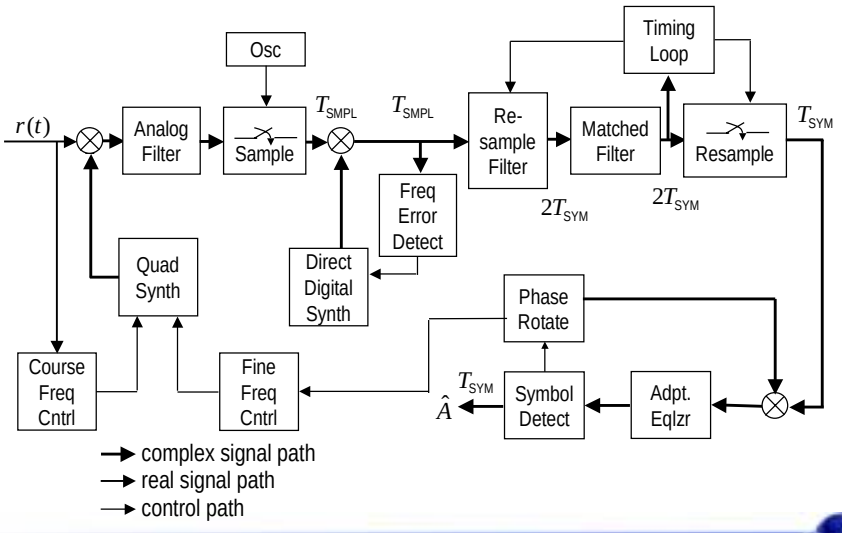
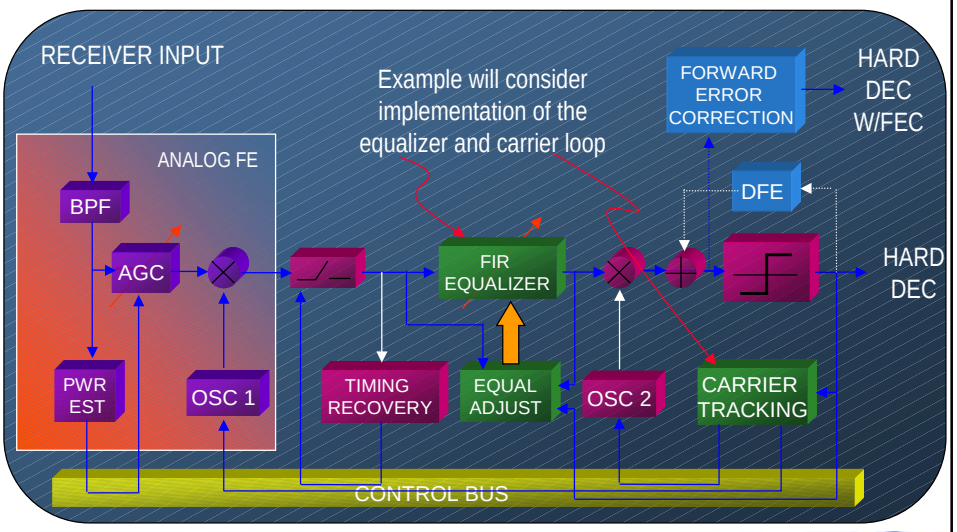
Synchronization

Dr Chris Dick
DSP Chief Architect
Director, Signal Processing Engineering

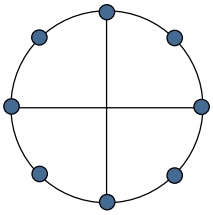
QAM Demodulator



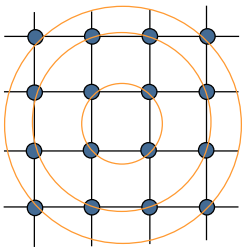
Equalized QAM Receiver



Signaling Set



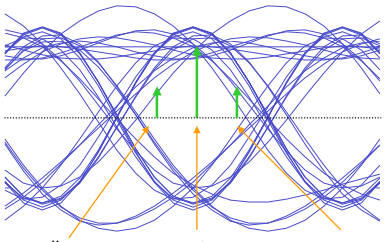
8-PSK
constant modulus alphabet



16-QAM
non-constant modulus alphabet

Timing Recovery

- Various options for timing recovery loop
  - Gardner loop (based on zero crossings in MF output)
  - Minimum variance loop (dither loop)
  - Maximum likelihood estimation (MLE)

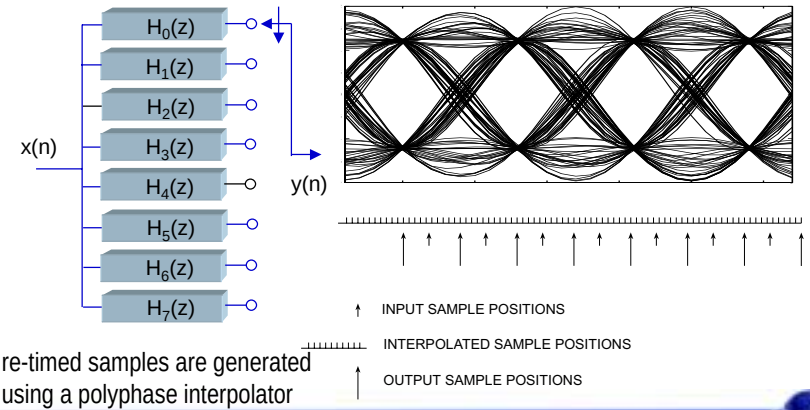


Early sampling | Optimum sampling time | Late sampling

Timing Recovery

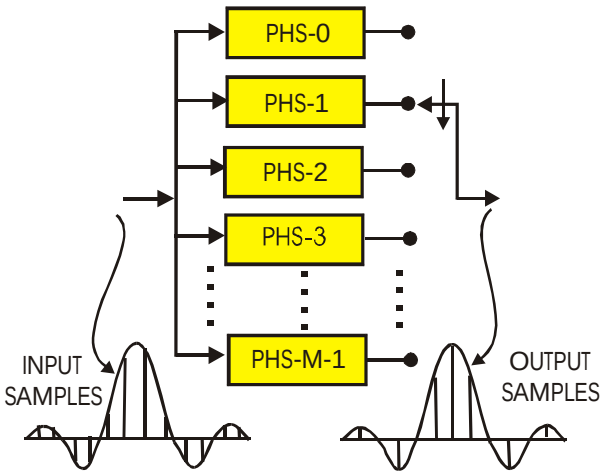
Synchronous comm system operating over a bandlimited channel with AWGN must sample matched filter output when eye is maximally open

At this time ISI is minimal and SNR is maximum

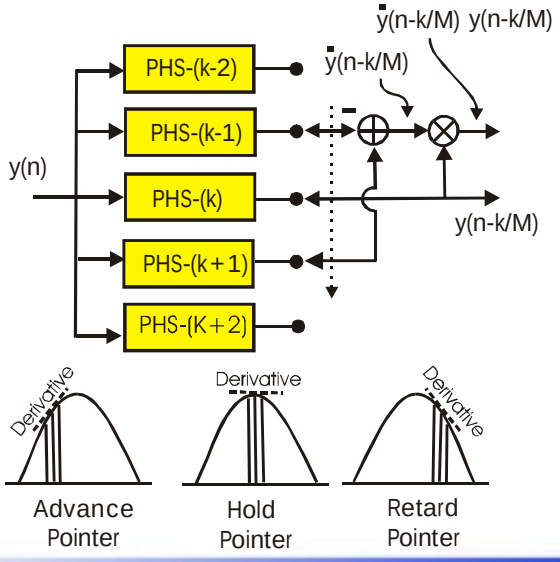


re-timed samples are generated using a polyphase interpolator

Timing Recovery

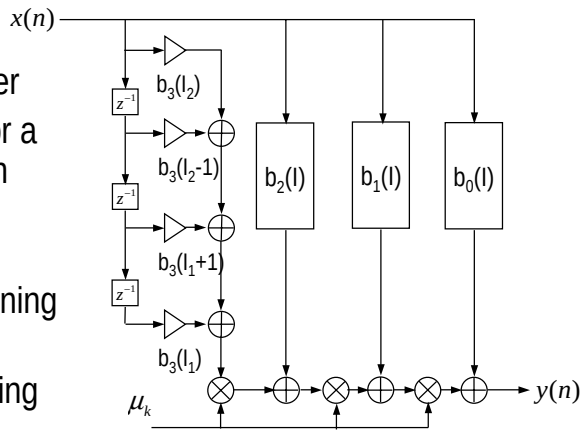


Timing Recovery



Symbol Timing Recovery

- Farrow filter
- Polynomial based filter
- Figure shows case for a cubic interpolator with coefficients based on Lagrange formulas
- Single control for defining fractional delay
- Nested evaluation using Horner's rule



Cubic Interpolating Polynomial

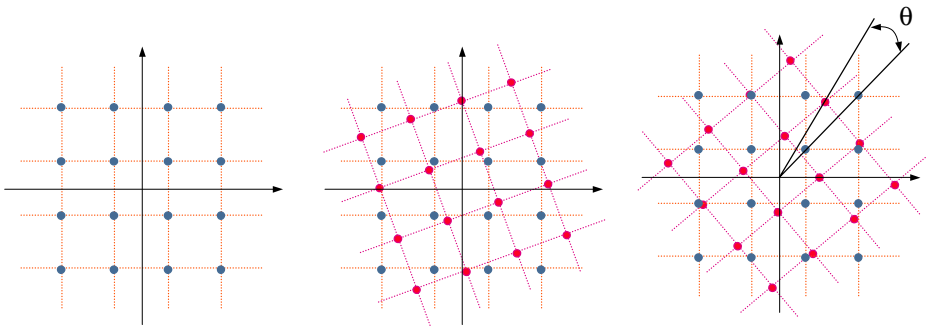
i	l=0	l=1	l=2	l=3
-2	0	-1/6	0	1/6
-1	0	1	1/2	-1/2
0	1	-1/2	-1	1/2
1	0	-1/3	1/2	-1/6

- Filter weights are fixed with this approach
- Could use table based approach for filter segments
- FPGA implementation could exploit
  - Distributed arithmetic
  - Canonic signed digit approaches

Timing Recovery Loop

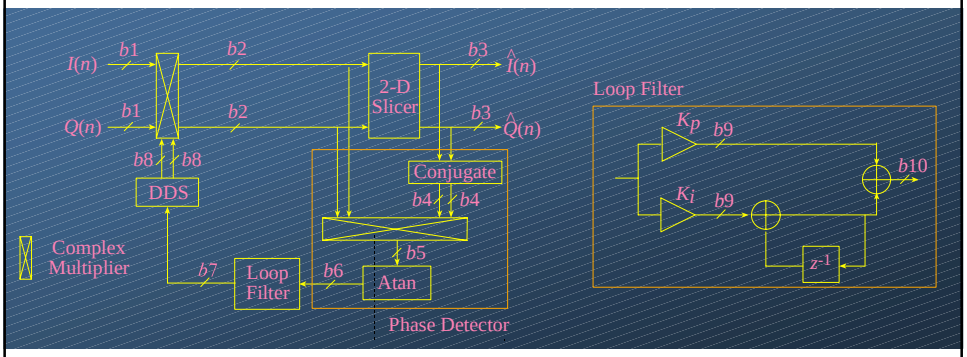
- Non decision directed approach used in this implementation
- Embed Farrow structure in a servo control loop using a PI filter
- Drive loop with gradient measure computed around optimal sampling instant
  - Maximum eye opening

Carrier Recovery



- Signaling waveform experiences rotational motion due to
  - Relative motion between Rx and Tx platforms
  - Mismatch between Rx and Tx analog mixers

Carrier Recovery Loop



- Decision aided Costas Loop
- PI loop filter

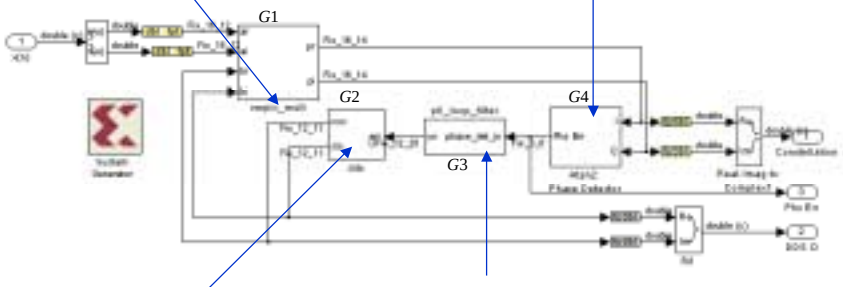
Carrier Recovery Loop

- Functional units
  - Input mixer
  - Phase detector
    - memory based (emphasis on FPGA block memory)
    - logic fabric based (consuming slices) using CORDIC
  - Loop filter
  - DDS

Carrier Recovery Loop

Mixer using Virtex-II
Embedded multipliers
- 3 multipliers/ 5 additions

CORDIC based
phase detector

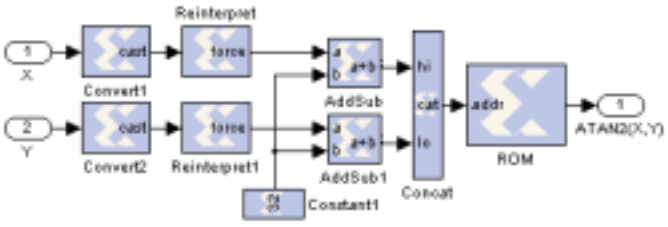


Look-up table Based DDS

PI Loop filter using 2
embedded multipliers

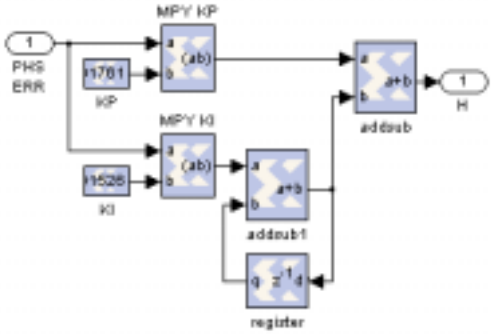
Memory Based PD

- I & Q samples merged to form address for atan2() LUT



PI Loop Filter

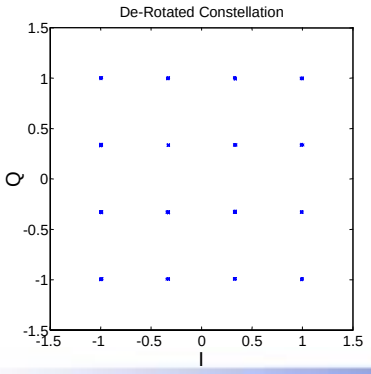
- Uses two Virtex-II(P) embedded multipliers
- Small amount of fabric

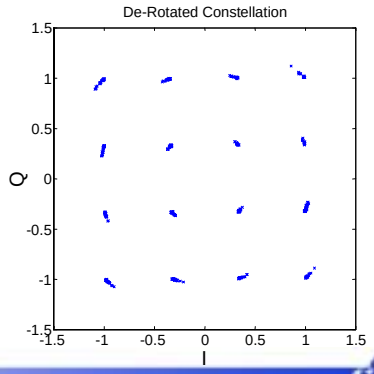


Presentation Name 17

Loop Simulation

- Floating-point reference
- Fixed-point: 4096x8-bit precision LUT
- 2 Virtex-II block ROMs

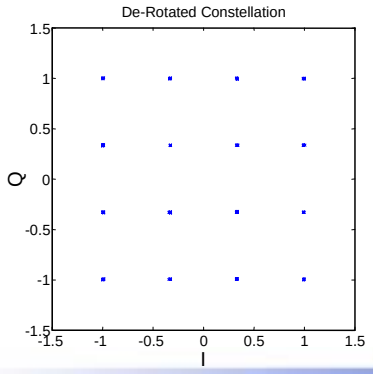


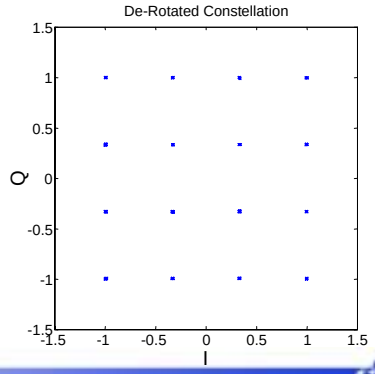


Presentation Name 18

Loop Simulation

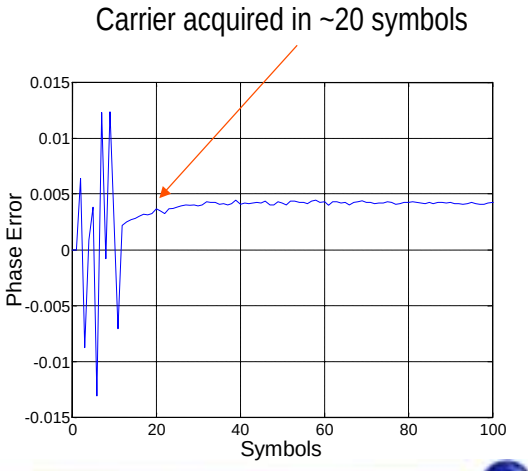
- Floating-point reference
- Fixed-point: 16384x8-bit precision LUT
- 8 Virtex-II block ROMs





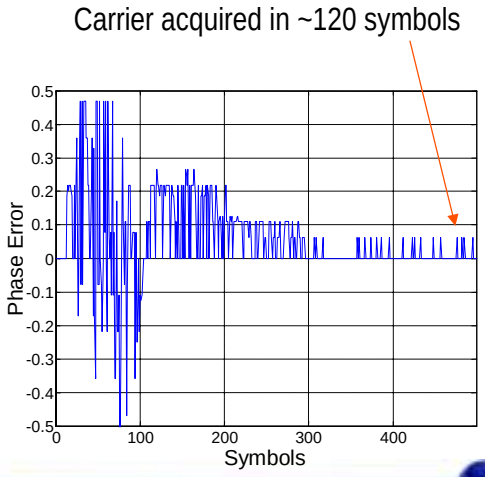
Acquisition Time

- Floating-point
- 0.001 Hz Doppler
- 4 samples/symbol



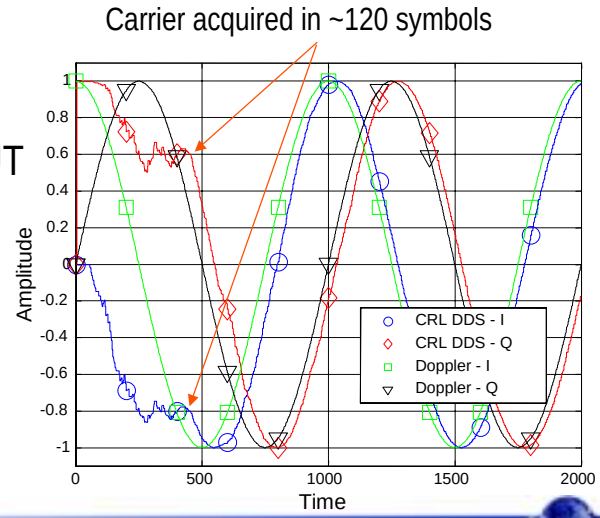
Acquisition Time

- 4096x8 atan2() LUT
- 0.001 Hz Doppler
- 4 samples/symbol



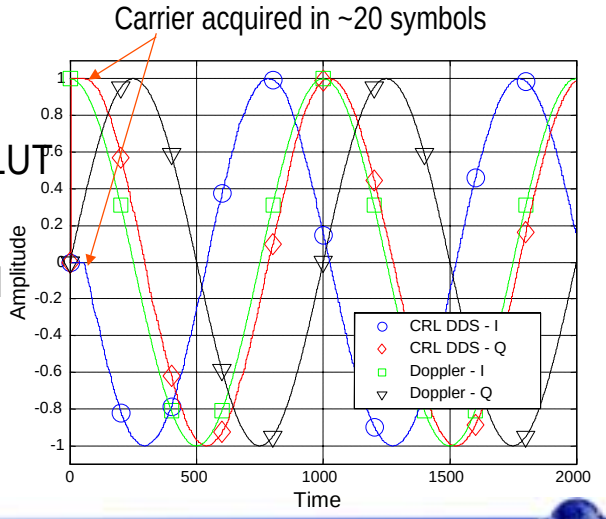
Acquisition Time

- 4096x8 atan2() LUT
- 0.001 Hz Doppler
- 4 samples/symbol



Acquisition Time

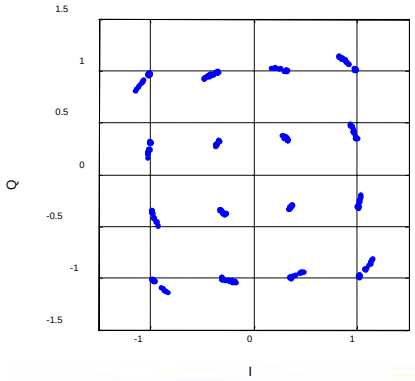
- 16384x8 atan2() LUT
- 0.001 Hz Doppler
- 4 samples/symbol



Acquisition Time

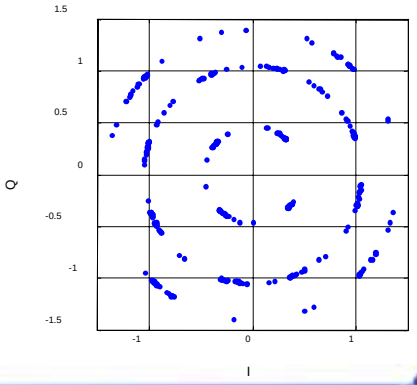
- Loop acquisition phase - symbols 50 to 400

16384x8 atan2() LUT



(a)

4096x8 atan2() LUT



(b)

CRL Resources

Memory-based PD

Function	Slice Count	Block RAMs	Embedded Multipliers
Heterodyne	111	-	3
DDS	5	1	-
Loop Filter	32	-	2
Phase Detector	106	2	3
Total	254	3	8

CORDIC PD

$i = 0$

$z_i = 0$

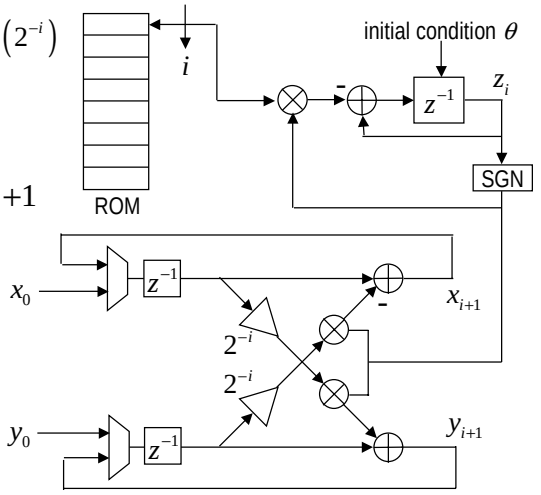
$a_i = -1$ if $z_i < 0$ otherwise $a_i = +1$

$x_{i+1} = x_i + a_i y_i 2^{-i}$

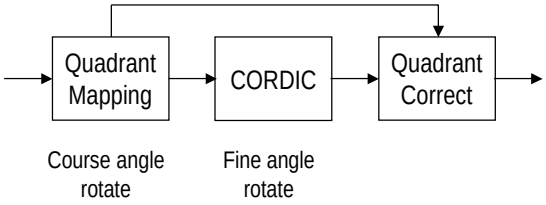
$y_{i+1} = y_i - a_i x_i 2^{-i}$

$z_{i+1} = z_i + a_i \tan^{-1}\left(2^{-i}\right)$

$i = i + 1$



Extended CORDIC

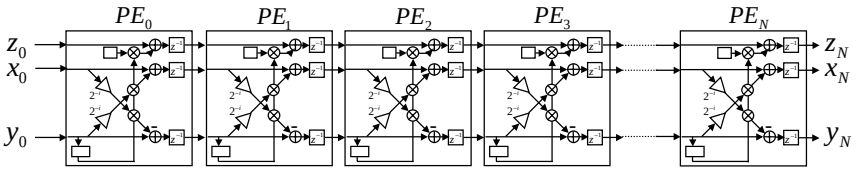


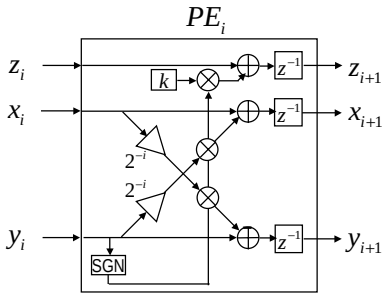
- Algorithm converges for angles

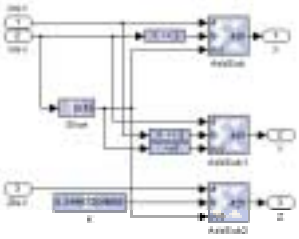
$$\frac{-\pi}{2} \le \theta \le \frac{-\pi}{2}$$

- Need to map angles to quadrants 1 and 4

CORDIC Fine Angle Processor





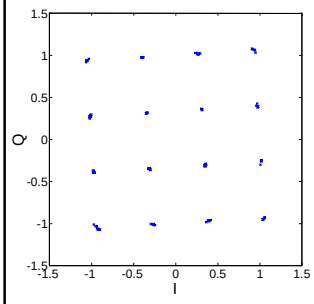


System Generator Implementation

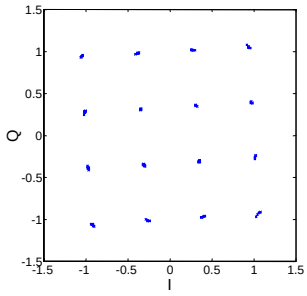
Acquisition Time

- 4 iteration CORDIC

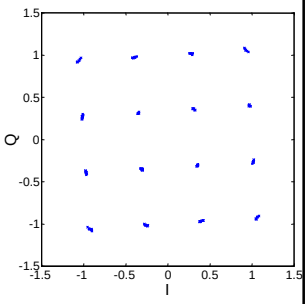
Q16.12 phase angle



Q14.10 phase angle



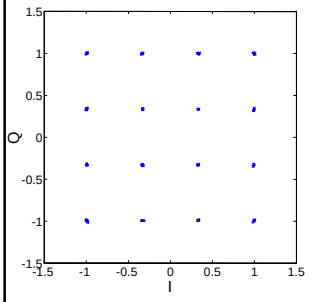
Q12.8 phase angle



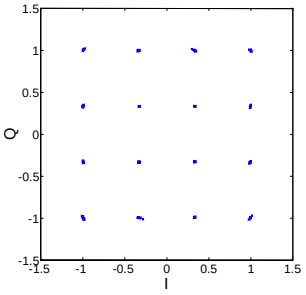
Acquisition Time

- 5 iteration CORDIC

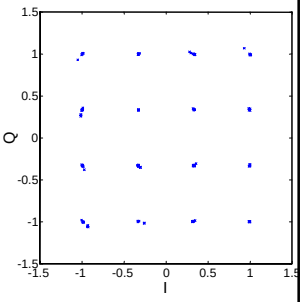
Q16.12 phase angle



Q14.10 phase angle

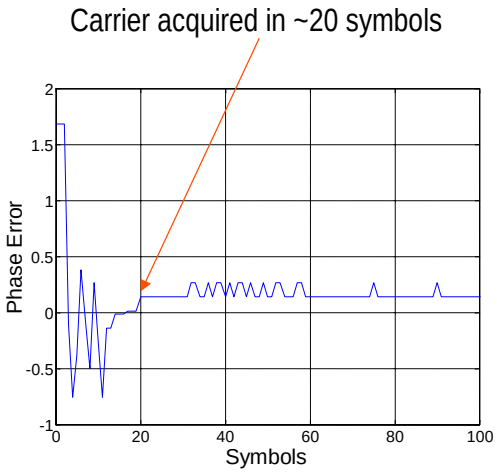


Q12.8 phase angle



Acquisition Time

- 0.001 Hz Doppler
- 5 iteration CORDIC

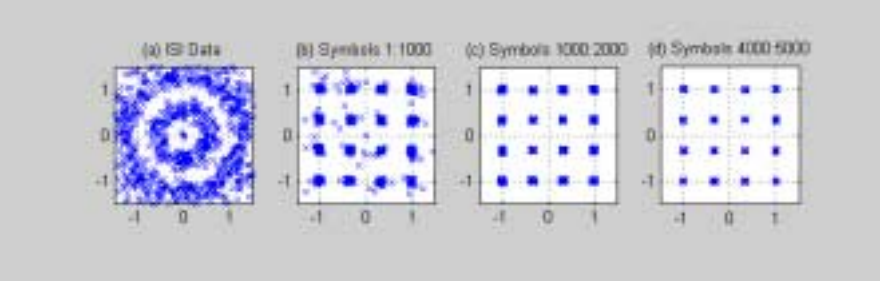


CORDIC CRL Resources

Function	Slice Count	Block RAMs	Embedded Multipliers
Heterodyne	111	-	3
DDS	5	1	-
Loop Filter	32	-	2
Phase Detector	270	-	3
Total	413†	1	8

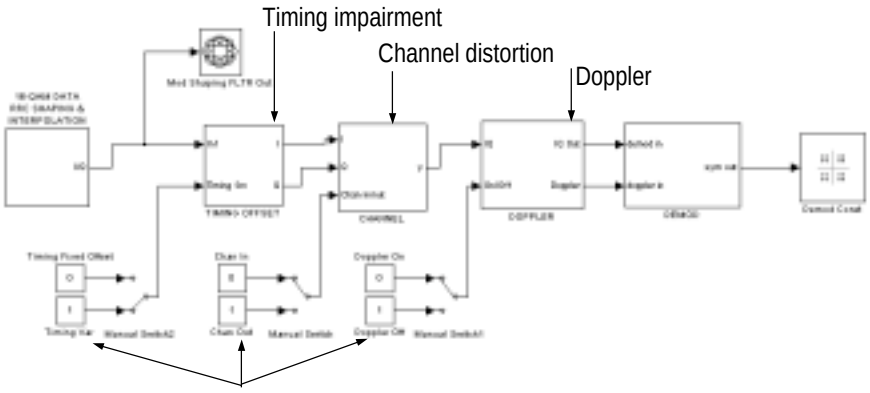
† The small slice count discrepancy is due to logic optimizations that occur when the individual CRL components are integrated into the complete system.)

EQ & CRL Simulation

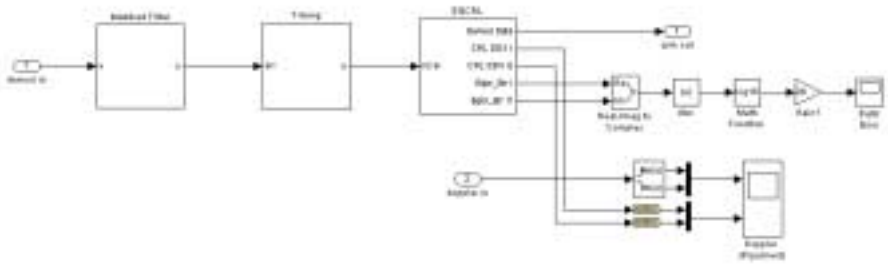


Top Level Design

- Verify demodulator in system level simulation environment



Demodulator

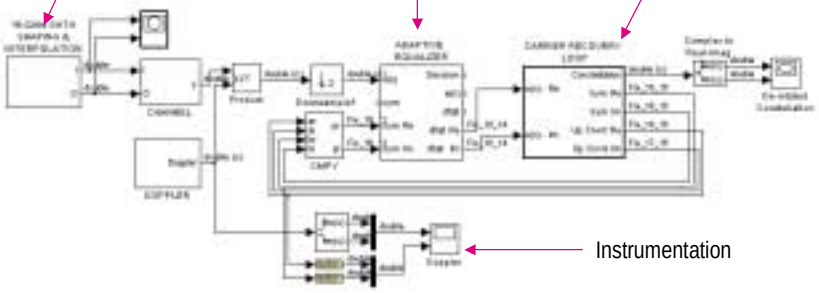


Equalized Receiver Example

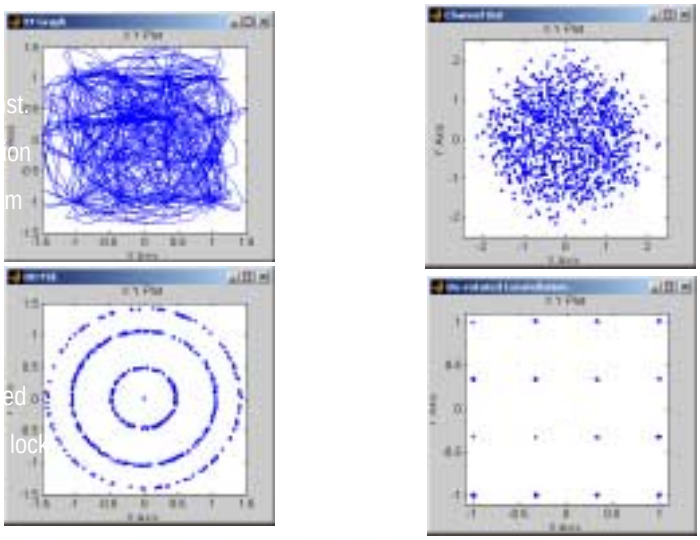
Transmitter Model
- 16-QAM Source
- Matched Filter
- Sample rate Change

Passband Adaptive Equalizer
- Fractionally spaced (T/2)
- Polyphase decimator structure
- LMS coefficient update
- coefficients updated at the symbol rate

Carrier Recovery
- CORDIC based PD



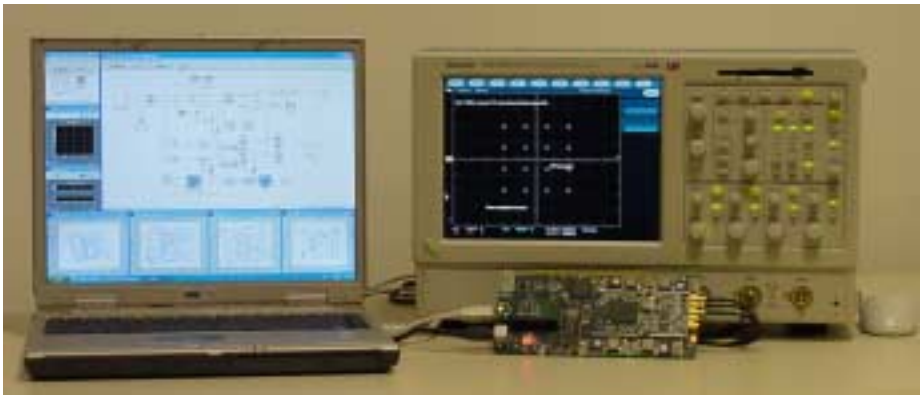
System Generator Simulation



Xilinx DSP Eval Board

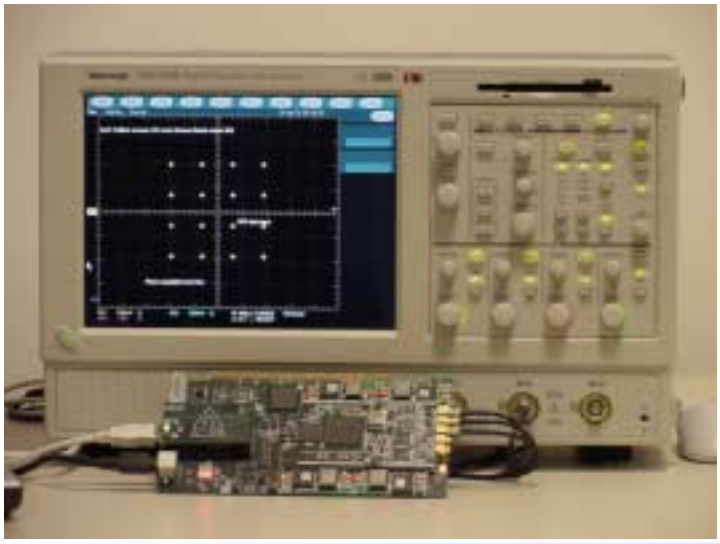
- Virtex-II (XC2V1000/3000)
- Dual A/D D/A
- PCI & USB interface to host system

QAM Demod Simulation



Presentation Name 39

Equalized Signal



Presentation Name 40