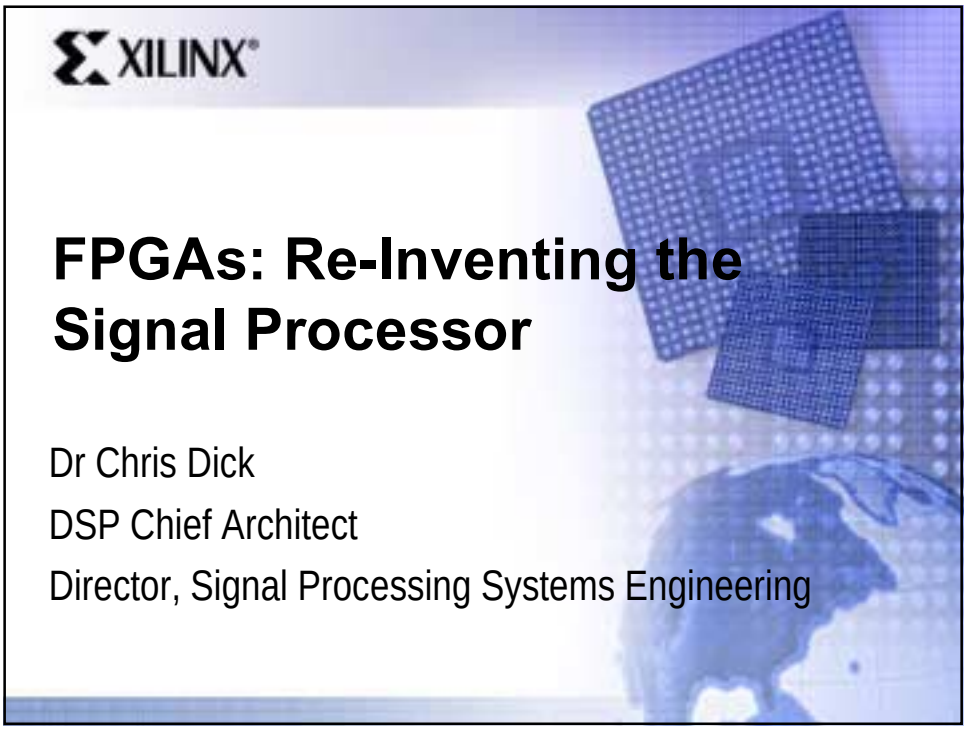


Agenda

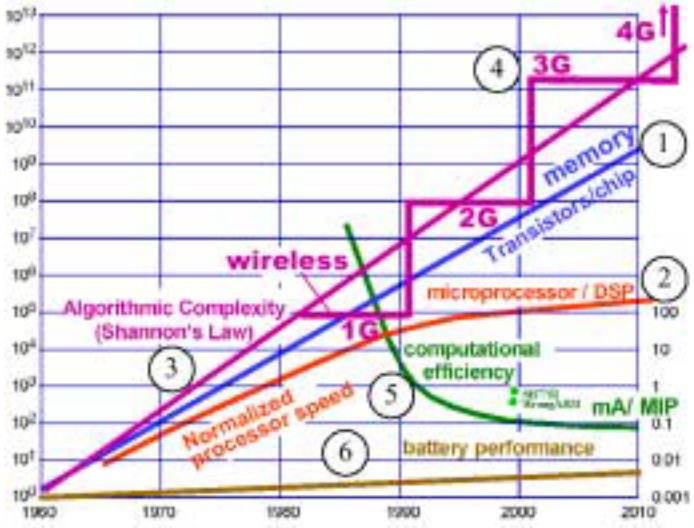
- The FPGA as signal processor
  - High-level perspective
  - FPGA device technology
- Design methodologies for FPGAs
- Design examples
  - Equalized QAM receiver
  - Spectrum channelization
  - OFDM receiver
- Conclusion

Using FPGAs SDRs

- Multiple use models for FPGA-based SDR
- Highly-parallel nature of FPGAs delivers enormous compute power to resource complex signal processing algorithms in SDR PHYs

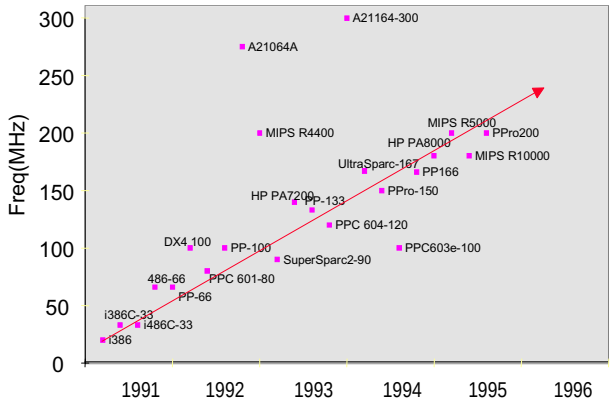
FPGAs: Re-Inventing the Signal Processor 3

Technology Trends



FPGAs: Re-Inventing the Signal Processor 4

Aren't software processors improving with Moore's law?



Primary means of performance increase of software processors is by increasing clock rate

Slide courtesy of B. Brodersen, UCB

Back to the Future

ENIAC

- Tubes: 17,468
- add time: 200 microseconds
- multiply time: 2,800 microseconds
- divide time: 24,000 microseconds
- arithmetic mode: **parallel ... later serial**

- "…This was a highly parallel machine, before von Neumann spoiled it"
  - D. H. Lehmer (1905-1991, U.C. Berkeley), "A History of Computing in the 20th Century"

What is the problem?

The Von Neumann architecture was developed in 1945!!

The assumptions back then

- Hardware is expensive
- Scientific computation is the application
- Cost, size and power are not an issue
- Hardware and software were separate

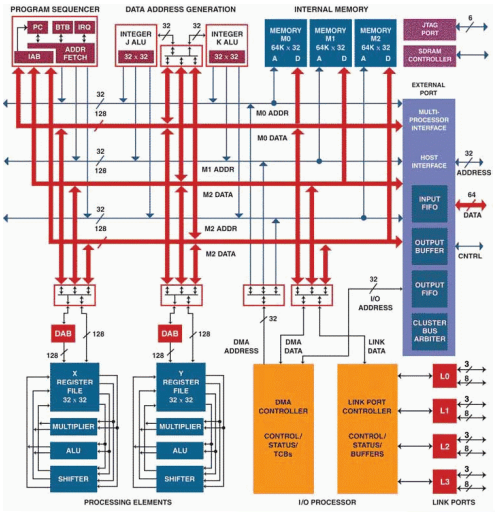
Time sharing the hardware was absolutely necessary

Observation about ISPs†

- Moore's Law brings more than increases in the number of transistors per chip; it also brings dramatic increases in power consumption and power density. If current trends continue, you would have a device with 425 million transistors in 2005 and a processor with 1.8 billion transistors by 2010, said Pat Gelsinger, Intel's vice president and chief technology officer …

  … Even using 0.1-micron technology, Gelsinger envisions a 425-million-transistor die, 40 mm per side, which, clocked at 30 GHz, would dissipate 3,000 to 5,000 watts. In terms of power density, its heat would be close to that of a rocket nozzle, Gelsinger said … "We can't keep building these things with ever increasing power budgets," he lamented.
- Intel technologist cites power as biggest issue, *The Electronic Design, Technology & News Network (EDTN)*, Feb. 6 2001.
- The article is a report on Gelsinger's presentation at ISSCC 2001.

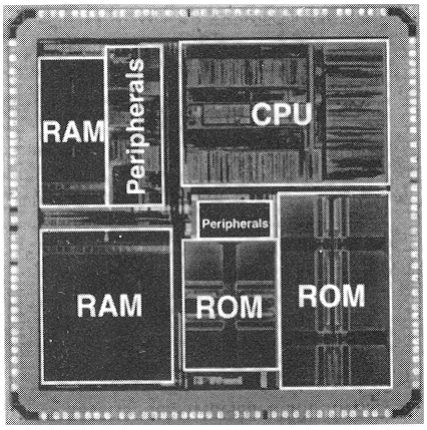
DSP μP: Architectural Limitations



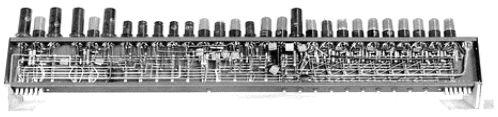
- DSP processor is a (very) close relative of the von Neumann machine
- Sever limitations
  - Functional unit type
  - Number of functional units
  - Functional unit precision
  - Interconnectivity between functional units

Time multiplexing a multiplier … is that a good idea?

DSP processor (25 mm^2)



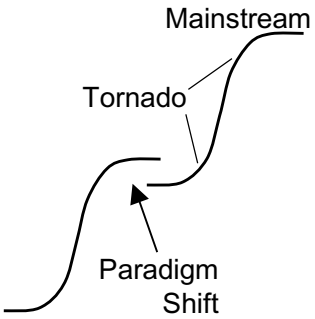
12x12 multiplier (.05 mm^2)

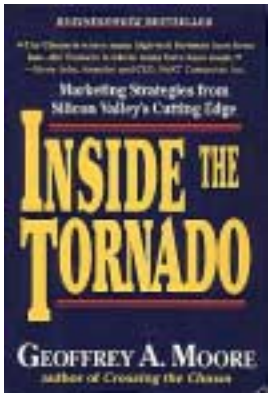


ENIAC: 20b (28 tube) accumulator

We're not in Kansas Anymore

- Development of Hypergrowth Markets





The Si Landscape is Changing

- Semiconductor process technology continues to advance according to Moore's Law
- SIA noted *design gap* 5 years ago
  - Number of transistors that can be put on a die is increasing at a rate of about 60 percent a year
  - Number of transistors that circuit designers could design into new independent circuits is going up at only 20 percent a year

Bass , M. J. and Christensen, C. M., "The Future of the Microprocessor Business", *IEEE Spectrum*, April 2002, pp. 34-39.

The Si Landscape is Changing

- To bring value to a state-of-the-art semiconductor the transistor budget must be used in a different way
  - This is one of the FPGA value propositions
- Christensen
  - Price and performance are still key metrics valued in the market
  - Signs that a seismic shift is occurring giving way to a new era in which customization matters more
- FPGAs are the ultimate in customization
  - Signal processing systems can be constructed that are limited only by the imagination of the designer

FPGAs: Re-Inventing the Signal Processor 13

Computing

- The introduction of the microprocessor caused a 30 year interruption to the significant evolution of computing architectures
- The vN Microprocessor the steam engine of the silicon age [1]
- Reconfigurable devices represent the resumption of the computing technology trajectory

[1] Reiner Hartenstein University of Kaiserslautern

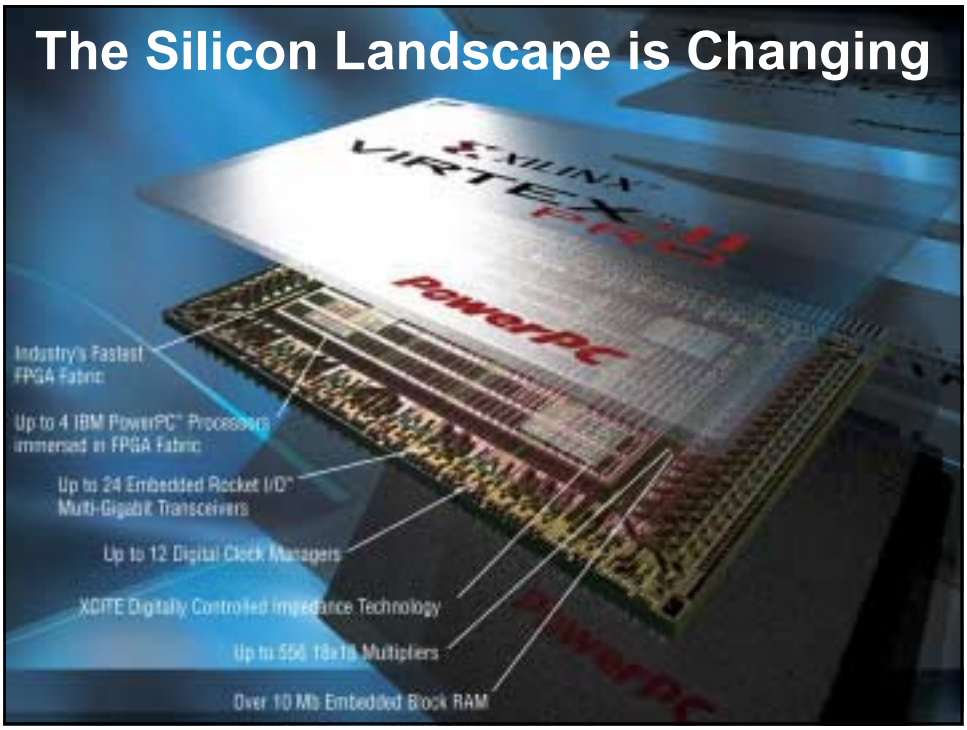
FPGAs: Re-Inventing the Signal Processor 14

Dead Supercomputer Society

- ACRI
- Alliant
- American Supercomputer
- Ametek
- Applied Dynamics
- Astronautics
- BBN
- CDC
- Convex
- Cray Computer
- Cray Research
- Culler-Harris
- Culler Scientific
- Cydrome
- Dana/Ardent/ Stellar/Stardent
- DAPP
- Denelcor
- Elexsi
- ETA Systems
- Evans and Sutherland
- Computer
- Floating Point Systems
- Galaxy YH-1
- Goodyear Aerospace MPP
- Gould NPL
- Guiltech
- ICL
- Intel Scientific Computers
- International Parallel Machines
- Kendall Square Research
- Key Computer Laboratories
- MasPar
- Meiko
- Multiflow
- Myrias
- Numerix
- Prisma
- Tera
- Thinking Machines
- Saxpy
- Scientific Computer
- Systems (SCS)
- Soviet Supercomputers
- Supertek
- Supercomputer Systems
- Suprenum
- Vitesse Electronics

[Gordon Bell, keynote at ISCA 2000].

The Silicon Landscape is Changing



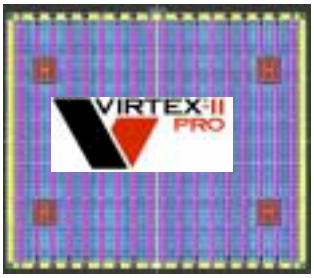
Virtex-II Pro Family

Device XC		2VP2	2VP4	2VP7	2VP20	2VP30	2VP40	2VP50	2VP70	2VP100	2VP125
Logic Cells		3,168	6,768	11,088	20,880	30,816	43,632	53,136	74,448	99,216	125,136
PPC405		0	1	1	2	2	2	2	2	2	4
MGT3.125Gb		4	4	8	8	8	12*	16*	20	20*	24*
BRAM (kbits)		216	504	792	1,584	2,448	3,456	4,176	5,904	7,992	10,008
Xtreme Mult.		12	28	44	88	136	192	232	328	444	556
DCMs		4	4	4	8	8	8	8	8	12	12
Package	Pitch	Available SelectI/O									
FG256	1.00	140	140								
FG456	1.00	156	248	248							
FF672	1.00	204	348	396							
FF896	1.00			396	556	556					
FF1152	1.00				564	692	692	692			
FF1148*	1.00						804	812			
FF1517	1.00						804	852	964		
FF1704	1.00								996	1040	1040
FF1696*	1.00									1164	1200

*** FF1148 and FF1696 special bond option: NO MGT with Maximum SelectI/O**

FPGAs: Re-Inventing the Signal Processor 17

FPGA Families



- Industry's most used FPGAs for DSP
- Highest performance DSP
  - Up to 556 hard embedded 18x18 multipliers
  - Up to 10MBit of dual port block RAM
  - Up to 4 PPC 405 processors for control
  - 3.125 Gbps serial transceivers
- Ideal for multi-channel designs

- Industry's lowest cost FPGA
  - 90 nm process
  - 300mm wafers
- High performance DSP
  - Up to 104 hard embedded 18x18 multipliers
  - Up to 2MBit of dual port block RAM
  - 32-bit MicroBlaze™ µP

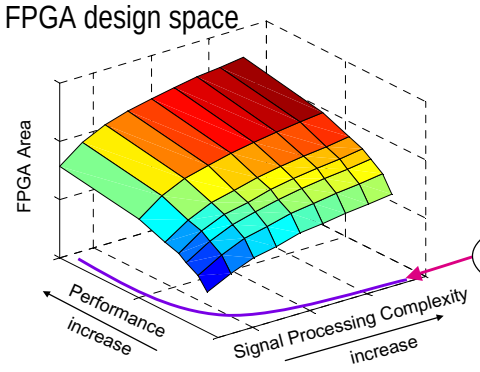
FPGAs: Re-Inventing the Signal Processor 18

Adding Parallelism in Conventional DSP Solutions

- New DSP architectures such as VLIW and super-scalar have one goal: provide higher degrees of parallelism
- Architecture evolution along the same design axis is not scalable
  - Too many MAC functional units makes programming, compilers and scheduling an issue
- The effective computing per chip area decreases
  - Memories grow geometrically while the datapath does not

FPGA Customized Datapaths

- Design tradeoffs and optimization in (design)-real-time



• FPGAs: Design the architecture for the algorithm
• ISA: Map the algorithm to the architecture

Instruction set architecture (ISA) design plane

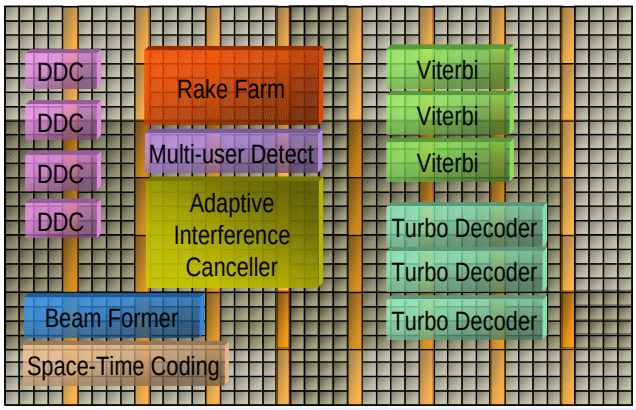
DSP Functions Implemented in FPGAs

Multirate filters, including Pulse shaping/interpolation, Matched filters/decimators: wireless, 3G BTS, SDRs, satellite, microwave, cable	Entire M-ary QAM modulators and demodulators including - High data rate equalizers: FFE, DFE, blind - Synchronization: Carrier Recovery, timing Recovery
Digital down- and up-conversion (DDC, DUC)	Multiple-input-multiple-output (MIMO) signal processing functions
Direct digital frequency synthesis	Fast Fourier transforms for OFDM and spectrum channelization
Radio spectrum channelization	Source coding (MPEG4/7) for image transport streams
Rake receiver	Space-time coding
Beam forming	Multi-user detection in 3G UMTS radios
Adaptive interference cancellers in 3G UMTS radios	Encryption/decryption
Digital pre-distortion for power amplifier linearization: 3G wireless	Peak-to-average control in OFDM transmitters: 4G wireless transmitters
Sinc correction for the digital-to-analog (DAC) in a wireless transmitter	Forward Error Correction: Convolutional codes, Viterbi decoding, R-S encoding and decoding, Turbo convolutional/product codes

FPGAs: Re-Inventing the Signal Processor 21

The Power of Parallelism

- In FPGAs we can exploit the large amounts of parallelism inherent in many DSP data paths



FPGAs: Re-Inventing the Signal Processor 22

FPGAs = Performance (1)

- 12 concurrently operating 64-tap filters
- 8-bit MACs – 8-bit data, 8-bit coefficients†
- Sample Rate (fs) = 154 MHz
- 13,704 slices (95% of device)
- 118 Billion MACs/s
- I/O bandwidth = 237 Giga-bytes/s

Virtex-II XC2V3000-5 with 14,336 slices

† Optimized for coefficient set

Software Radio Architecture

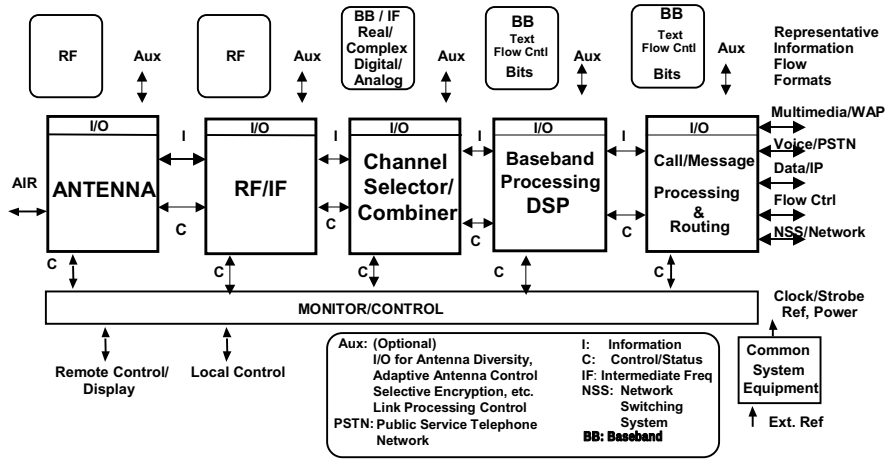
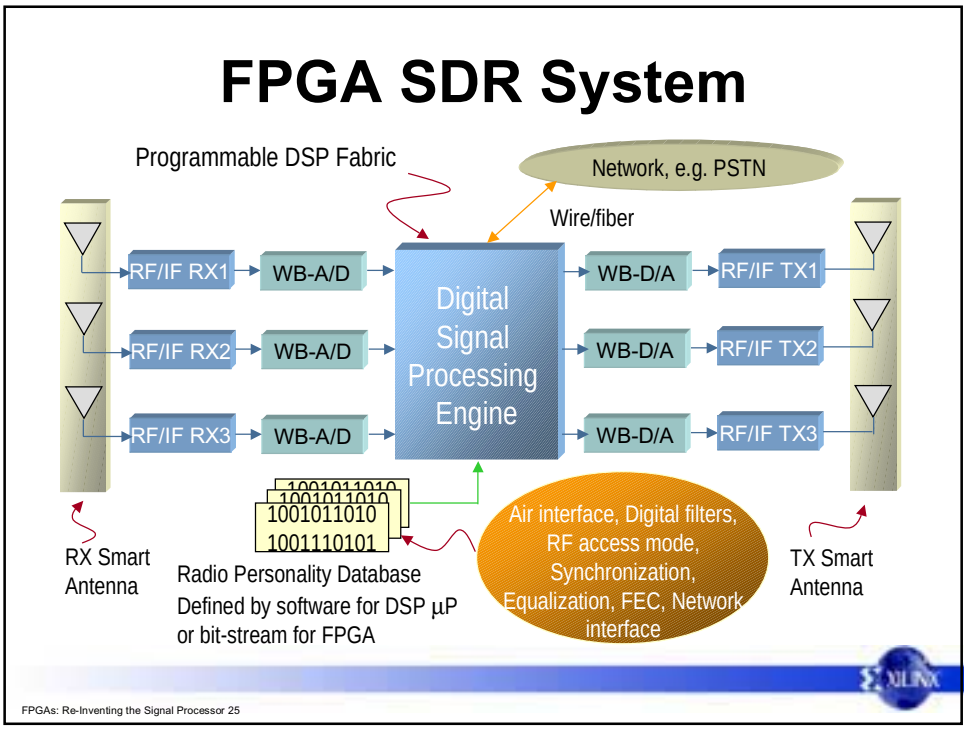
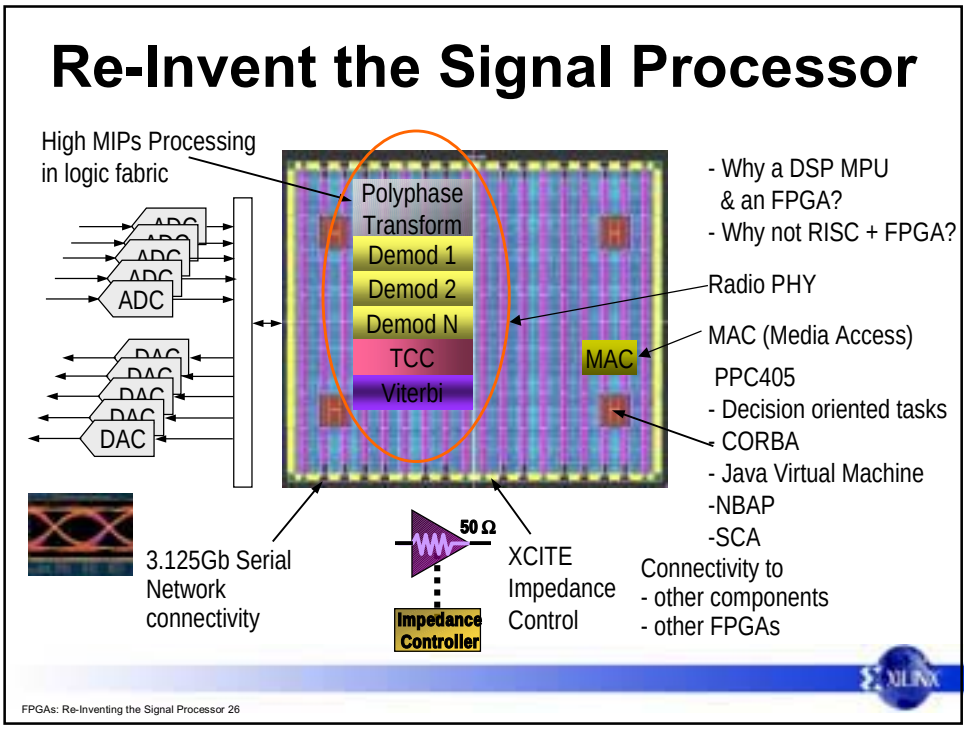
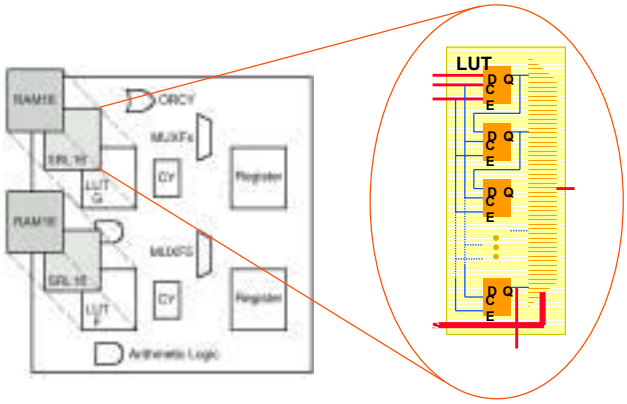


figure used with the permission of the SDR forum: www.sdrforum.org





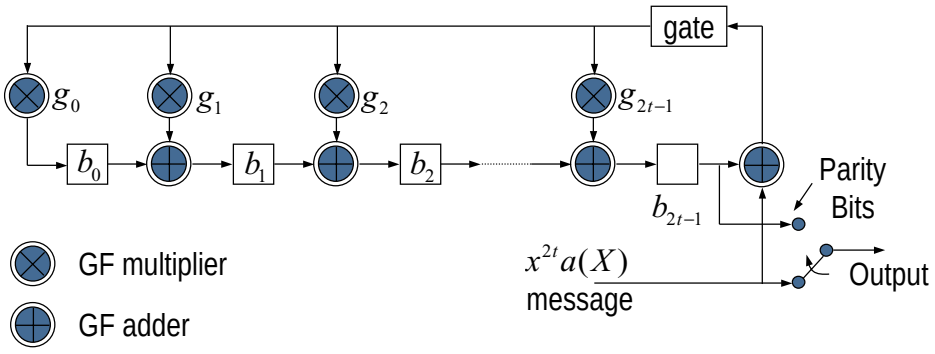
Increasing Compute Density



- SRL16 can dramatically increase FPGA compute density by enabling the construction of efficient TDM hardware structures
- Enables highly efficient implementations of multi-channel datapaths
- Unique to Xilinx FPGAs

Single-Channel Processing Example - RS Encoder

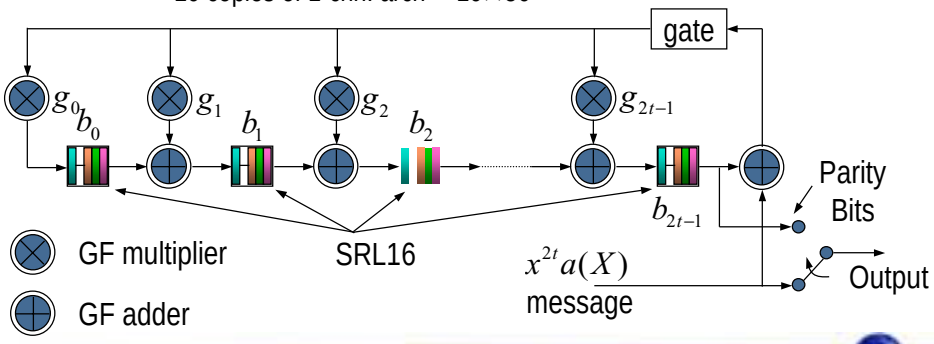
- 1 Channel (128,122) R-S encoder
  - 56 slices



Efficient Multi-channel RS-Encoder

- 16 Channel (128,122) R-S encoder
  - 89 slices

$$\frac{\text{16-chn arch}}{\text{16 copies of 1-chn. arch}} = \frac{89}{16\times 56}\times 100 = 10\%$$



Xilinx DSP IP Library Leverages SRL16 Capability

- This Xilinx unique capability is applied in our DSP IP libraries
  - Multi-channel Viterbi decoder
  - Multi-channel R-S encoder/decoder
  - Multi-channel multirate FIR filters
  - Modulator
    - J.83 modulator in DSP IP library – new member

Extensive IP Core Library to Accelerate Productivity

- FFTs
  - 16 - 64K point complex FFT
    - Fixed-point datapath
    - Block floating-point datapath
- Filters
  - Distributed arithmetic FIR filter
  - CIC filter
  - Multi-channel FIR filter
  - Multirate filters
    - Decimators
    - Interpolators
- Direct Digital Synthesizer
  - >115 dB spurs
- CORDIC arithmetic unit
  - Math functions: rect->polar, sqrt, atan2,…
- Forward Error Correction (FEC)
  - Reed-Solomon encoder/decoder
  - Convolutional encoder
  - Viterbi decoder
  - Interleaver/de-interleaver
  - Turbo product code encoder/decoder Turbo Convolutional Codec
    - 3GPP
    - CDMA2000
- Cable modem modulator
- Digital down converter (DDC)
- Digital up-converter (DUC)

Reference Slides

- The subsequent slides provide an overview of selected modules in the Xilinx IP portfolio

Viterbi v3.0 (1)

- Very Fast
  - Using new arithmetic technique in ACS unit
  - For constraint length 7
    - 147 MHz V2-5
    - 175 MHz V2-6
    - 183 MHz V2p-6
    - 203 MHz V2p-7

	Xilinx Area Optimized v2p-7	Xilinx Speed Optimized v2p-7	Altera Stratix
Area	1170 slices	2905 slices	1961 LE's
Speed	162 MHz	203 MHz	159 MHz

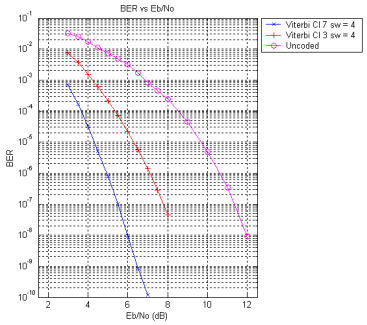
  - Area optimization can also be selected for lower speed but much smaller size.
  - Serial option gives extremely small Viterbi if throughput is low
- Multi-channel
  - Uses SRL16 technique. Only a small increase in size. Can be clocked at ~280 MHz (V2-6)
  - Can handle up to 32 interlaced channels with one Viterbi decoder

Viterbi v3.0 (2)

- Reduced latency
  - Latency reduction option, cuts the previous latency in half
  - Important for some modem standards
  - Only available with area optimized or multi-channel Viterbi.
- Trellis mode
  - Allows the user to cost the decoded data externally to decoder
  - Means core can accommodate advanced modulation schemes
- Erasure extension
  - Erasure can now be used with any rate decoder i.e. from 1/2 to 1/7, previously only available on rate 1/2
- Best State
  - Best state at start of traceback now available as an option on the core
  - Latency can be reduced for punctured codes

Viterbi v3.0 (3)

- Full AWGN examples available with Sysgen Pro running on the Xtreme DSP Development Kit
- Running with Matlab interface on Xtreme DSP Development kit with Xilinx AWGN core:



CDMA2000 TCC (1)

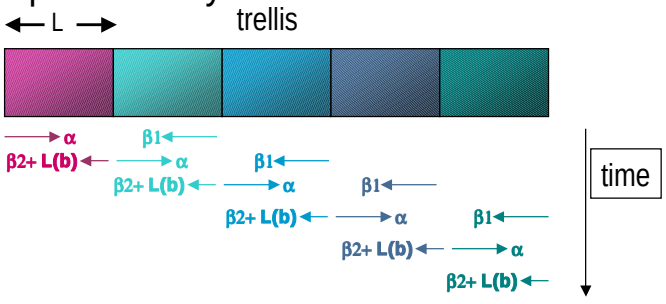
- Implements the 3GPP2 (CDMA2000) specification
- Contains the full 3GPP2 interleaver
  - Supports block sizes 378-20730
- Supports all code rates and puncture patterns
- Implements the MAX* or MAX scale algorithm
- User configuration of numerical precision
  - Area/speed can be traded off against BER
  - Twos complement fractional soft data used
- Drop-in module for Virtex-II™ and Virtex-II Pro™ FPGAs

CDMA2000 TCC (2)

- FPGA footprint
  - 1490 slices
  - 15 block memories
  - 2 hardware multipliers
- Max clock Rate = 90-110MHz
- Block size = 378
  - 3 iterations: 12.5 Mbits/s
- Block size = 20730
  - 3 iterations: 14.5 Mbits/s
  - 5 iterations: 9 Mbits/s
- Throughput can be increased by using multiple decoders in parallel

TCC Window-Based Decoding

- Calculate metrics in blocks of L symbols
- Double beta metric calculation
- Small alpha memory

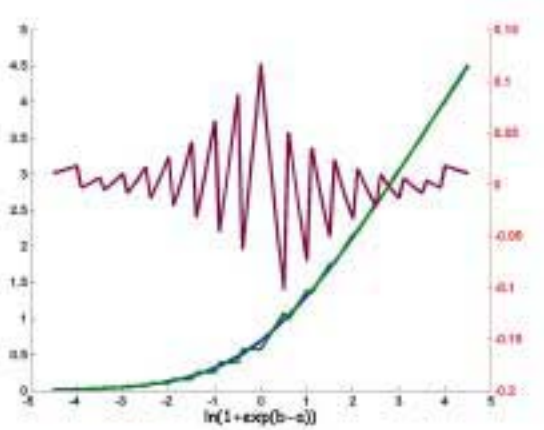


Max* = Log(sum_of_exp())

$\ln(e^a+e^b) = a + \ln(1+e^{(b-a)}) = b + \ln(1+e^{(a-b)}) = \max^*(a,b)$

$a >> b : \ln(1+e^{(b-a)}) \approx 0$
$b >> a : \ln(1+e^{(a-b)}) \approx 0$

Max*=max(a,b)+offset
offset = table, 8 entries
if -4 < (b-a) < 4



Log-Max Soft ACSO

$\ln(e^a+e^b) = a + \ln(1+e^{(b-a)}) = b + \ln(1+e^{(a-b)}) = \max^*(a,b)$

$a >> b : \ln(1+e^{(b-a)}) \approx 0$
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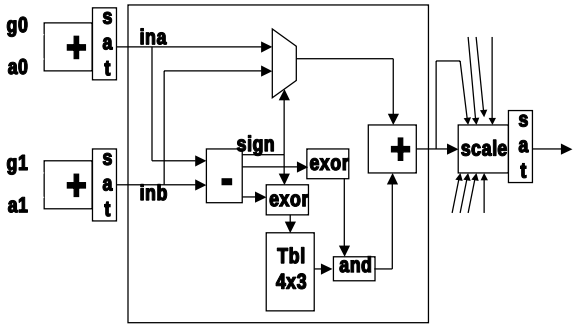
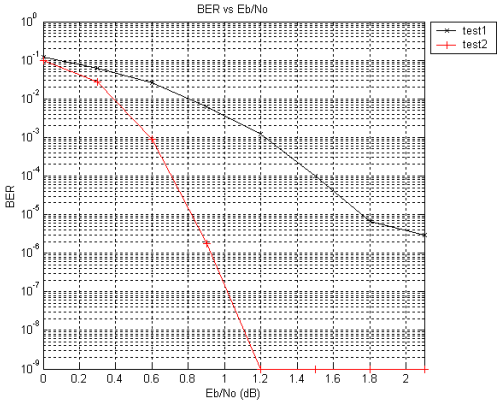
Max*=max(a,b)+offset
offset = table, 8 entries
if -4 < (b-a) < 4



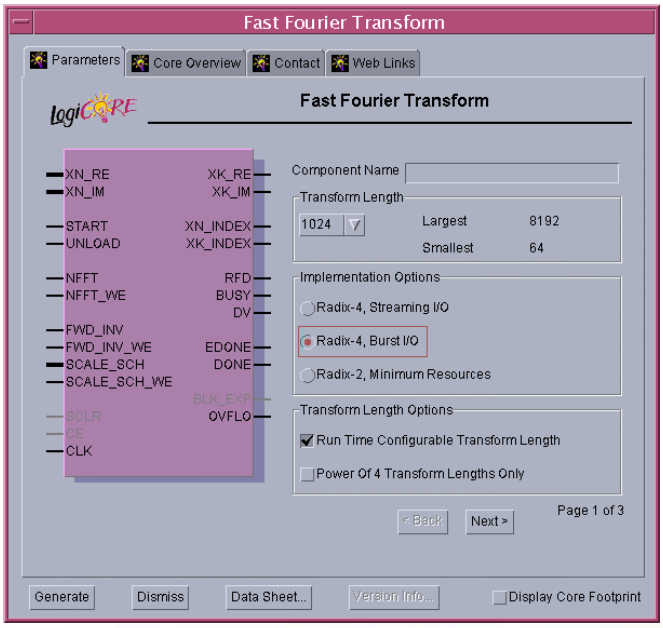
CDMA2000 TCC (3) Performance



- Test1=block size 378. Test2=block size 4602. Iterations =5.
- Input width = 2 integer bits, 4 fractional bits
- Internal width = 6 integer bits, 3 fractional bits

FFT

- FFT
  - Applications
    - OFDM mod/demod
    - Imaging radar
  - N=16, 32,…,8192, 65536
  - Parameterized on
    - Input data precision
    - Phase factor precision
  - 3 Area/performance tiles
  - Arithmetic
    - Scaled Fixed-point
    - Unscaled/full-precision fixed point
    - Block Floating point
    - Convergent/truncation rounding
  - Simple interface
  - Memory embedded in module
  - Multiple point sizes accommodated by one core
  - Increase performance and numerical quality over previous designs
  - Radix-4 decomposition employed for $N=r^4$
  - Mixed radix for other point sizes to achieve high performance
  - Radix-2 engine used for implementation with smallest FPGA footprint

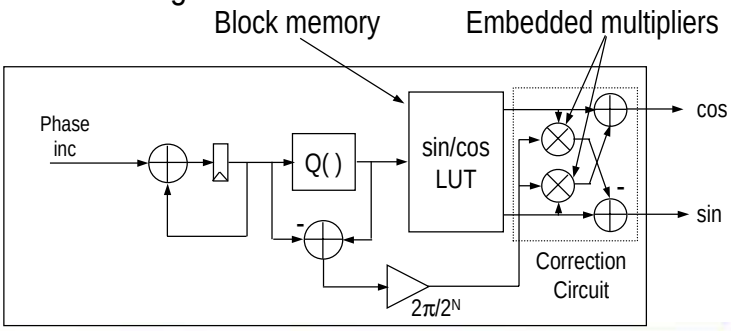


DDS (1)

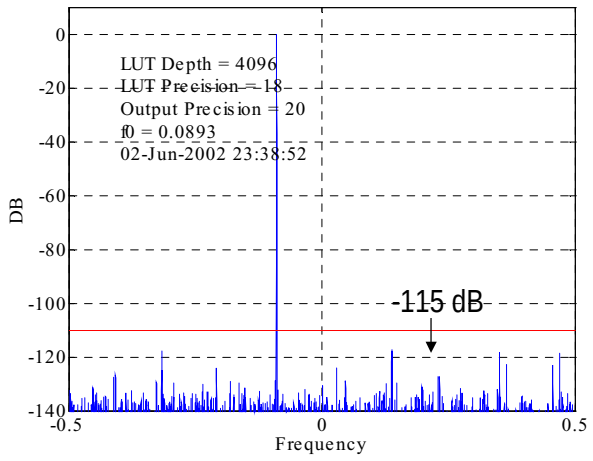
- New DDS
  - Improved max fclk
  - Taylor series correction
    - -115dB SFDR
    - 315 slices, 1 block memory, 2 embedded 18x18 mpys
  - Multi-channel support
    - Single DDS servicing multiple DDCs/DUCs

DDS(2)

- Direct digital synthesizer (DDS), SFDR = -115 dBC
  - DDC
  - DUC
- 1 Channel design

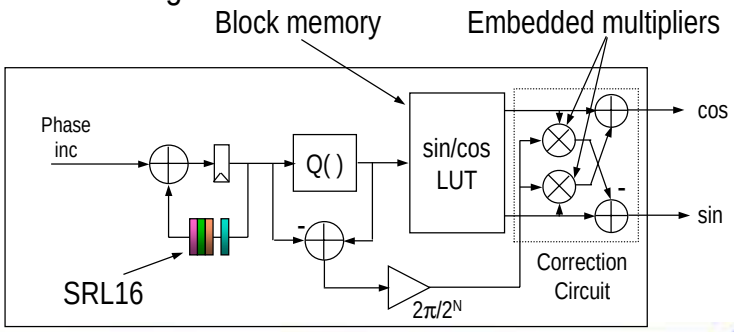


DDS (3) - SFDR



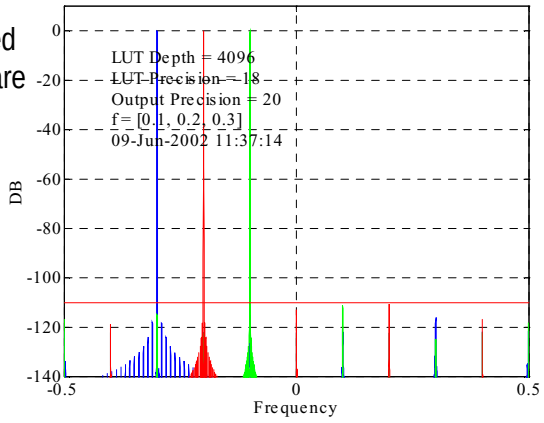
DDS (4)

- Direct digital synthesizer (DDS), SFDR = -115 dBC
  - DDC
  - DUC
- N Channel design

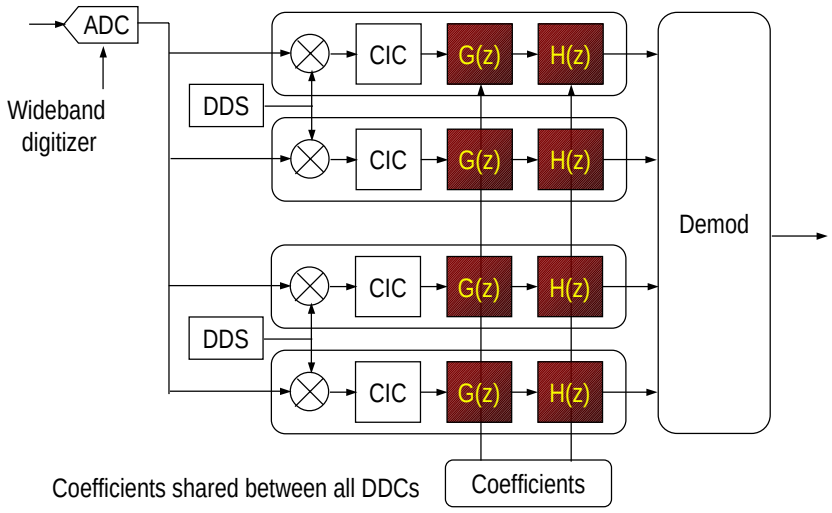


DDS (5)

- 3 tones efficiently generated by time sharing the hardware
- Sample-rate versus area tradeoff



DDS Used in DDC



Multirate Filters

- MAC FIR
  - New features and fclk max improvements
  - Reduced area
  - Polyphase
    - Decimator
      - Multi-channel
    - Interpolator
      - Multi-channel
  - Symmetry utilized (optional) for efficient implementation
  - Multi-MAC architecture support

CORDIC v2.0 (1)

- Considerably Enhanced Parameterization:
  - Optional instantiation of coarse rotation module
  - Input and output widths can be independently configurable
  - Parameterized control of number of micro-rotation iterations
  - Parameterized control of internal precision
  - Optional ND (New Data) signal
  - Optional input and output registers
  - New rounding modes added

CORDIC v2.0 (2)

- Improved Pipelining
  - New pipelining mode - “No Pipelining”
  - Pipelining mode now applies to whole CORDIC implementation
- New Data Formats for Square Root Functional Configuration
  - New Data Formats: “Unsigned Fraction” and “Unsigned Integer”
- Compensation Scaling
  - New “Block Multiplier” option for compensation scaling using the built in 18x18 multiplier

RS Encoder v4.1 (1)

- Variable block length (n)
  - Can be used with standards like ETSI-BRAN
- Multi-channel
  - Uses SRL16 technique. Very little increase in size for up to 17 channels
- Supports ITU J.83 Annex B
  - Additional auxiliary circuit for 128th symbol is included in core
- Already in use in Universal Modulator and ETSI-BRAN project
- Available in Coregen G.IP1. Alpha netlists available now.

RS Encoder/Decoder v4.1 (2)

- Variable block length (n)
  - Efficient buffering scheme still allows continuous throughput
  - Can be used with standards like ETSI-BRAN
- Multi-channel encoder
  - Uses SRL16 technique - very little increase in size for up to 17 channels
  - e.g. 16 channel RS Encoder takes around 90 slices => 6 slices per Encoder!
- Encoder now fully supports ITU J.83 Annex B
- Ease of use improved - handshaking signals added (ND, RDY, RFD, RFFD), true Clock Enable

Interleaver v3.1

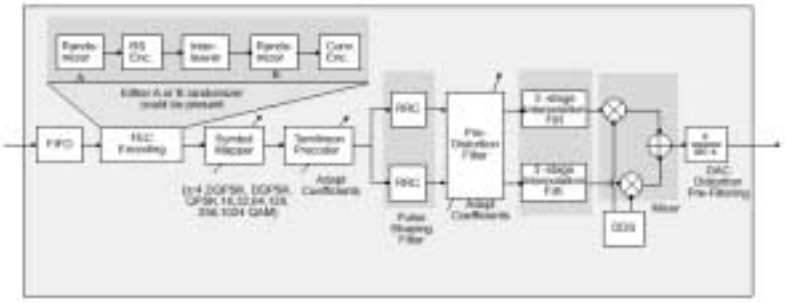
- External symbol RAM option added
- Multiple Convolutional Interleaver configurations supported
  - Can be used with standards like ITU J.83 Annex B & CDMA2000
  - Complete J.83 interleaver is only 124 slices + 2 block RAMs (using external symbol RAM).

ITU J.83 Annex B Modulator (1)

- Drop-in Module for VII and VIIPro.
- Has Clock Management.
- Tested on Xilinx/Nallatech XtremeDSP Kit with External
  - ZBT SRAM
- Single channel features
  - Programmable interleaver control
  - Zero switching time between 64/256 QAM
  - Optional External single port ZBT SRAM interface

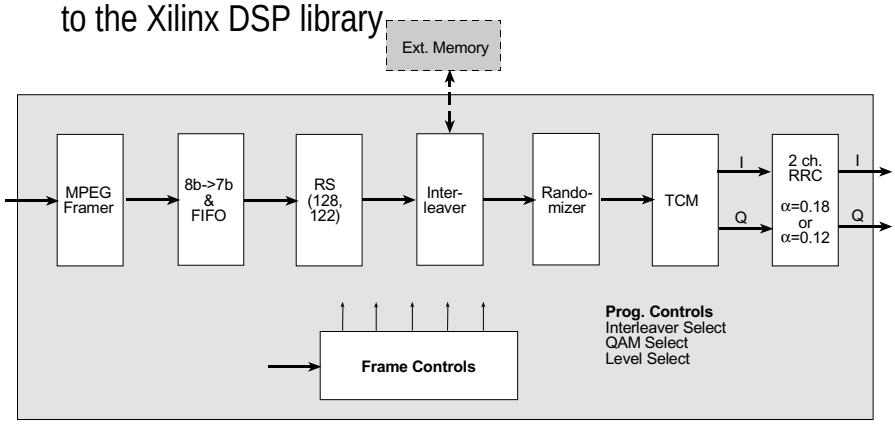
Universal Modulator (2)

- J.83 annex B beta netlists being delivered now
- Annex A & C to follow



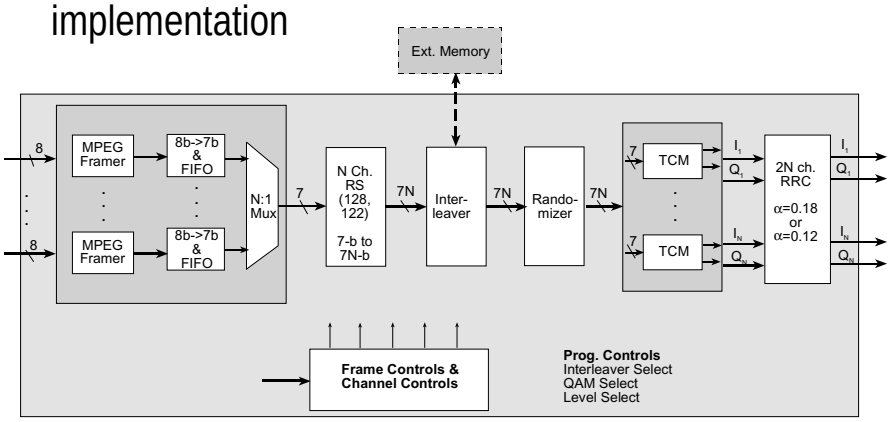
ITU J.83 Annex B Modulator (3)

- Cable modem downstream modulator is a new addition to the Xilinx DSP library



N-Chan. ITU-T J.83 Annex B Mod. (4)

- SRL16s used to realize minimum area multichannel implementation



J.83: Resource Utilization

	1 channel	4 channel		8 channel		12 channel		16 channel	
Granularity per Group		1 channel	4 channel	1 channel	4 channel	1 channel	4 channel	1 channel	4 channel
Slices	862	3,249	1,758	6,483	3,459	9,625	5,156	12,947	6,839
BRAMs	2	8	2	16	4	24	6	32	8
BUFGs	2	2	2	2	2	2	2	2	2
DCMs	2	2	2	3	2	3	2	5	2

Resource Utilization excluding RRC

Xilinx DSP Eval Board

- Virtex-II (XC2V1000/3000)
- Dual A/D D/A
- PCI & USB interface to host system