System-Level Design for Software Defined Radio

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Agenda

- MathWorks products for system-level design of SDR
- Introduction to Simulink
- Case Studies:
  - Ultra-Wideband Radio
  - Digital Down Conversion
- HDL Verification and Co-simulation
  - Link for ModelSim
- Case study: SSB Software Defined Radio
  - Partition design into FPGA + DSP processor
  - Live demo: real-time FPGA/DSP implementation

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Today's System Design Challenges

- Increasing complexity of wireless technology
  - Multi-band, multi-standard, multi-target
- Time-to-market pressure
  - Design verification occurs late
  - High risk of design failure and time-to-market delays
- Design team integration
  - Geographically diverse teams
  - Analog/Mixed-Signal, digital hardware, DSP S/W, control S/W

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Problem: "Joint" or Shared Radio Systems

- Wireless interface to Wireline, Sensors, Surveillance Systems
- Many military and commercial standards
- Millions of radios
- Multi-service integration
- Increased need:
  - Standardize
  - Continue to support legacy systems

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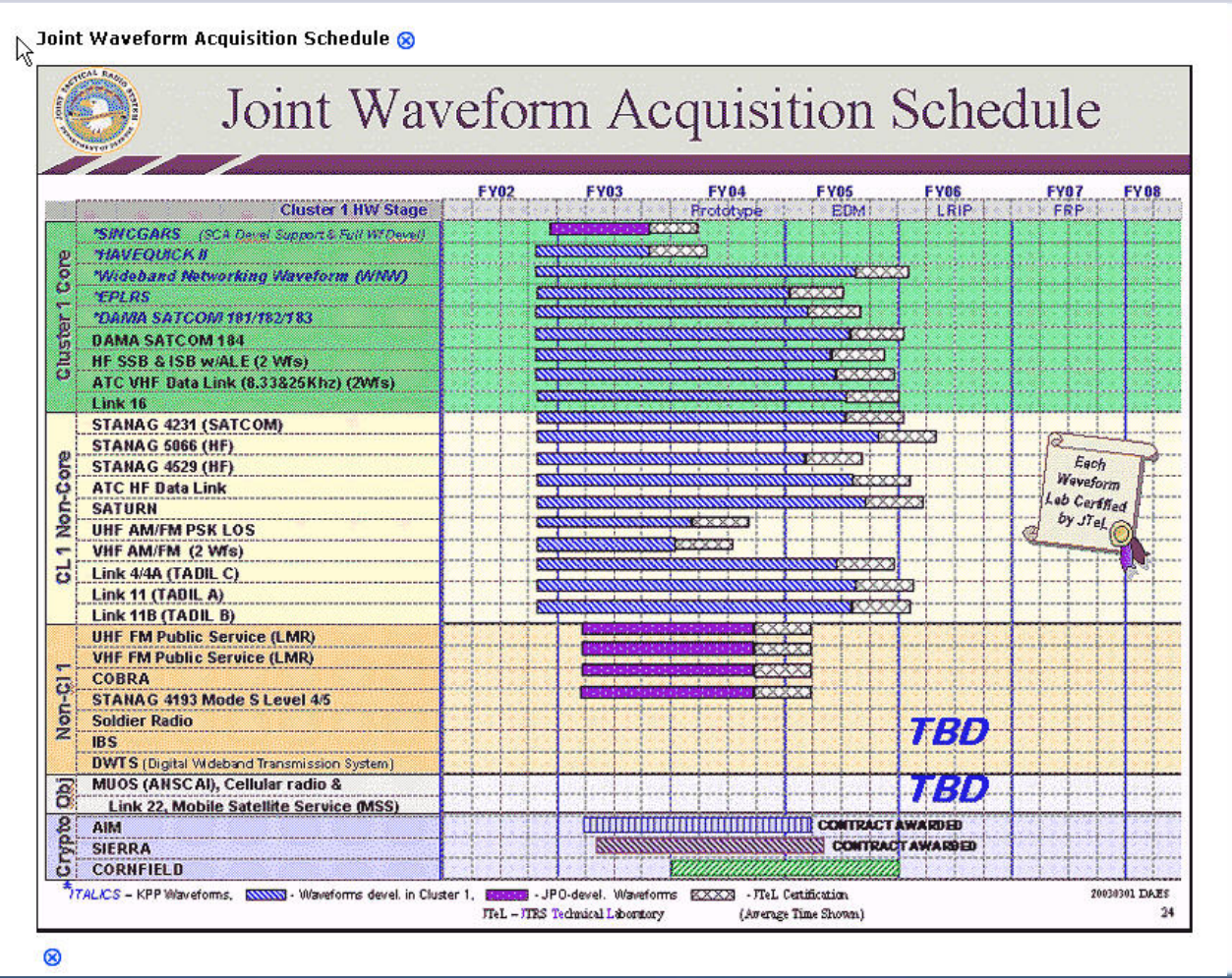
Example: JTRS Timeline Pressure



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Challenges for Software Radio

- **System Design**
  - Modular and hierarchical hardware/software, analog/digital design
- **Component and Algorithm Design**
  - Configurable, tunable, reusable, computationally efficient filters
  - Wide and multi band, CDMA, multi-carrier components
    - **ADCs, VCOs, Power Amplifiers**
  - Increasingly complex algorithms
    - **Multi-rate and fixed-point algorithms**
    - **More complex synchronization, interpolation, decimation, equalization**
- **Implementation on programmable hardware**
  - **Code generation for DSPs/FPGAs/General purpose processors**

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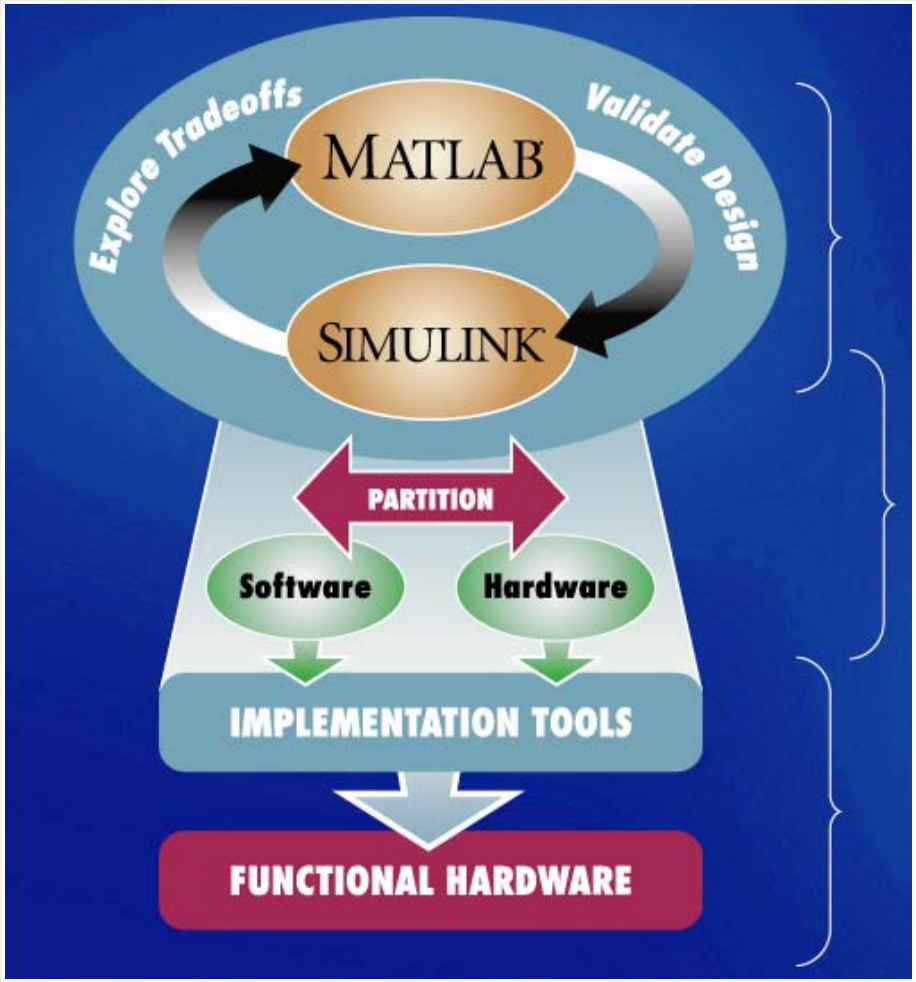
MathWorks Products for System-Level Design



- Create and validate design
- Detect design flaws early
- Reduce risk and time-to-market
- Use Simulink model as reference and executable specification

- Partition Design
- Add Implementation Detail

- Complete design flow to hardware (FPGA + DSP)

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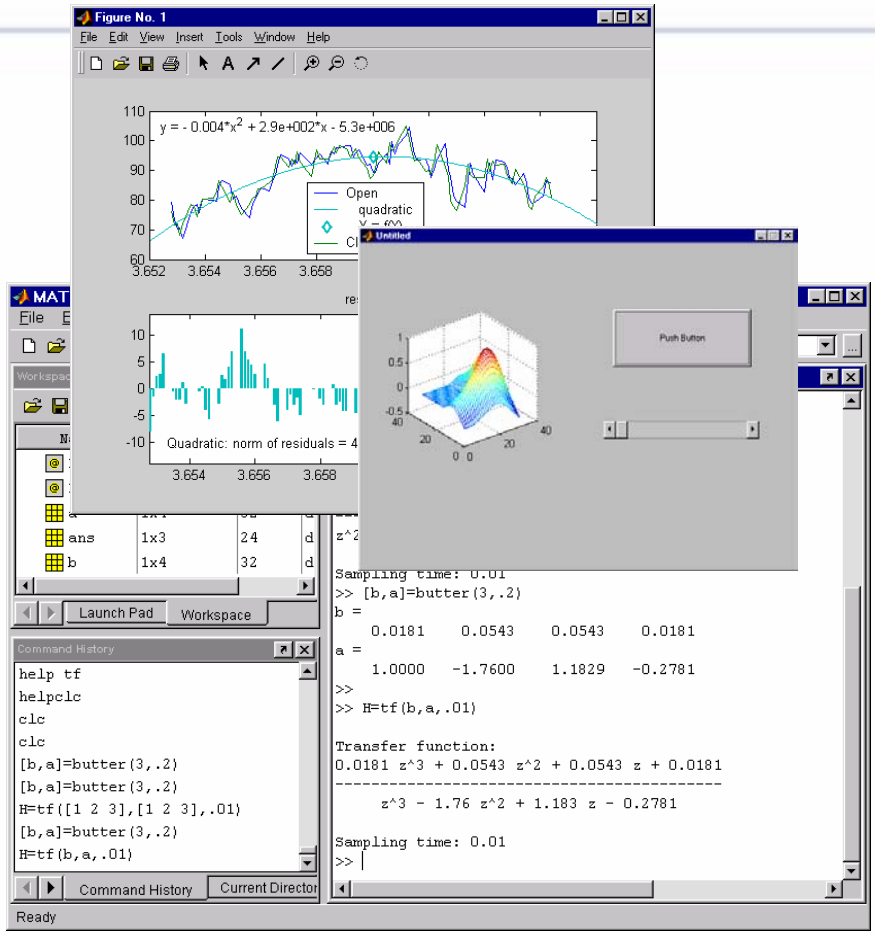
MATLAB

- **MATLAB** is the leading software tool for DSP algorithm development
- Perform mathematical modeling
- Develop algorithms
- Acquire, visualize and analyze data



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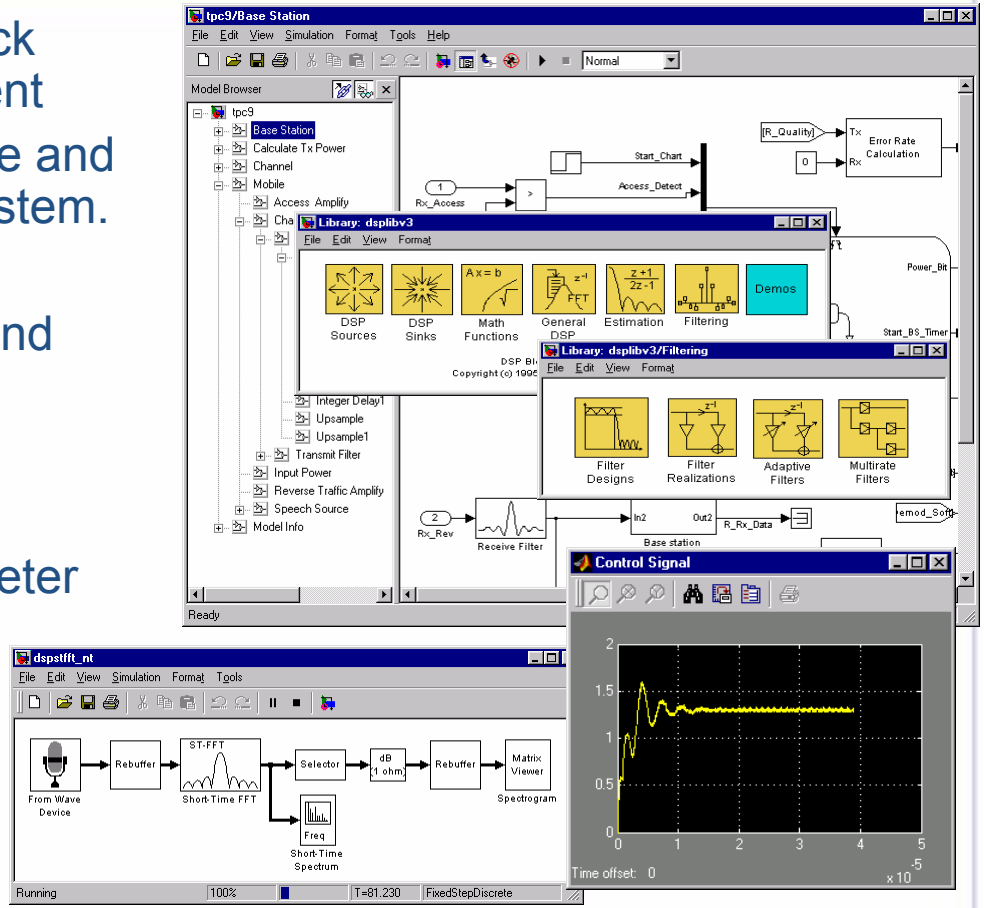
Simulink

- **Simulink** is an interactive block diagram simulation environment
- Graphically design architecture and simulate behavior of whole system.
- Bit-true cycle accurate.
- Digital, analog/mixed signal, and event-driven
- Libraries of pre-built blocks
- Import C or MATLAB Code
- Test, optimize, explore parameter & architecture trade-offs



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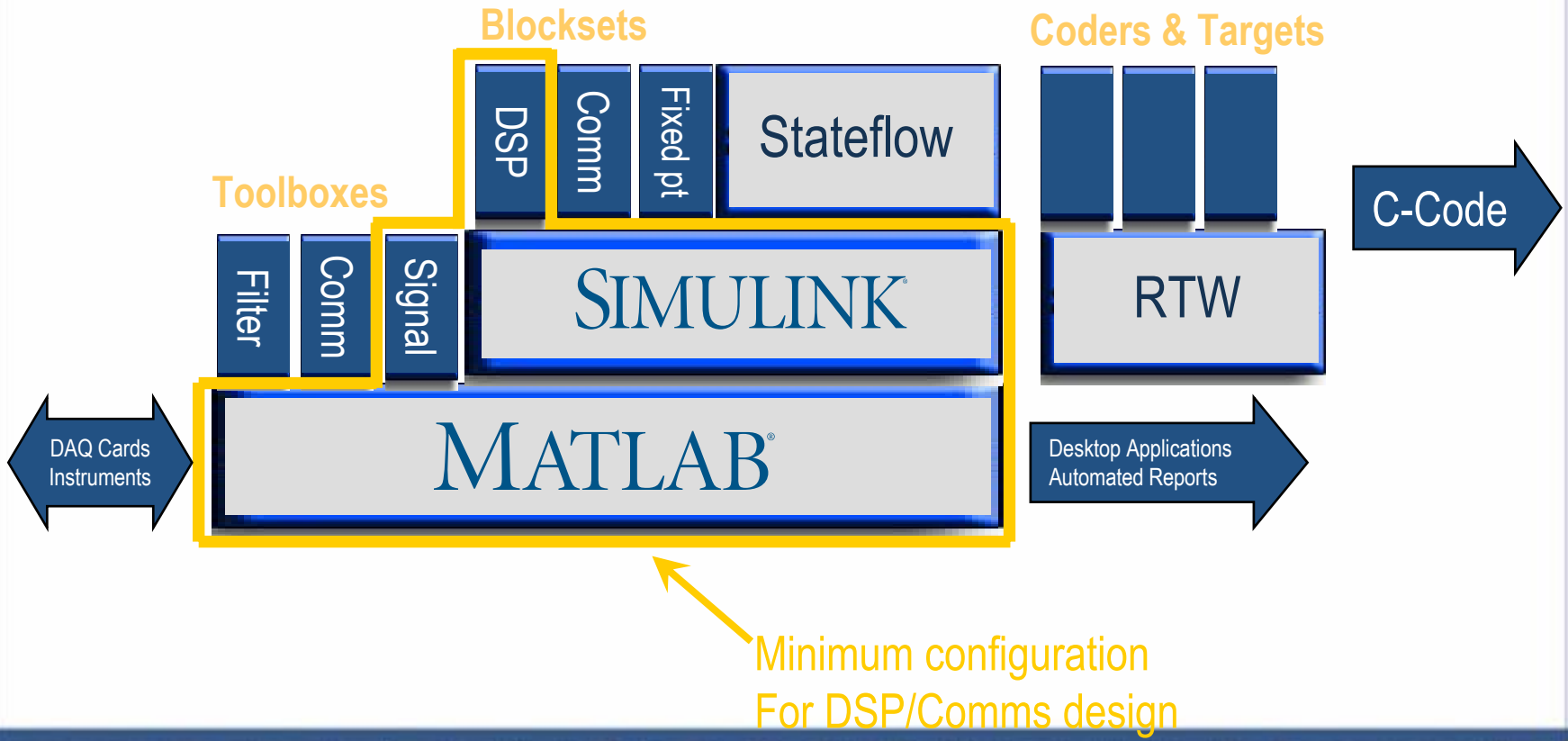
MathWorks Product Family



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Simulink Tutorial

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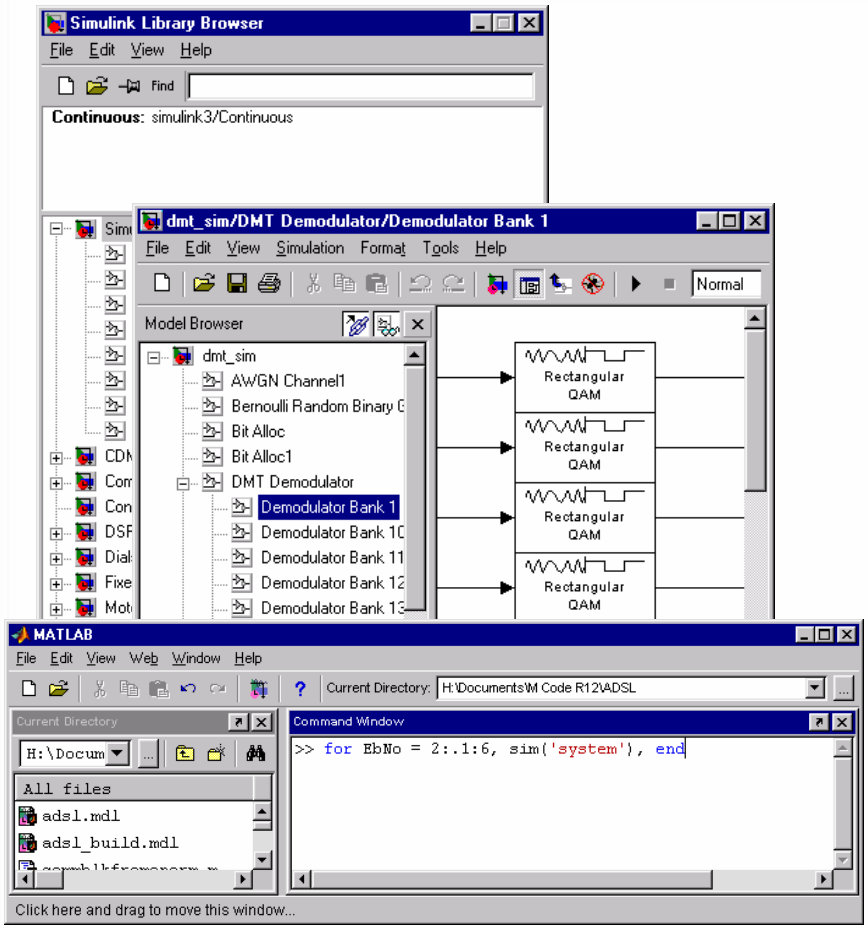
Tutorial Topics



- The block libraries
- Model construction
- Subsystems and hierarchy
- Complex timing & concurrency
- Custom blocks and libraries
- Multi-rate and analog
- Data types

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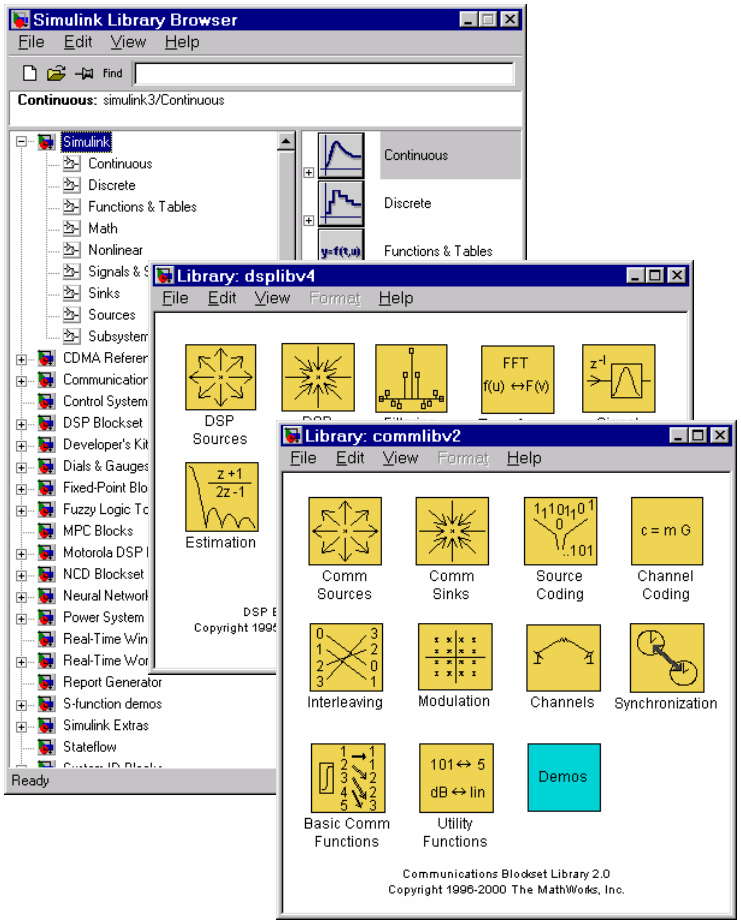
The Block Libraries



- Simulink
  - Sources
  - Sinks
  - Continuous
  - Discrete
  - Non-Linear
  - Math
- Key Blocksets
  - DSP
  - Communications
  - Fixed-Point

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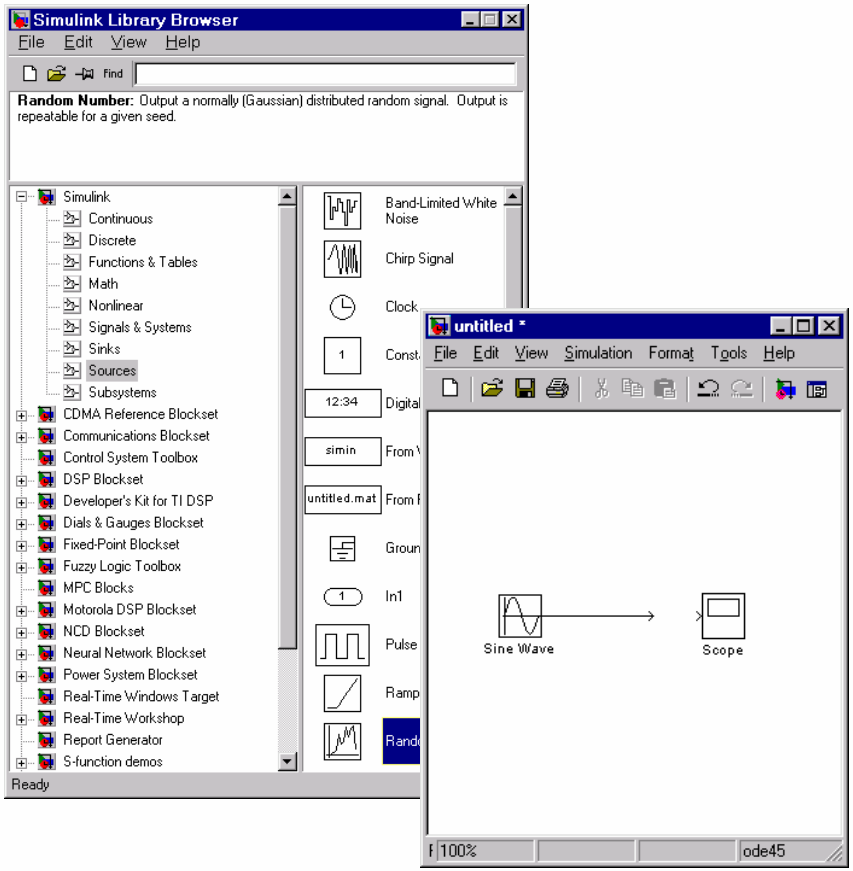
Model Construction



- Drag and drop
- Connect

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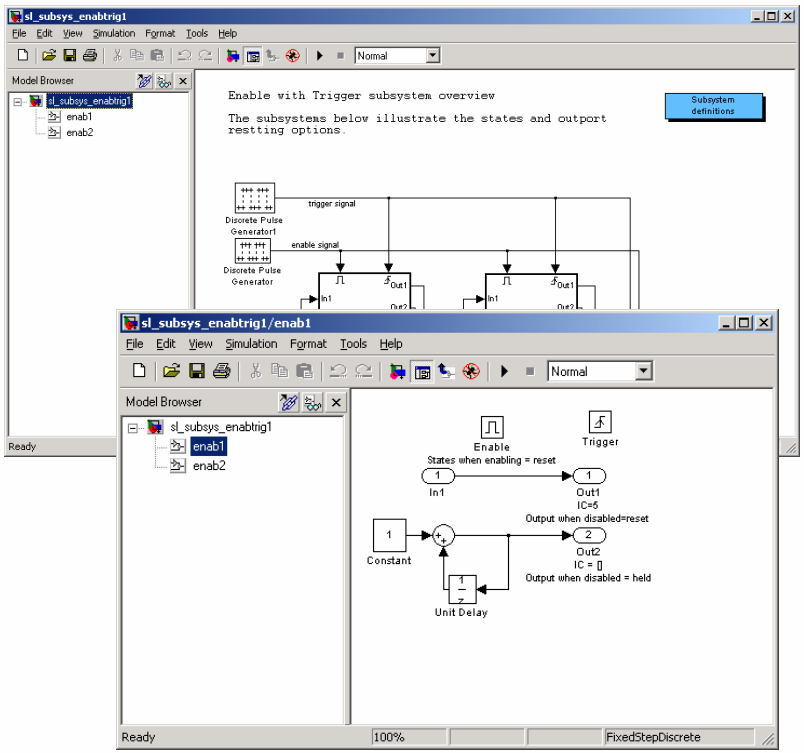
Subsystems and Hierarchy



- Group multiple blocks into subsystem to any level
- Model browser
- Conditionally executed subsystem
  - Enabled and triggered
  - If, while, for, switch
- Configurable subsystem

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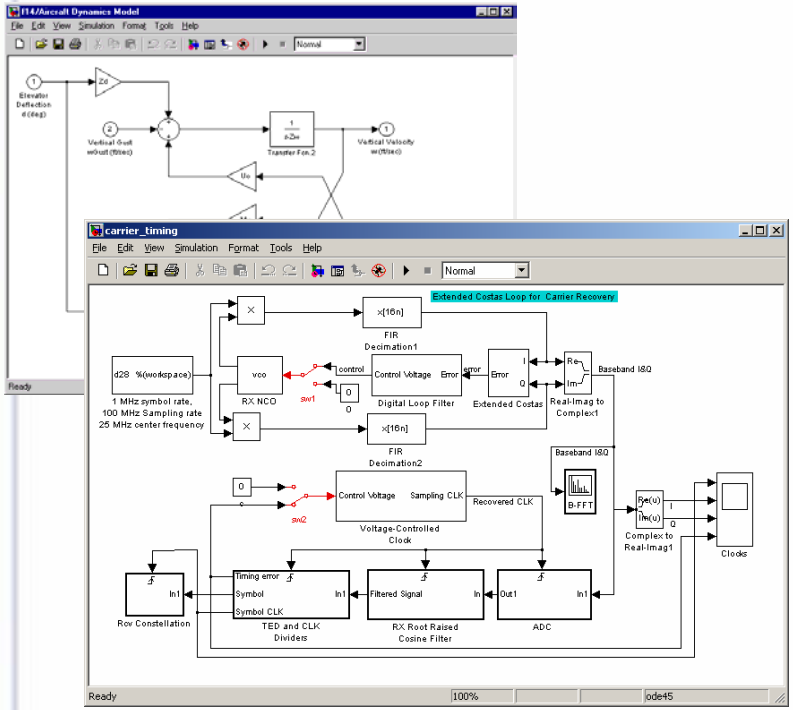
Complex Timing and Concurrency



- Complex timing
  - Feedback
  - Asynchronous edge triggered blocks
  - Multi-rate digital with arbitrary sample rates
- Concurrency
  - True expression of parallelism
  - Important for whole system or hardware subsystem design
  - Not possible with programming language like C

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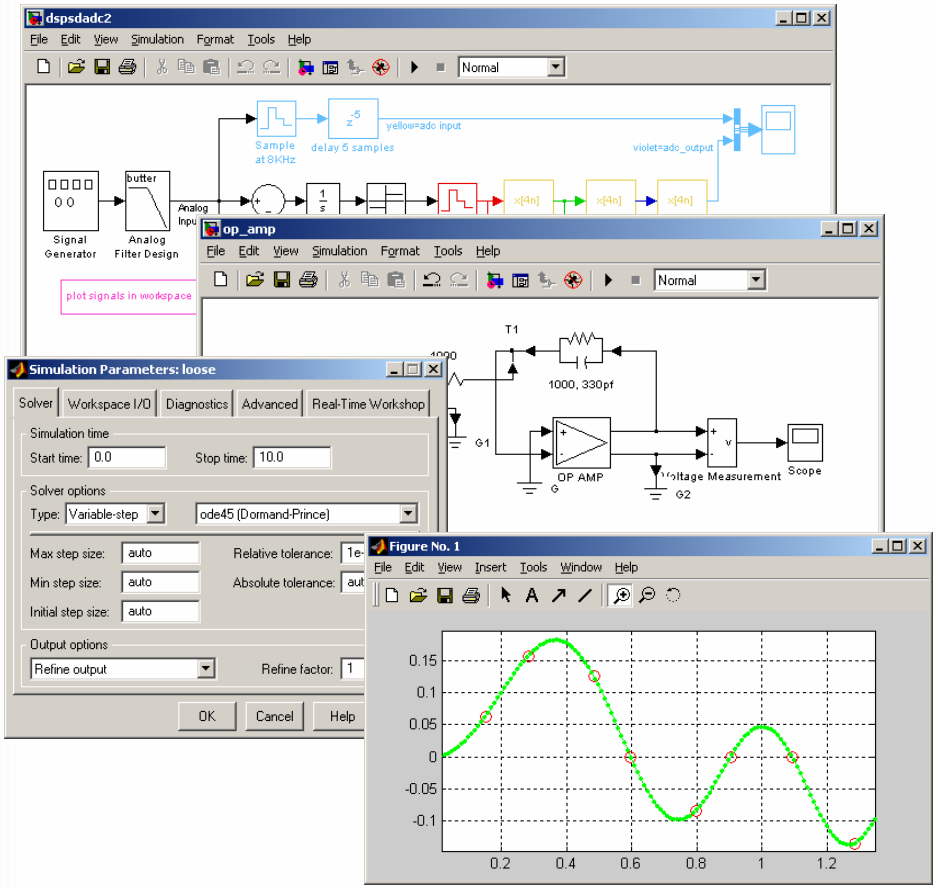
Multirate and Analog



- Digital
  - Fast frame based simulation
  - Schedules complex multirate systems
- Analog
  - Variable step numerical integration solvers
  - Zero-crossing detection

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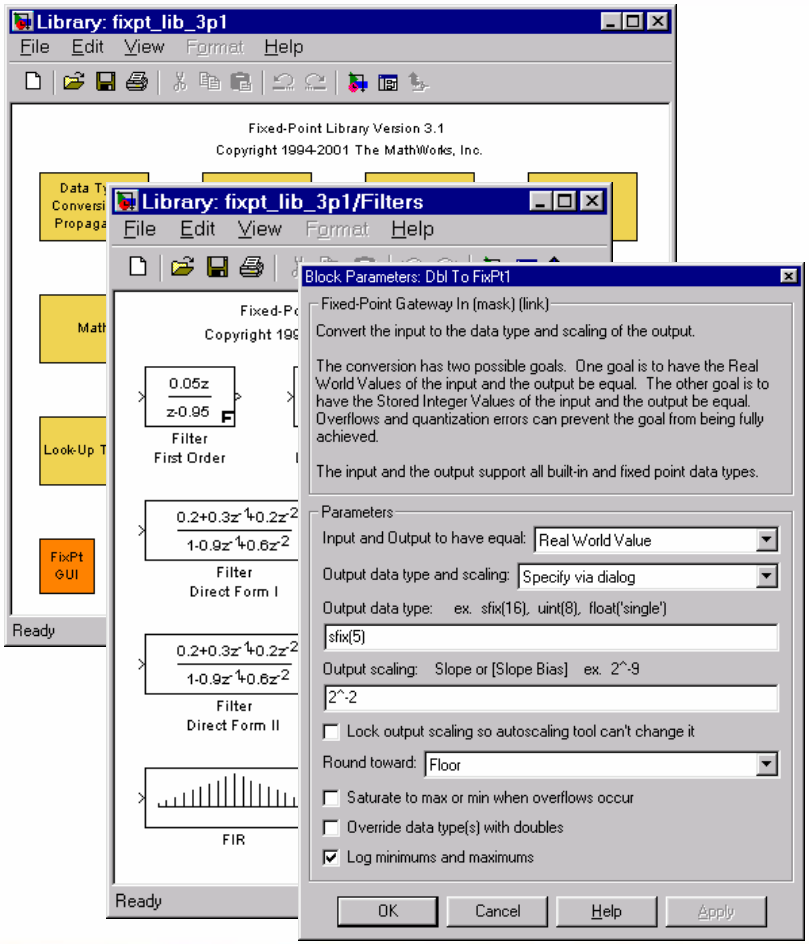
Data Types



- Default double
- C data types in Simulink
- Fixed-Point Blockset
  - Specify word length
  - Integer, fixed, fractional and custom float types
  - Scaling, rounding and overflow
  - Include own bit-true code

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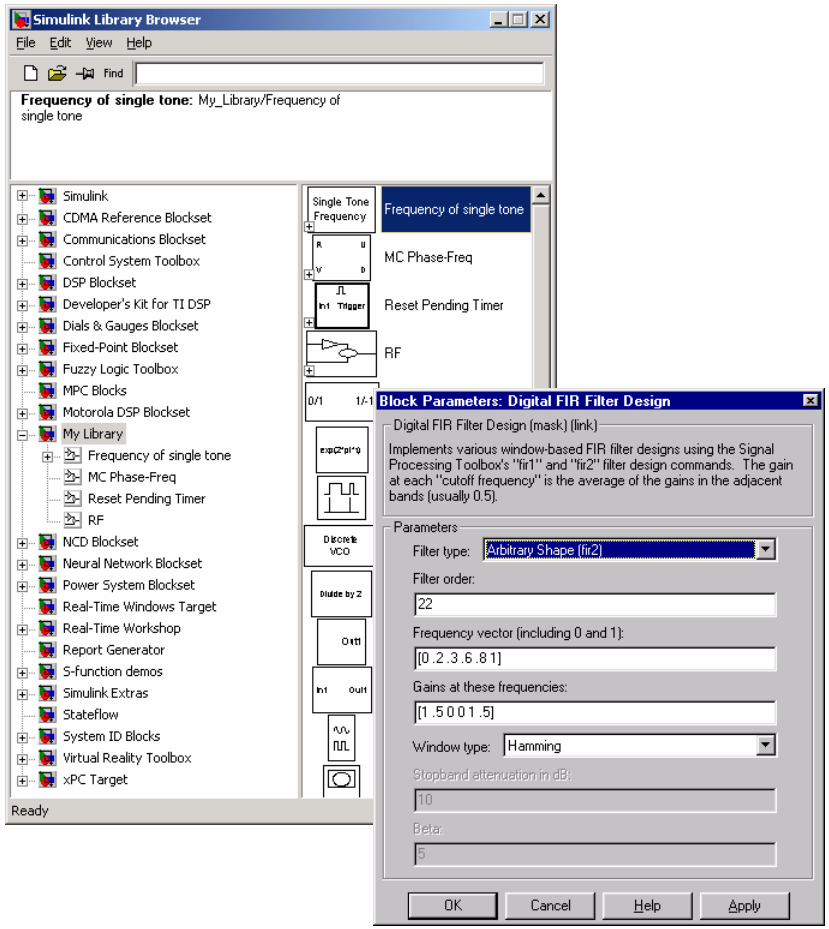
Custom IP Blocks and Libraries



- Created from
  - Other blocks
  - C code
  - MATLAB code
- Custom parameter GUIs
- Custom icons
- Store in custom libraries

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System-Level Simulation Example: Ultra-wideband (UWB) Radio

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Ultra-wideband (UWB) Radio

- Application: WPAN* multimedia
  - High-speed data (~100-500 Mb/s) over short range (~10 m)
  - In-home video distribution, e.g., DVD → HDTV
- Stringent FCC requirements:
  - Frequency allocations/bandwidths
  - Minimize interference with existing services (GPS, 802.11a)
- IEEE 802.15.3a

* WPAN: Wireless Personal Area Network

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Role of MATLAB & Simulink in UWB Definition

- *Common modeling platform*
  - *standards groups, regulators, and design engineers*
  - Assess performance, potential interference and FCC compliance
  - Share models within and between organizations
  - Build *executable* specification as standard emerges
- *Example using MATLAB & Simulink:*
  - 802.15.3a Multiband OFDM PHY model
  - Adapted from existing 802.11a PHY model in ***3 days***

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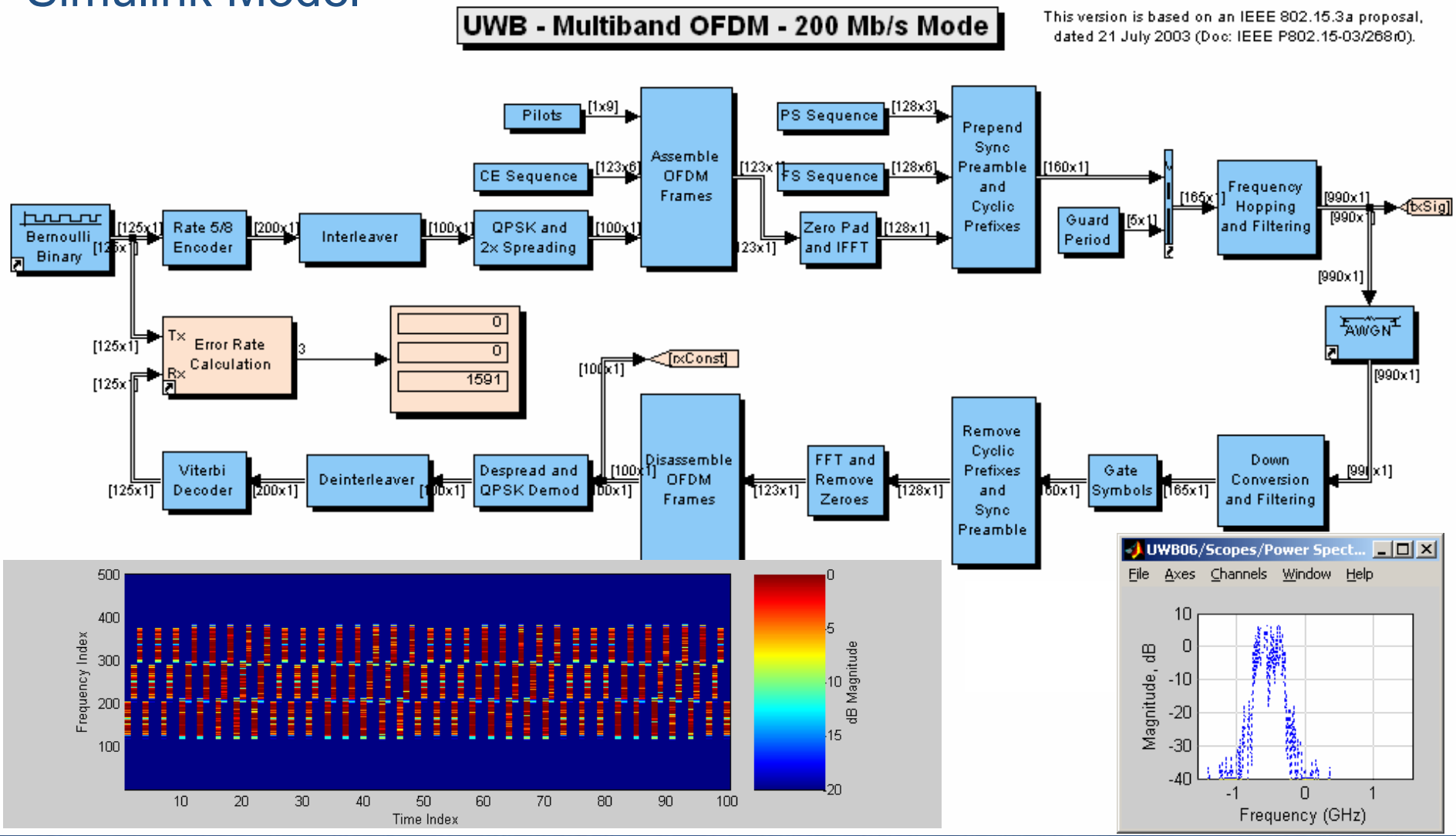
Simulink Model

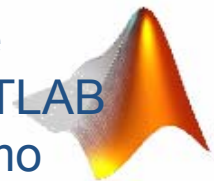


Simulink Model Demonstration

- Current model captures data/signal path of Multiband OFDM PHY as specified in 802.15.3a proposal

- Model easily enhanced to include:
  - RF impairments (Communications Blockset)
  - Multipath channel and equalization (see 802.11a example)
  - Interference modeling within piconets and with other wireless devices (see Bluetooth models for examples)
  - Fixed-point modeling (DSP Blockset; see 802.11a example)

Live MATLAB Demo



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DSP Component Design: Digital Down Converter

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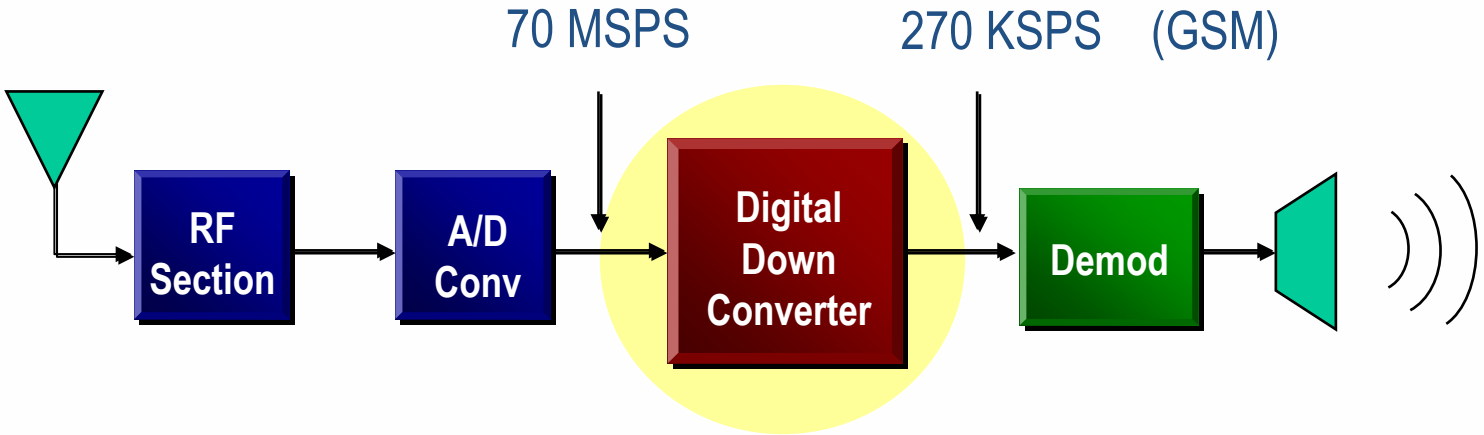
Simplified Digital Radio



Digital Down-Converter (DDC)

- Performs **digital mixing** using low-pass filters and decimation
- Example: TI/GrayChip **GC4016** DDC

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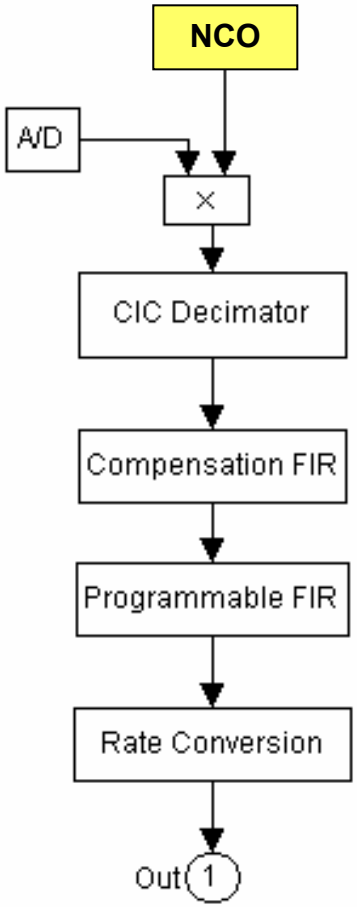
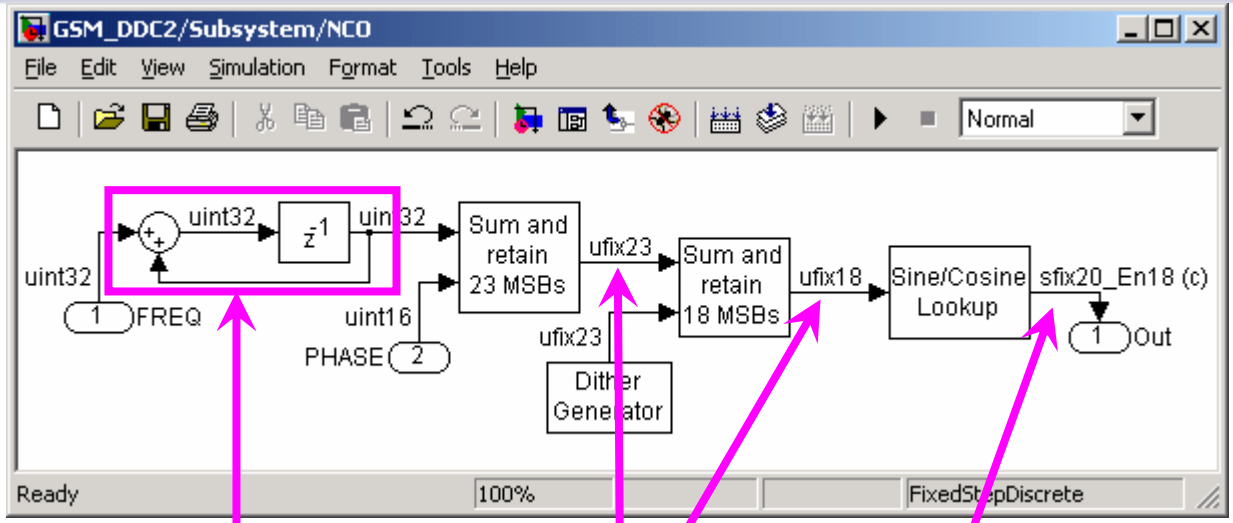
NCO: **N**umerically **C**ontrolled **O**scillator





- 32-bit accumulator
- 23- and 18-bit integers
- Signed 20-bit fixed point
  - 18 bits after binary point
  - complex data “(c)”

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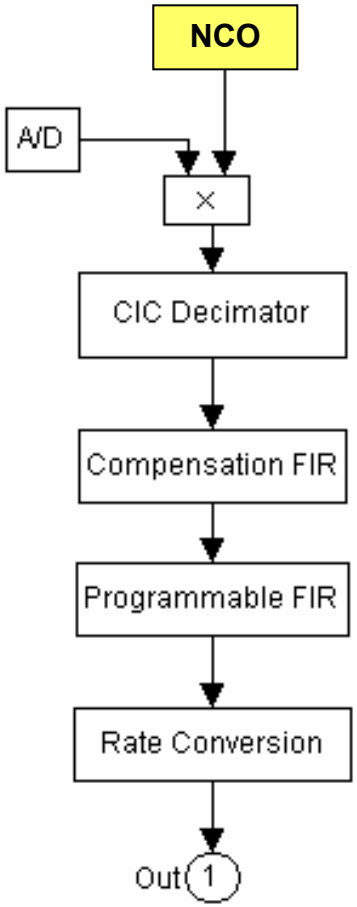
NCO Analysis



Digital Down Converter

- Use MATLAB and Simulink to:
  - Analyze spectrum of fixed-point NCO
  - Evaluate spectrum with dither applied
  - Compute SFDR (Spurious-Free Dynamic Range)

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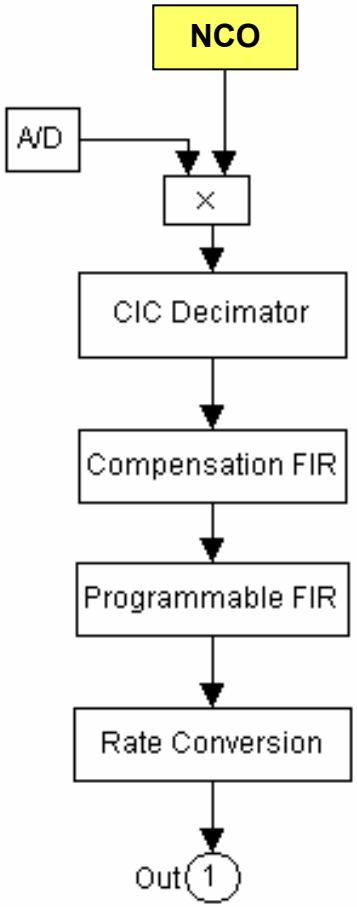
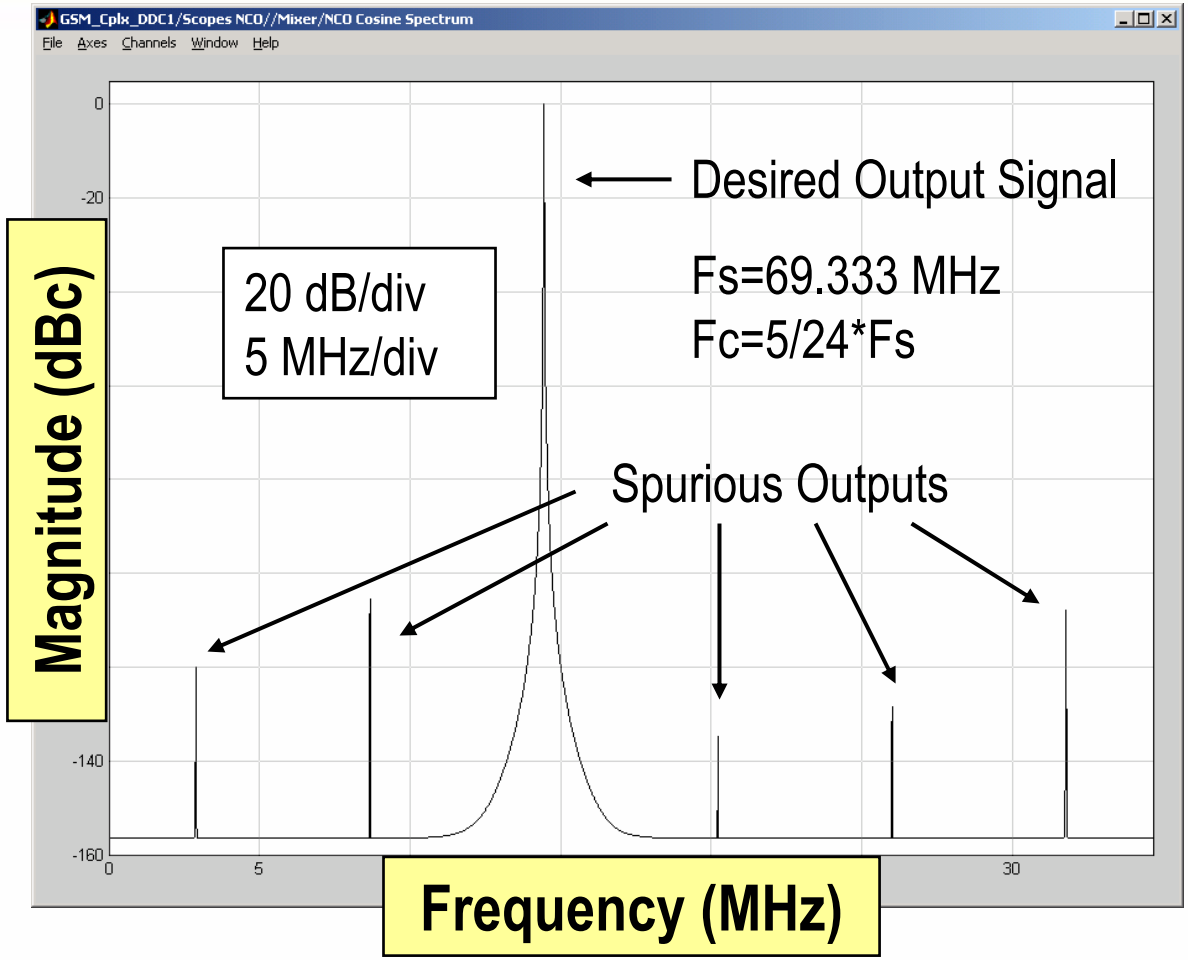
NCO Analysis





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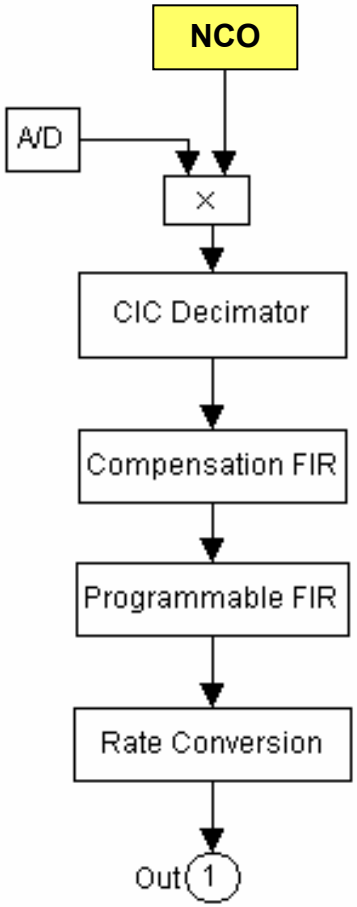
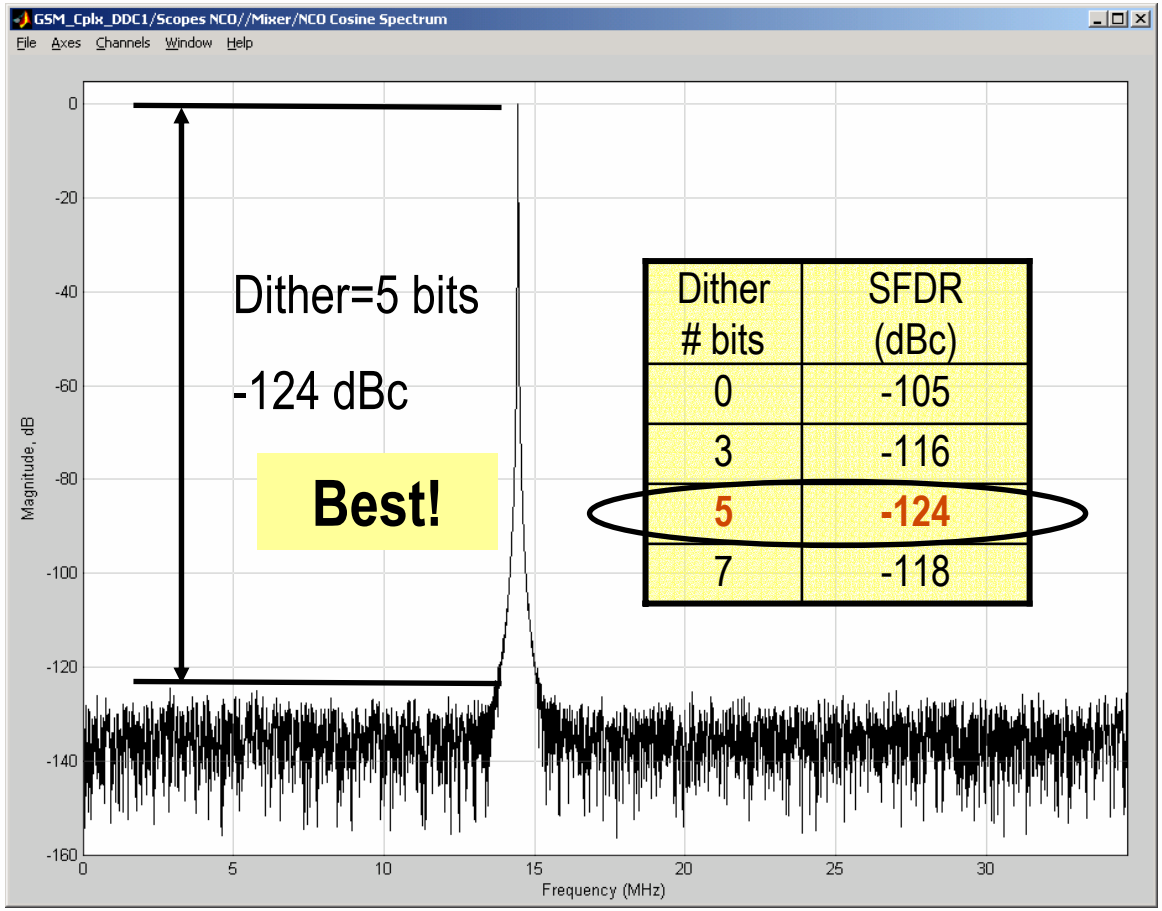
NCO Analysis





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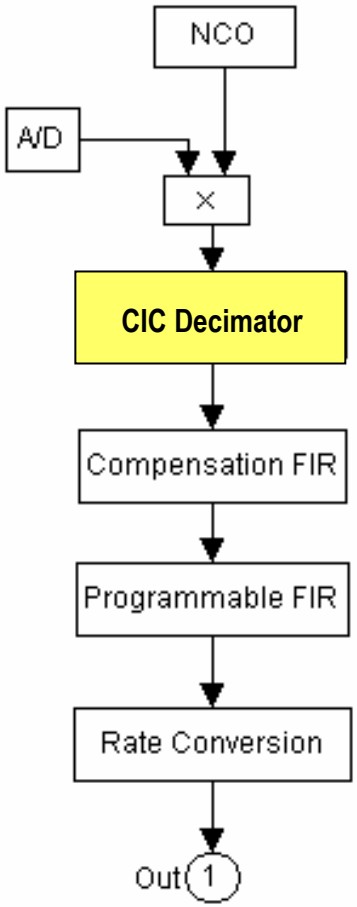
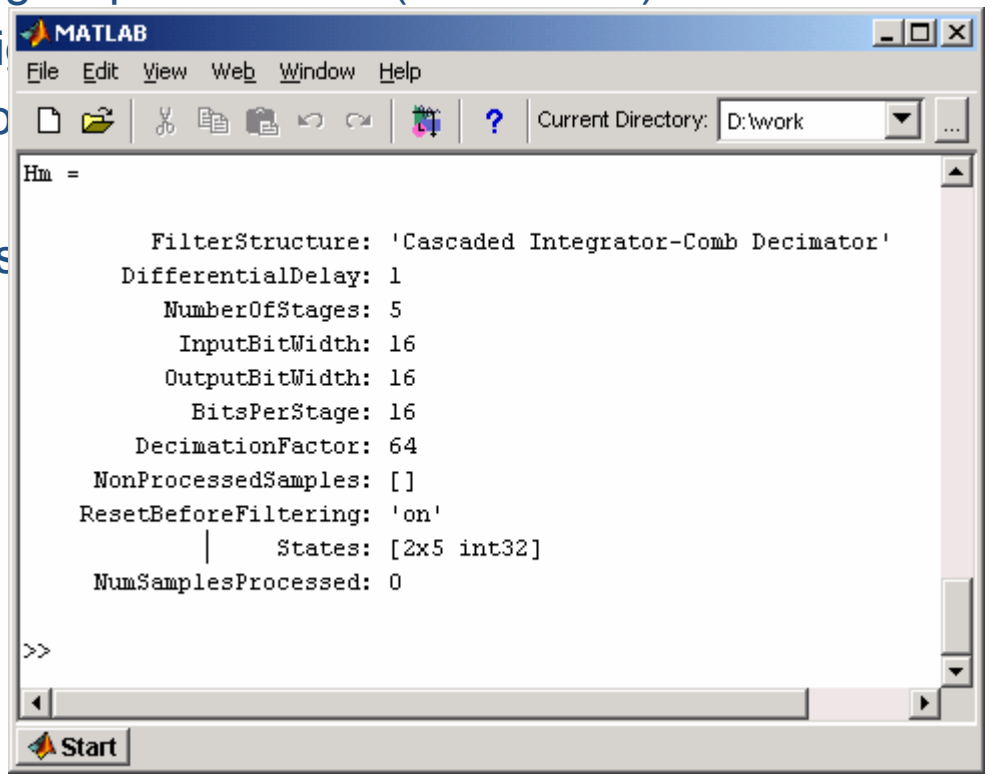
CIC Filter Design



Cascaded Integrator Comb filter

- High input data rate (69.33 MHz)
- Hi
- Lo
- Us



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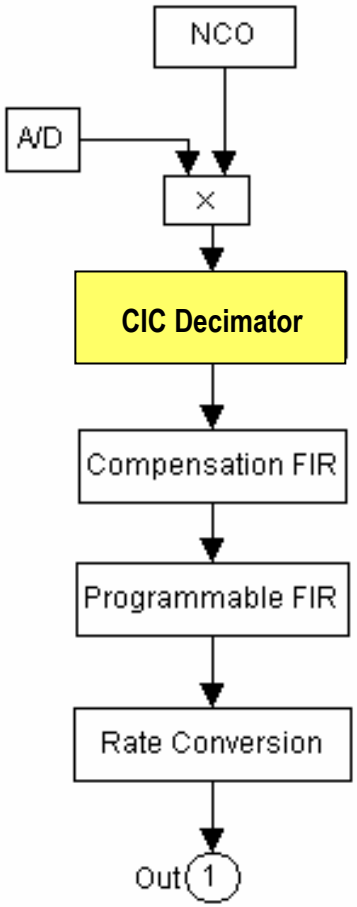
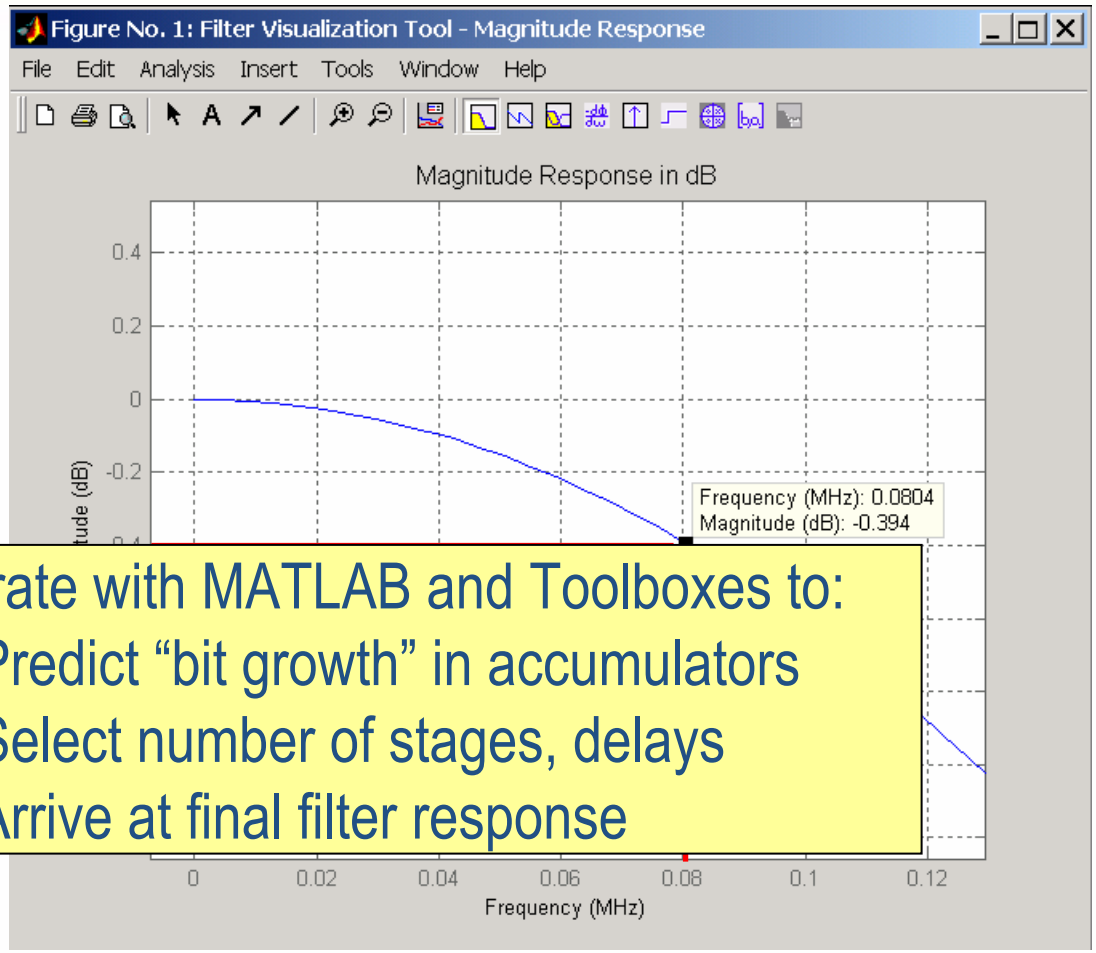
CIC Filter Analysis





Iterate with MATLAB and Toolboxes to:
- Predict "bit growth" in accumulators
- Select number of stages, delays
- Arrive at final filter response

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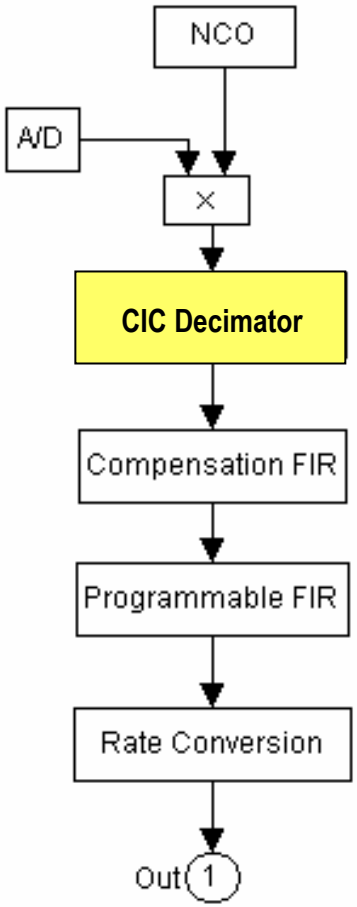
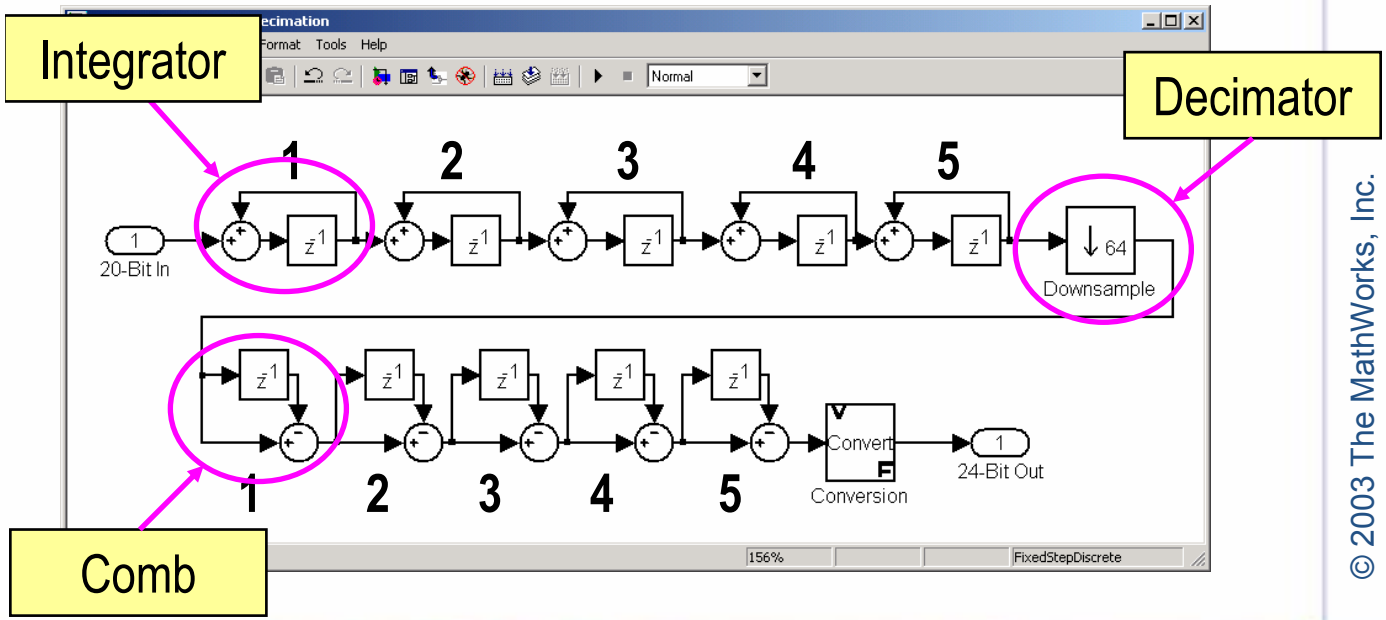
CIC Filter Design



Cascaded Integrator Comb filter

- Automated fixed-point implementation using DSP and Fixed-Point Blocksets



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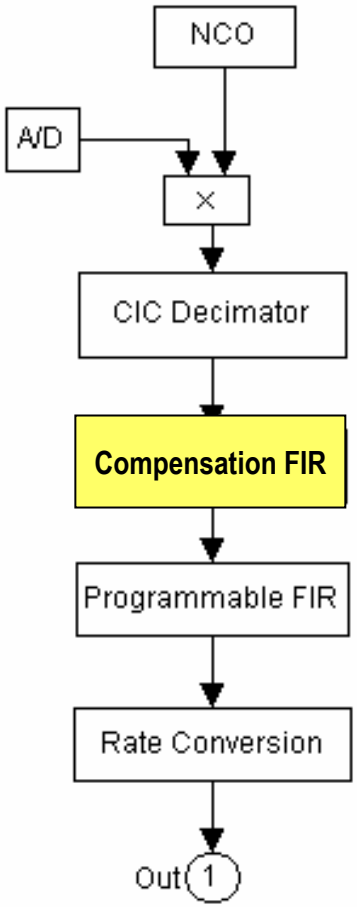
Compensation Filter Design



Design objectives:

- Compensate CIC passband roll-off
- Provide anti-aliasing for decimation
- Fixed-point operation

Typical GSM design parameters:

- 21-tap, 16-bit symmetric FIR
- Input rate 1.083 MHz (69.33 MHz / 64)
- Output rate 541.66 kHz (1.083 MHz / 2)

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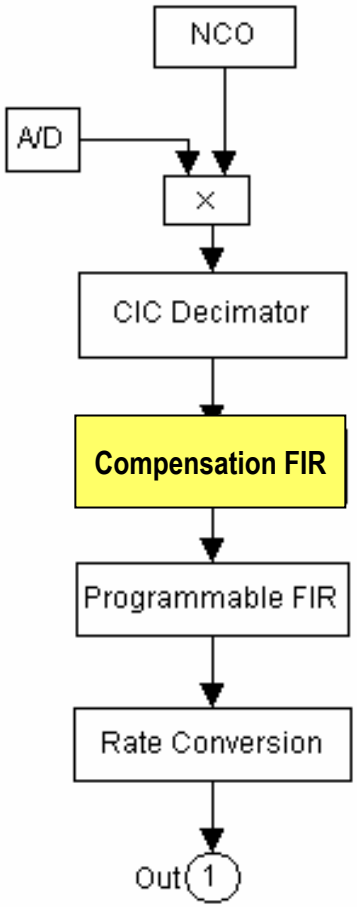
Compensation Filter Design



Fixed point filter response

Constrained Equiripple FIR
- FIRCEQRIP
- 16-bit fixed point

Filter specifications:
- Stopband slope (60 dB)
- 5th order Inverse sinc
- Passband, stopband ripple

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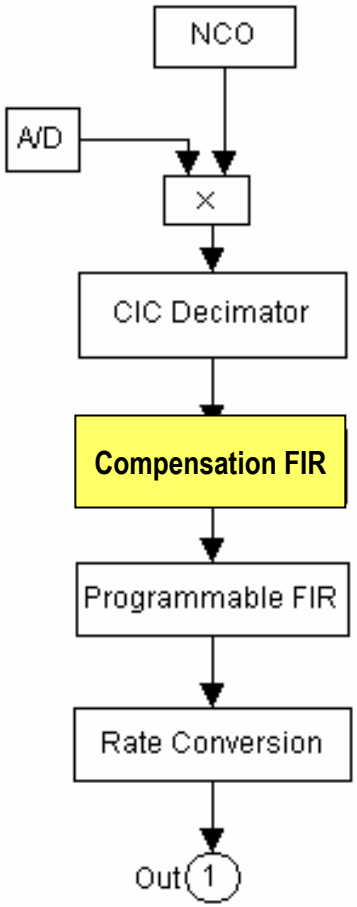
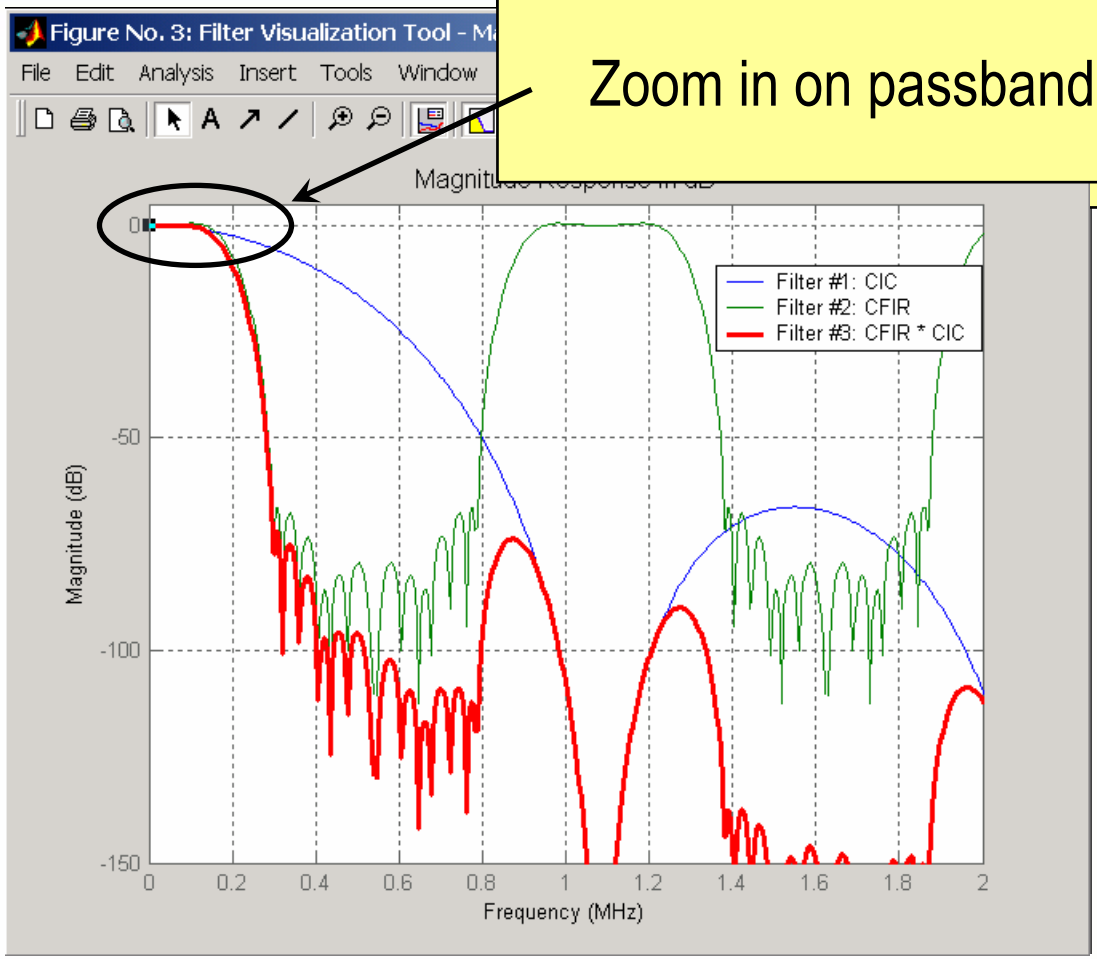
Compensation Filter Analysis





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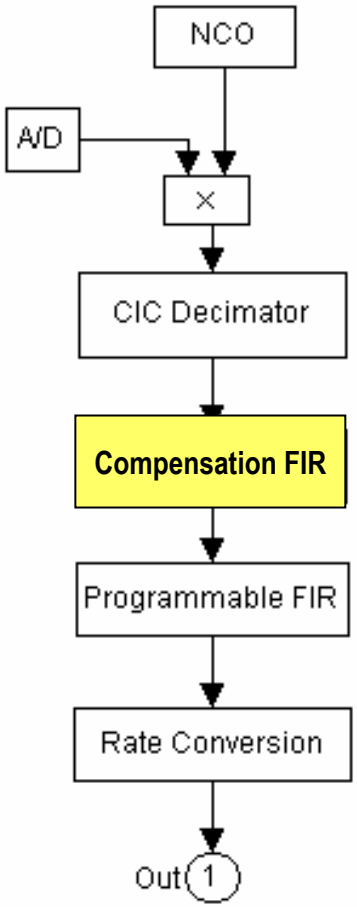
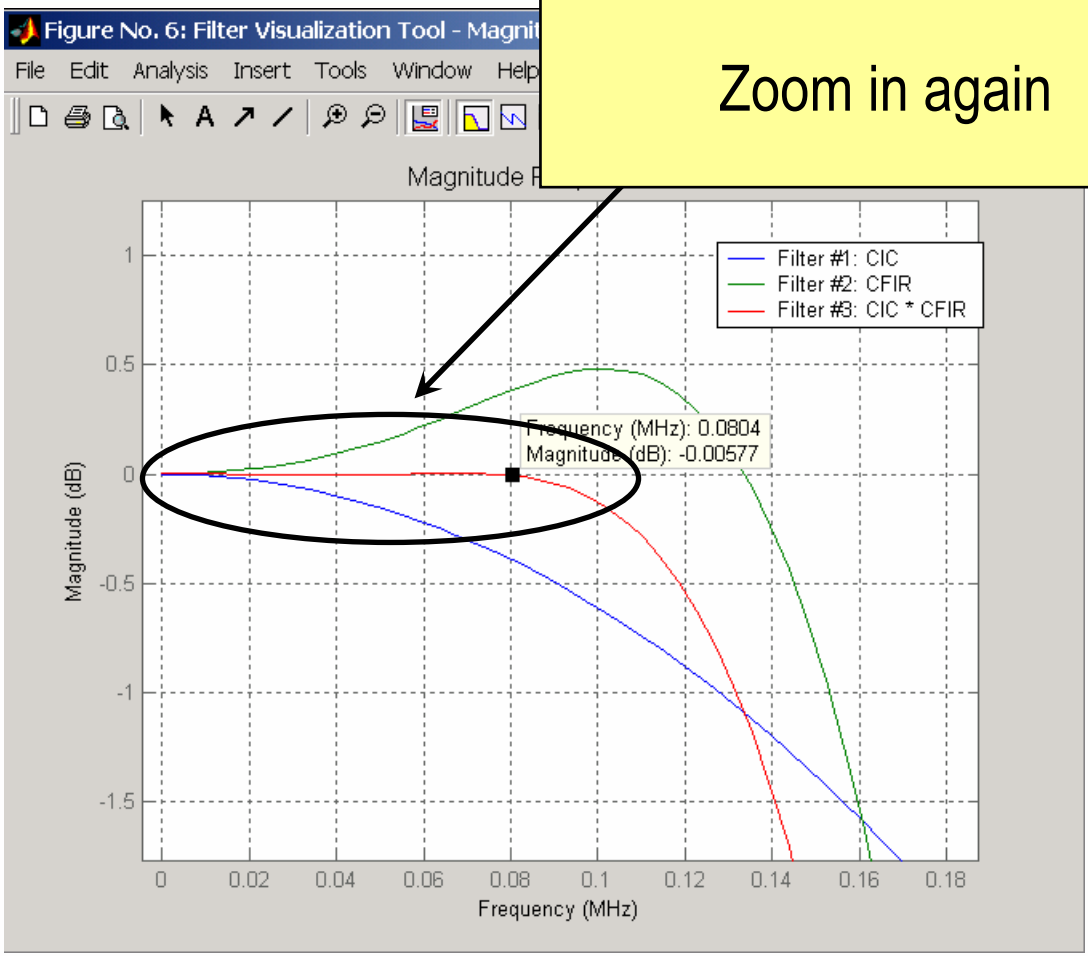
Compensation Filter Analysis





Zoom in again

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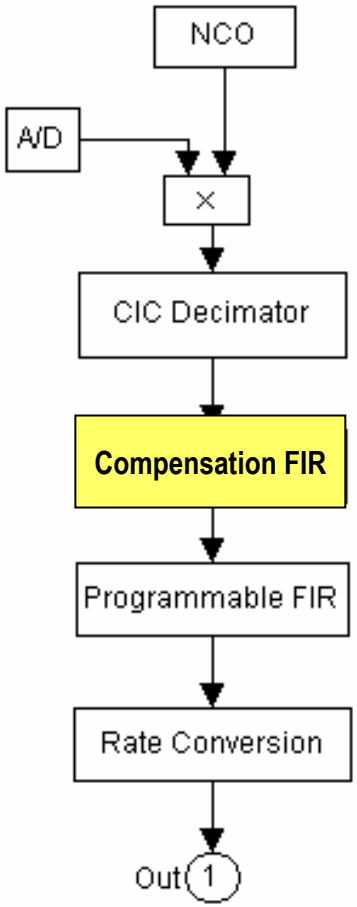
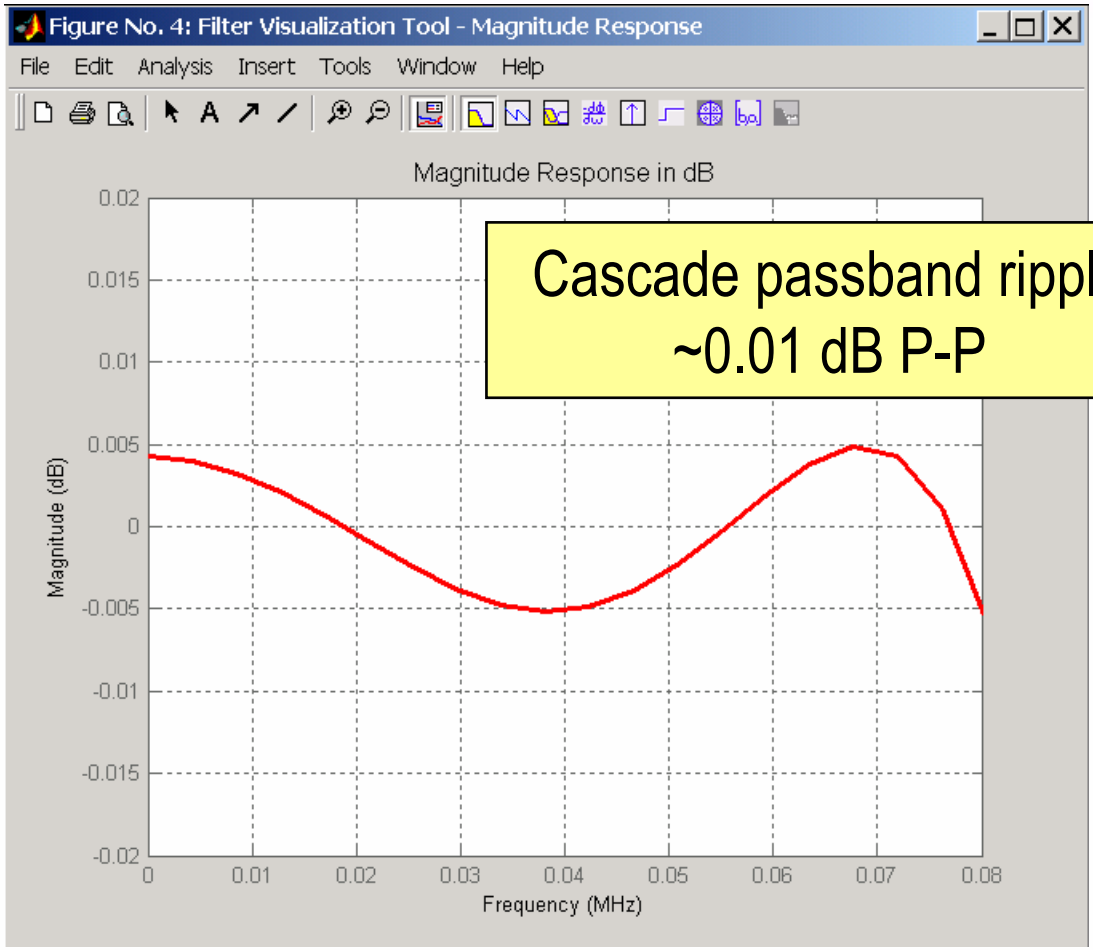
Compensation Filter Analysis





Cascade passband ripple
~0.01 dB P-P

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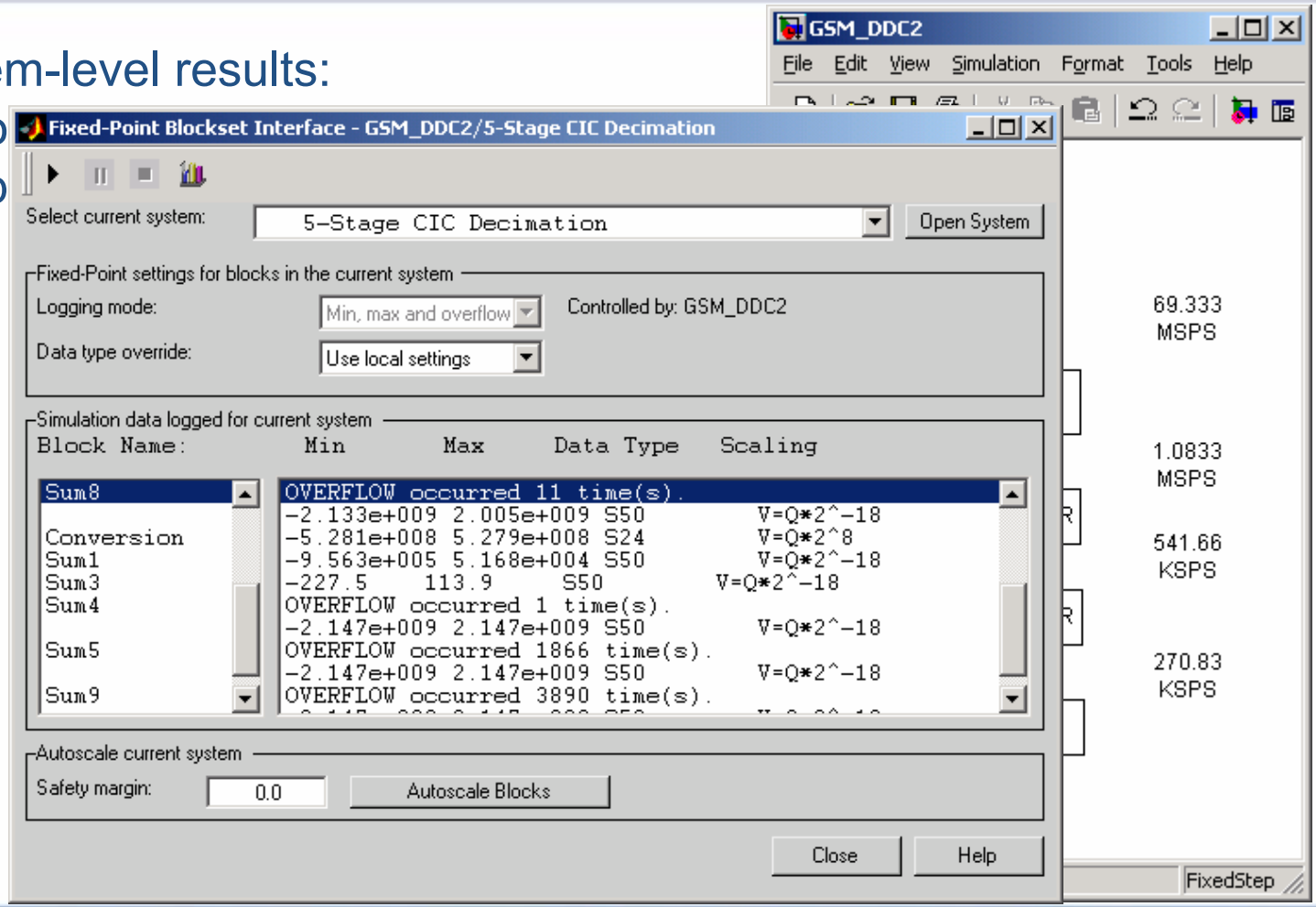
System-Level Analysis

Key system-level results:

- monito
- fixed-p



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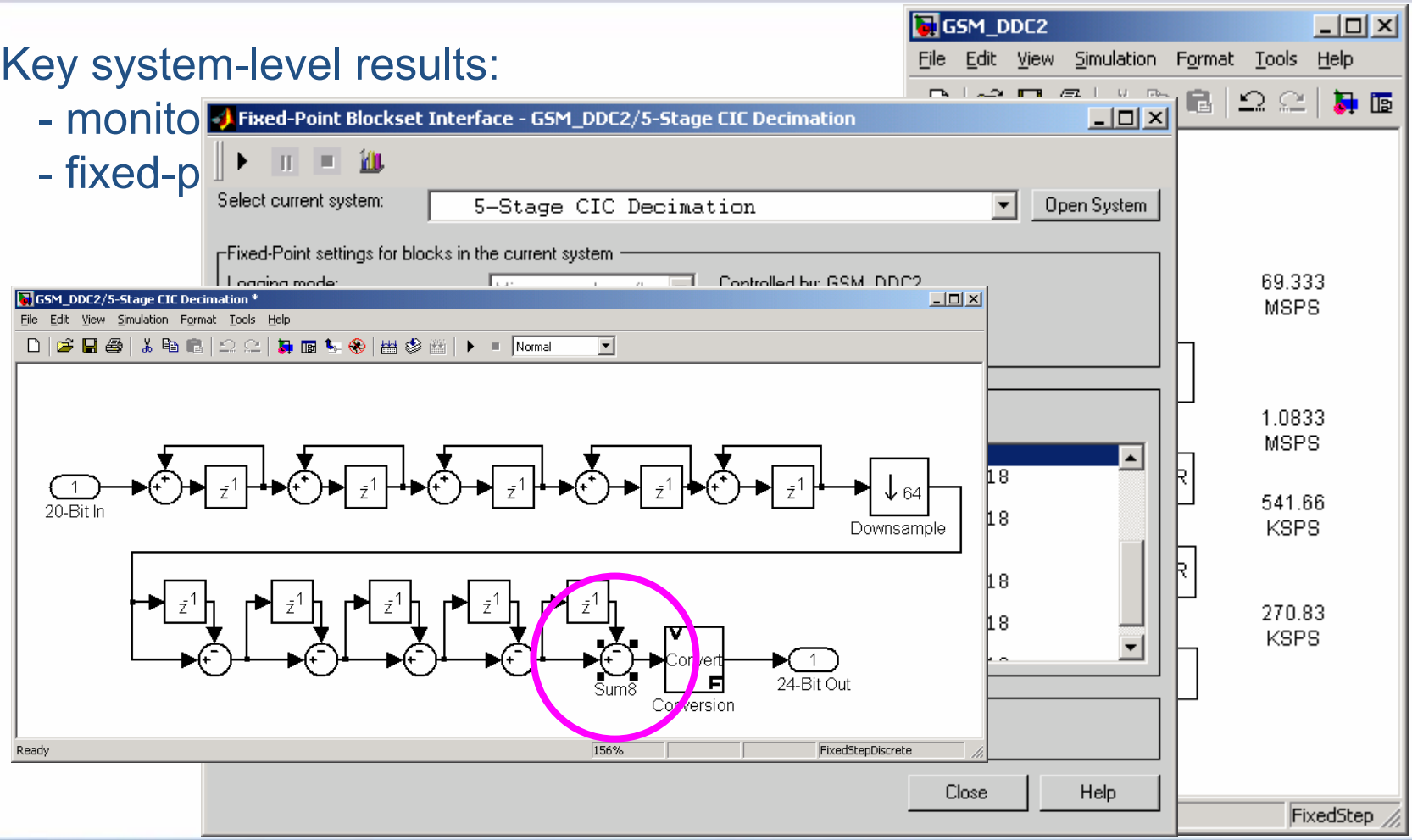
System-Level Analysis

Key system-level results:

- monito
- fixed-p



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DDC Demo Summary

- MathWorks tools working together to create an integrated design environment
  - MATLAB, Simulink
  - Signal Processing Toolbox, Filter Design Toolbox
  - Fixed Point Blockset, DSP Blockset
- Value to you
  - Implement new designs faster
  - Verify behavior of existing silicon (GC4016) under real-world conditions

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System-Level Verification of HDL Designs using Link for ModelSim

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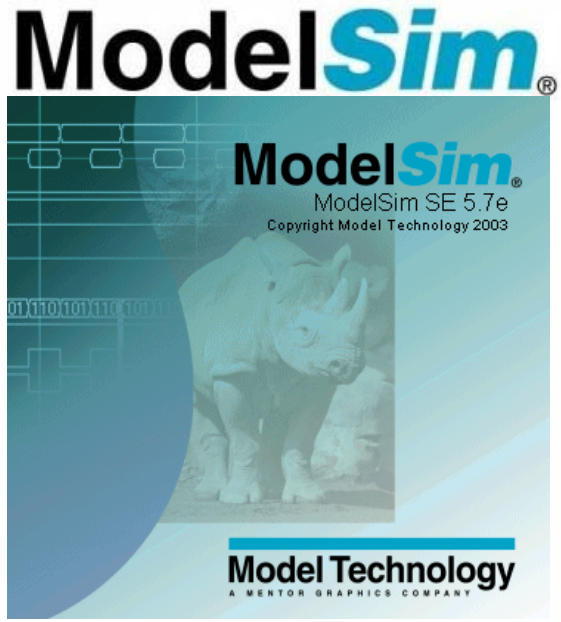
Link for ModelSim®

- Connects MATLAB and Simulink to ModelTechnology's ModelSim® HDL Simulator
- MATLAB Validation of HDL designs
  - Data visualization
  - Test benches and test signals
  - Substitute M for HDL
- Simulink Integration with HDL designs
  - Co-simulation of HDL
  - System-level views of HDL code
  - HDL data file I/O



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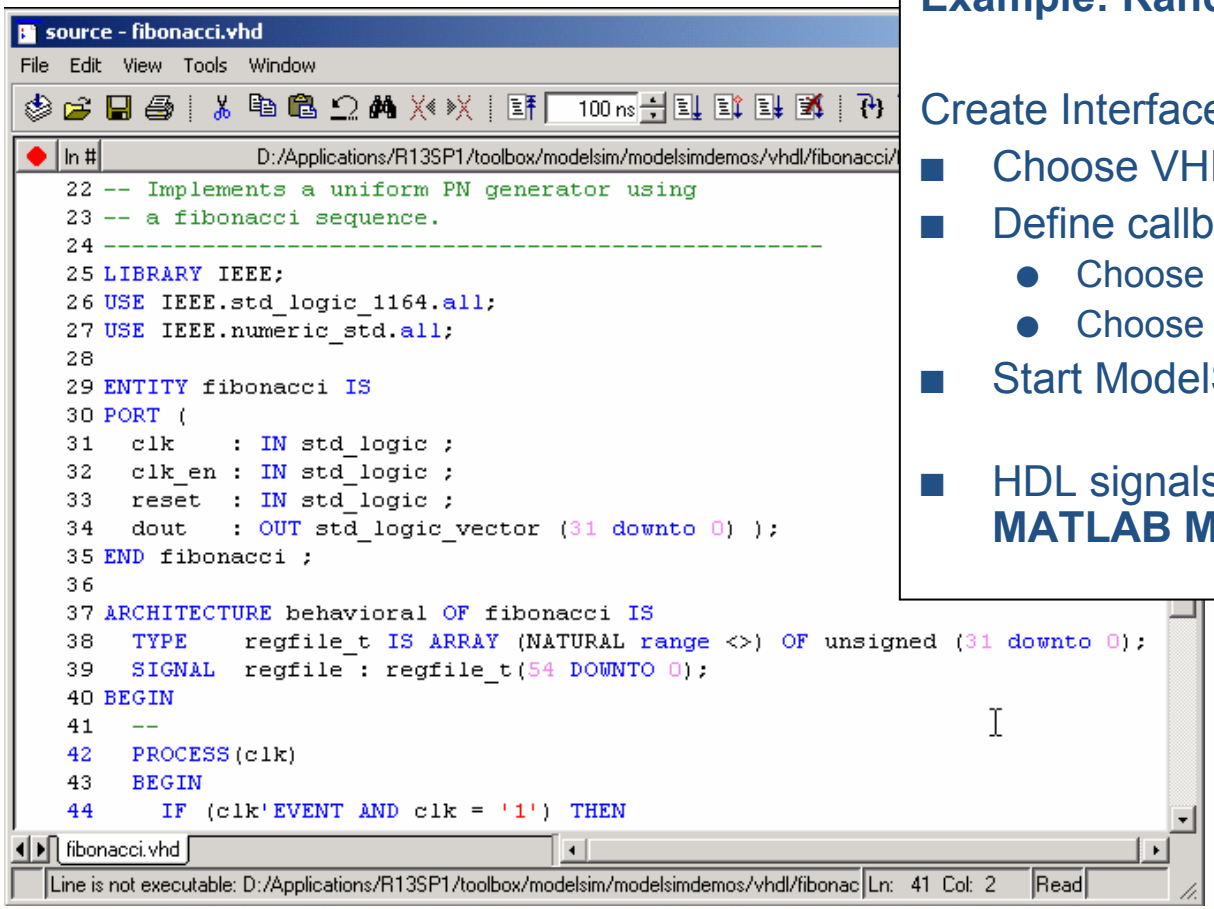
MATLAB: Data Visualization



Example: Random Number Generator

Create Interface to MATLAB:

- Choose VHDL entity
- Define callback in MATLAB
  - Choose M-file
  - Choose timing model
- Start ModelSim simulation
- HDL signals can pass **to and from MATLAB M-file**

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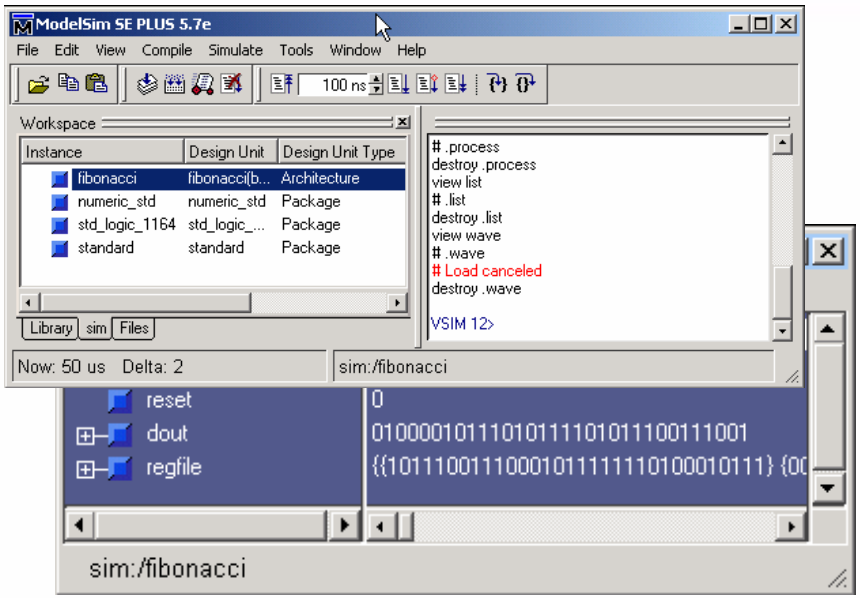
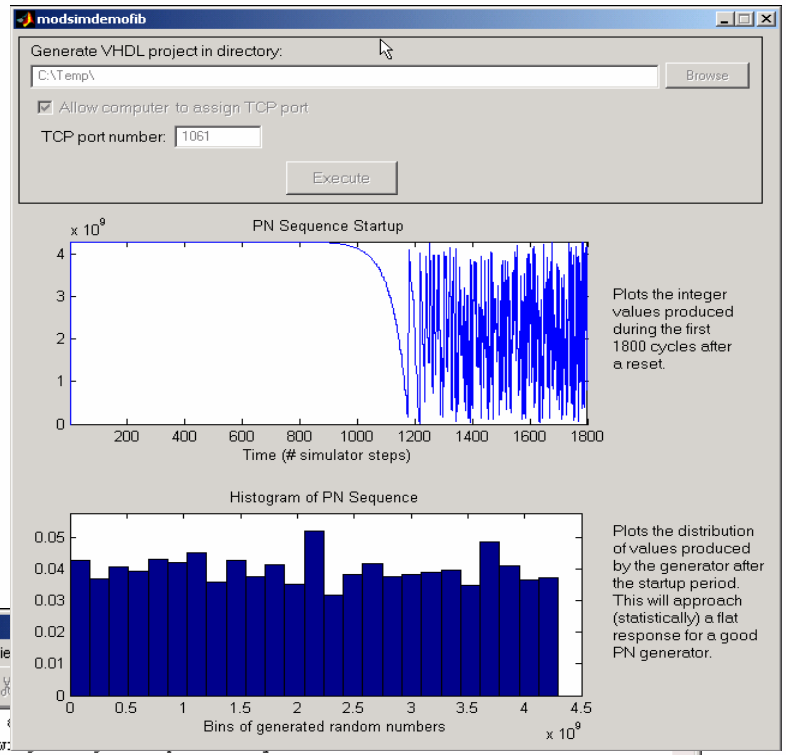
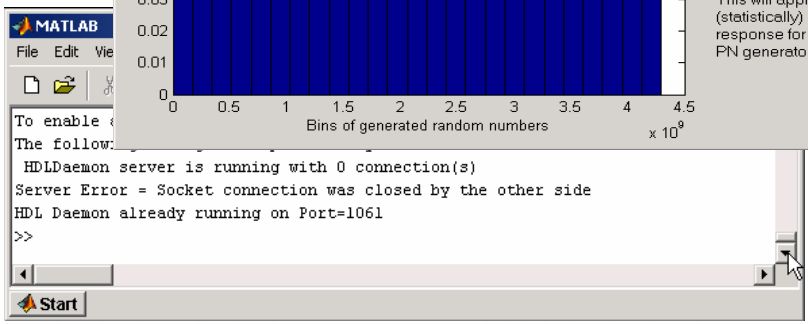
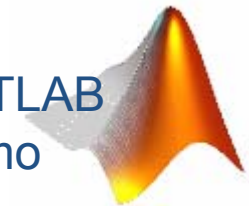
MATLAB: Data Visualization







Live MATLAB Demo



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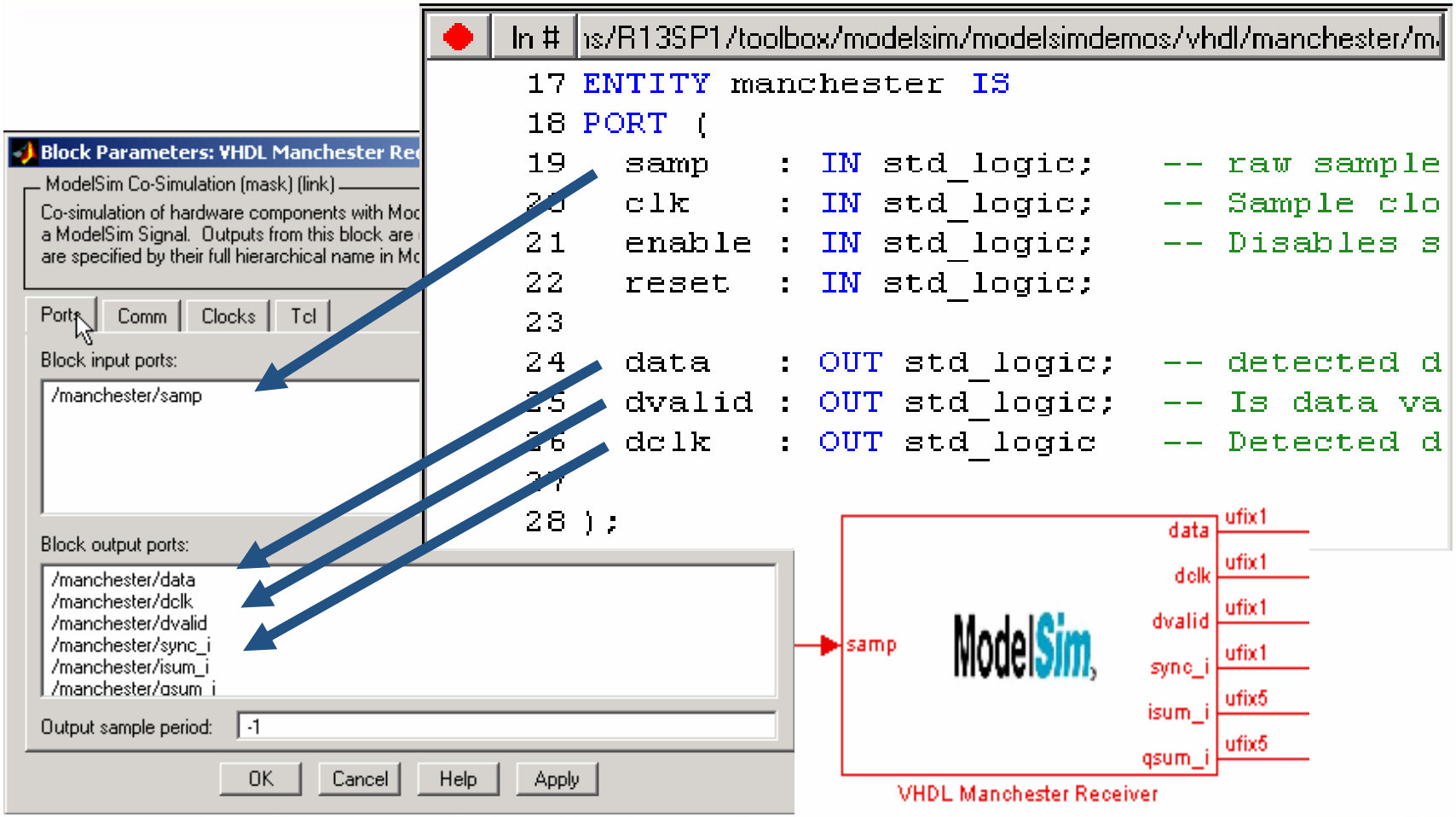
Simulink Co-Simulation



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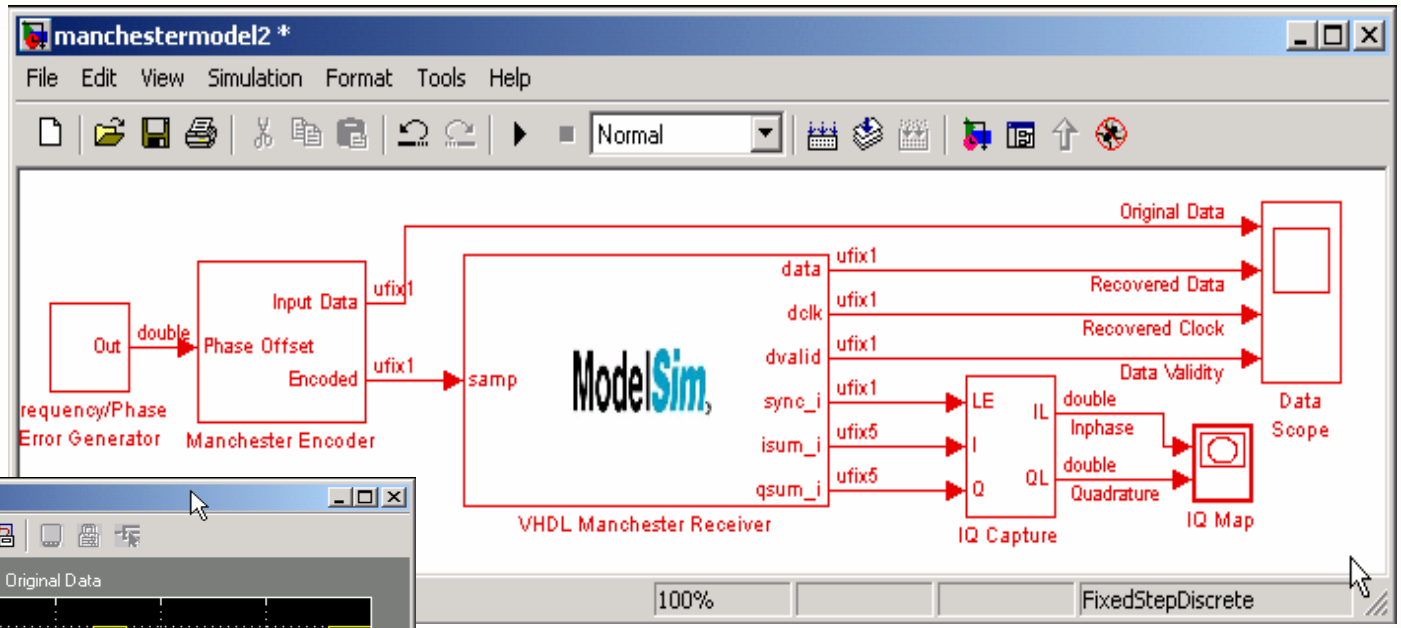
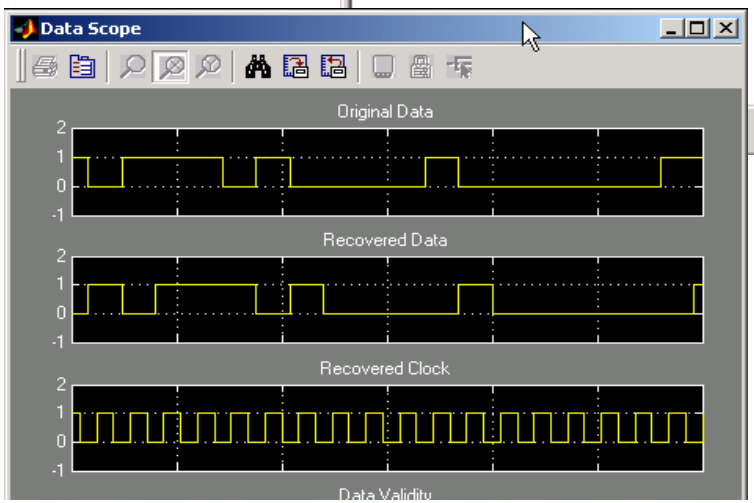
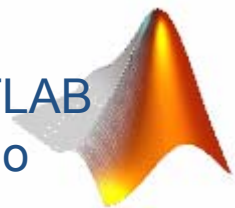
Simulink Co-Simulation: Single Entity





Example: Manchester Receiver

Live MATLAB Demo



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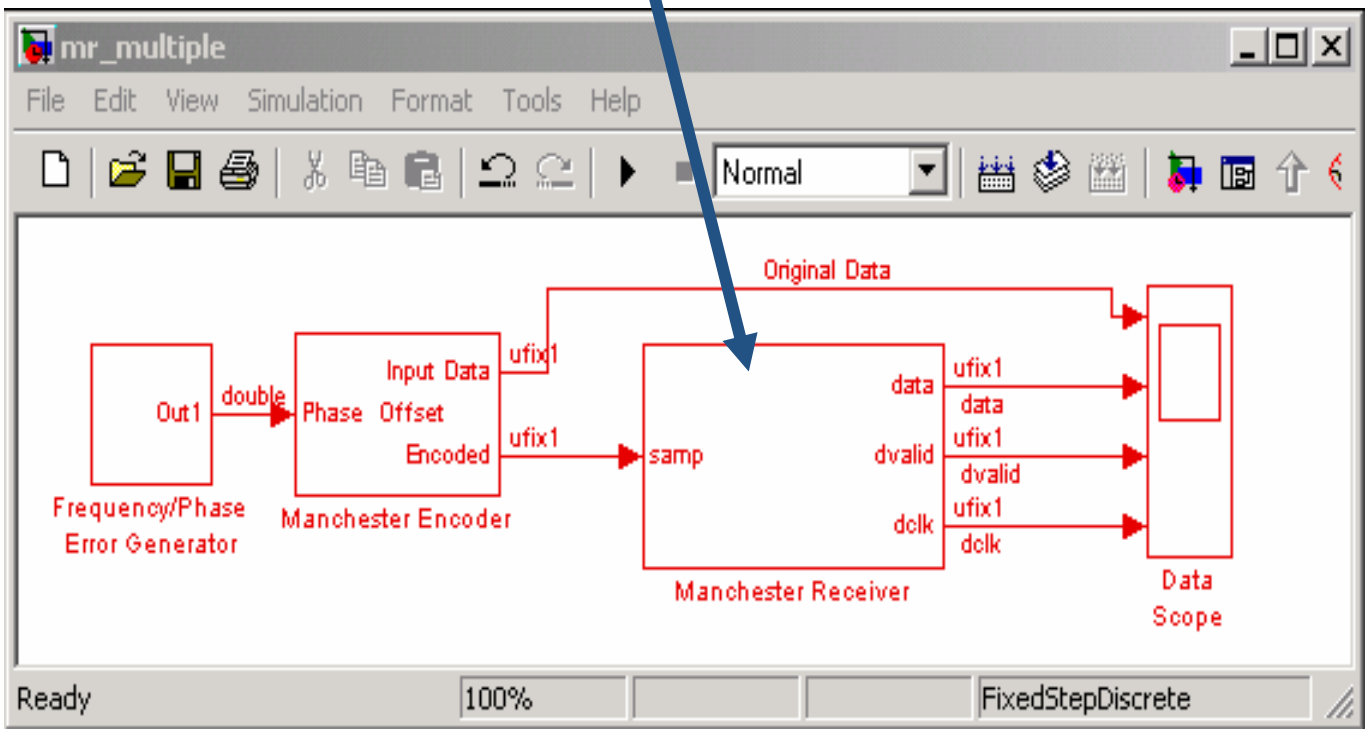
Simulink Co-Simulation: Multiple Entities

SUBSYSTEM: Creates hierarchy in the Simulink model



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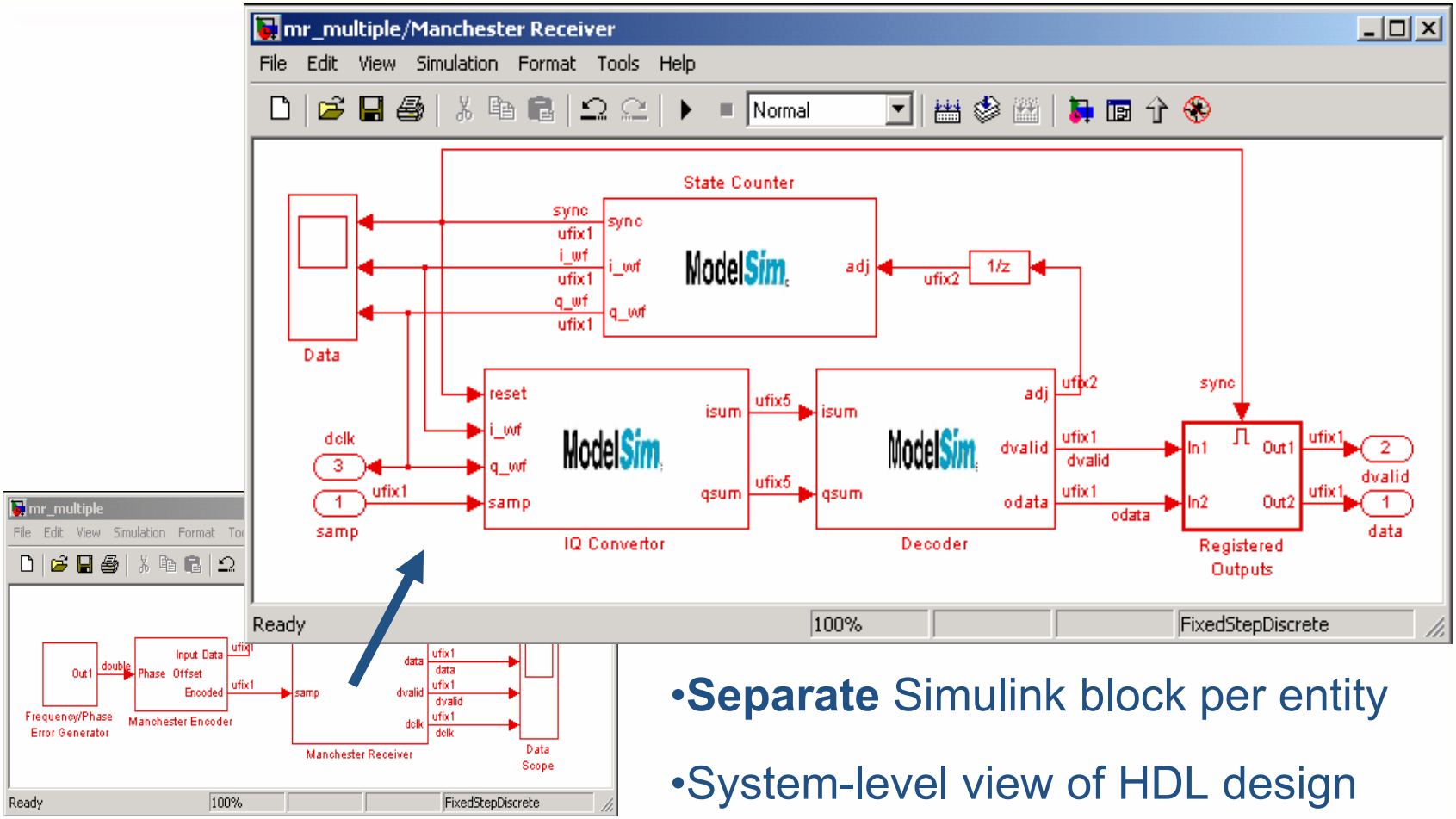
Simulink Co-Simulation: Multiple Entities



- **Separate** Simulink block per entity
- System-level view of HDL design

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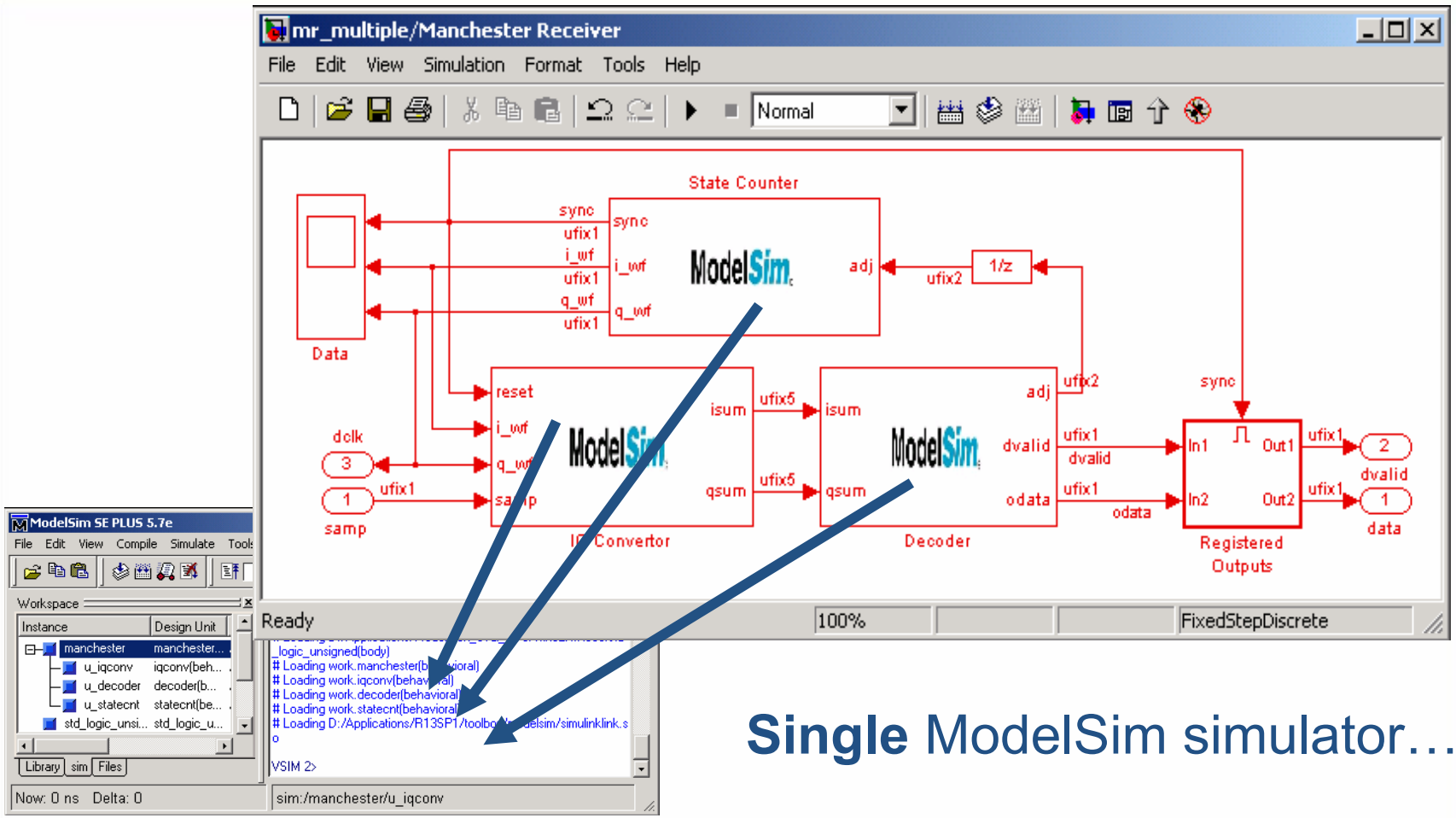
Simulink Co-Simulation: Multiple Entities



Single ModelSim simulator…

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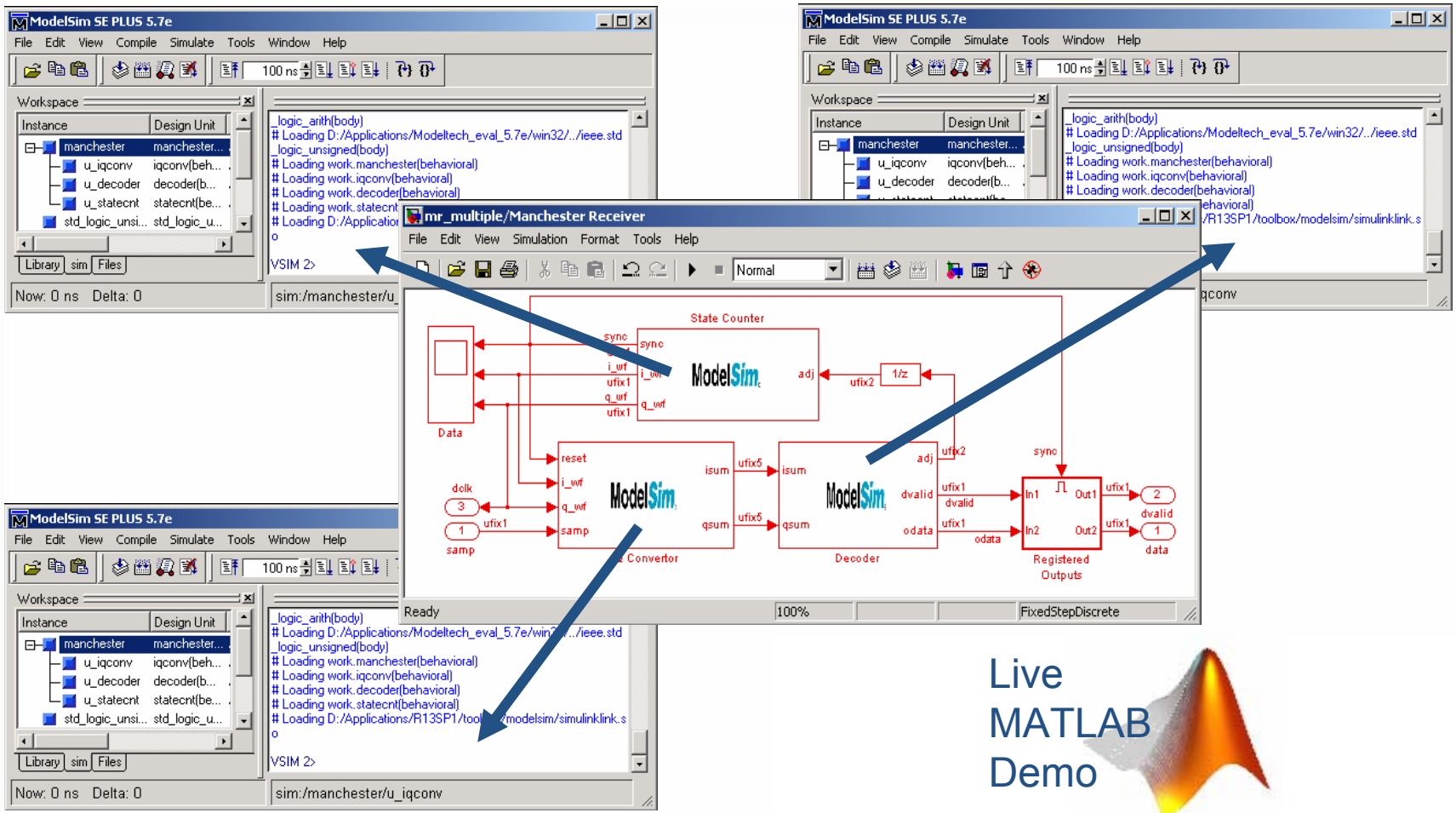
Simulink Co-Simulation: Multiple Simulators



Live MATLAB Demo

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Link for ModelSim®

Availability

- Version 1 - November 2003
  (Web download: www.mathworks.com)

Requirements

- MATLAB: R13SP1
- Simulink: Fixed Point Blockset
- ModelSim: v5.7a, 5.7c, 5.7e
  (latest 3 versions at time of release)
- Windows and Solaris
- Native VHDL support, Verilog via VHDL Wrappers

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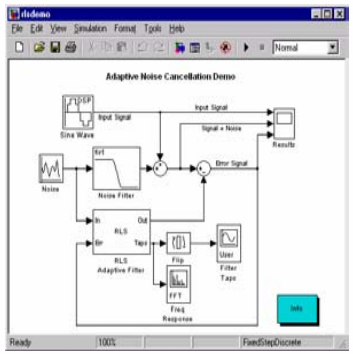
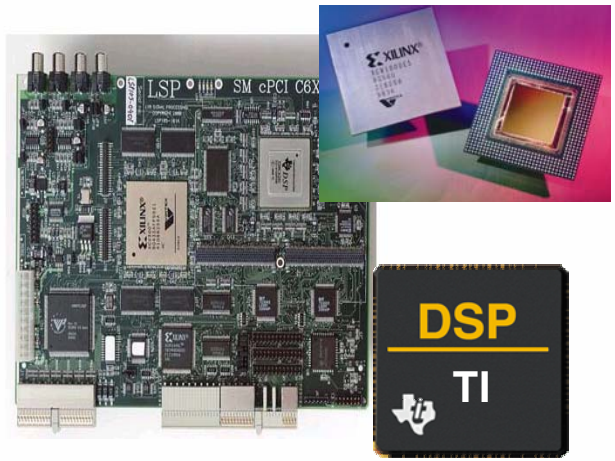
Code Generation for Programmable Hardware





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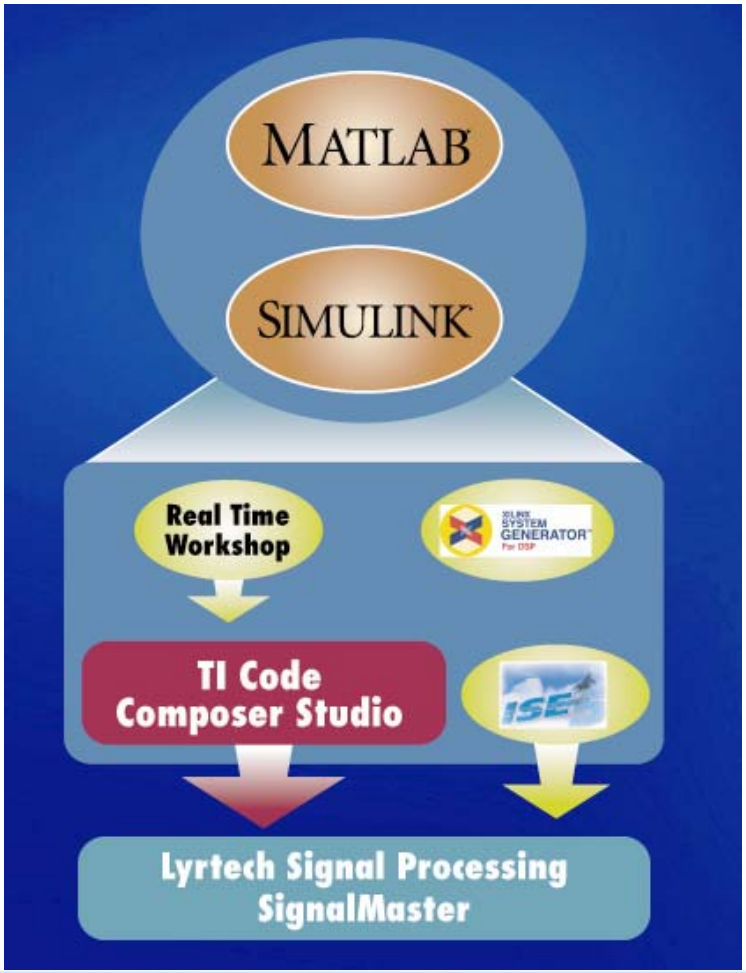
Hardware Implementation Flow



- MathWorks: MATLAB, Simulink & Real Time Workshop
  - Modeling & simulation
  - C code generation for TI DSPs
- Xilinx: System Generator & ISE
  - Optimized HDL for Virtex & Spartan FPGA families
  - Synthesis, place, & route
- Texas Instruments: Code Composer Studio
  - Development environment for TI DSPs
- Lyrtech Signal Processing:
  - Development board

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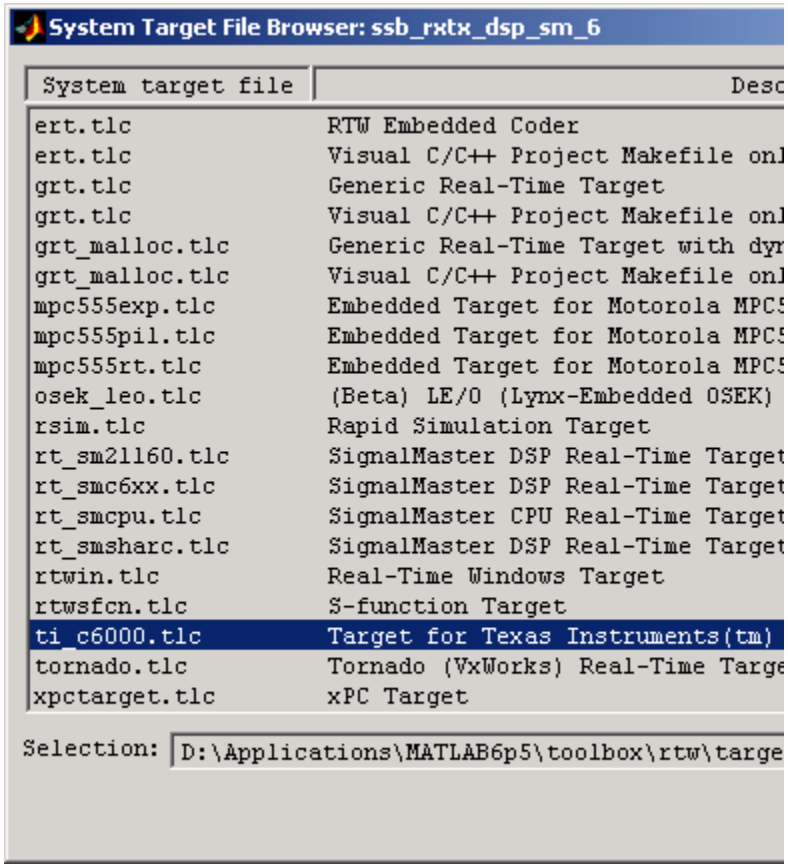
Real-Time Workshop

- Code Generation Engine fully-integrated with Simulation Engine
- Supports Target Language Compiler architecture
- Single-click re-targeting



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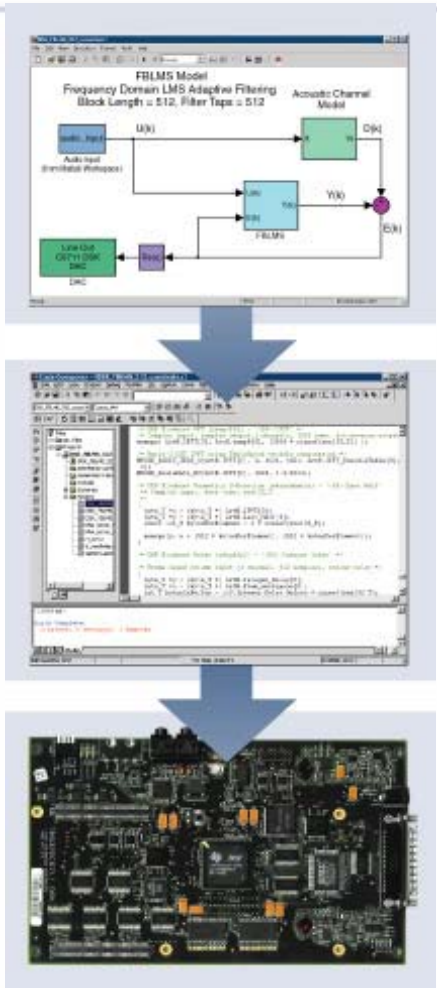
Code Generation for DSP

- Design and simulate with Simulink and blocksets
- Automatically generate high-quality C code
- Automatically compile and link in Code Composer Studio (TI Processors)
- Evaluate in real-time while code executes on DSP target
- Profile code for performance
- Visualize and analyze in MATLAB or Simulink
- Simulink Model can become debugging GUI



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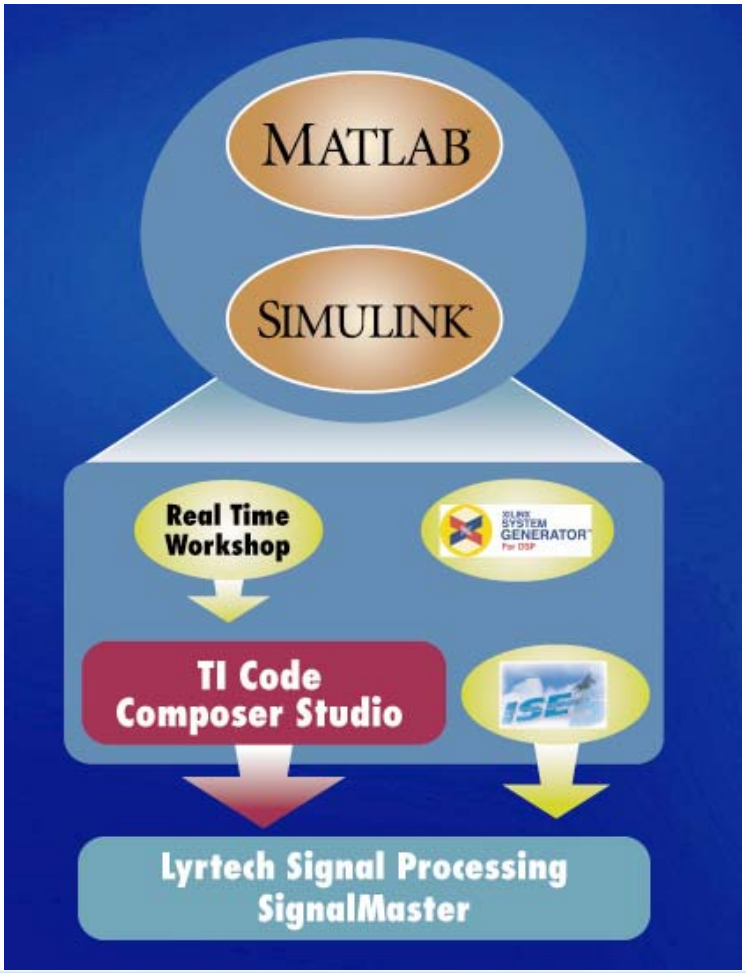

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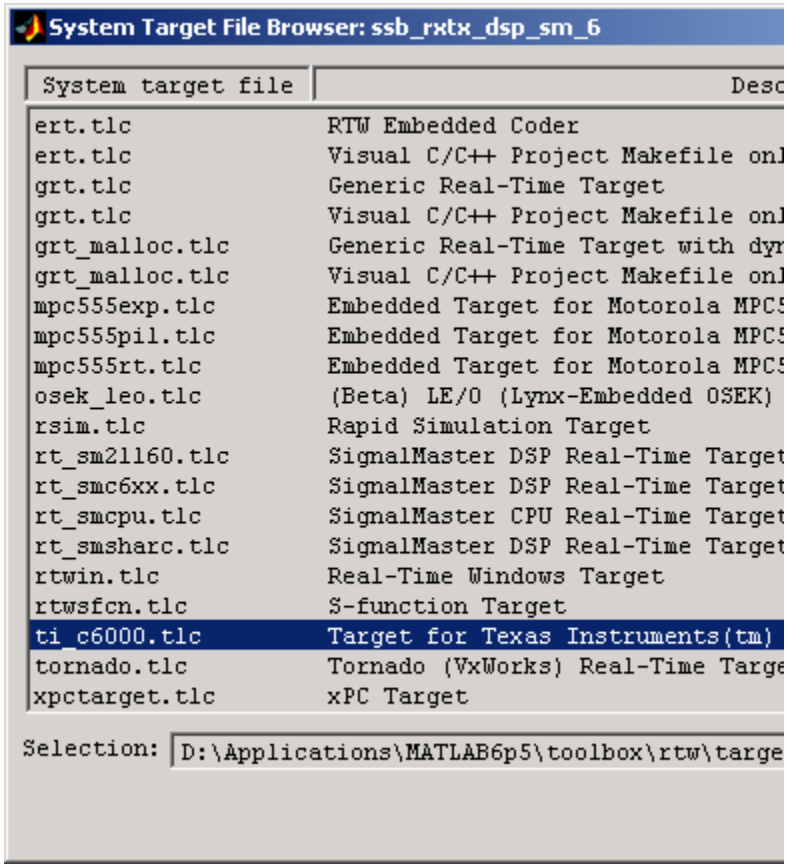

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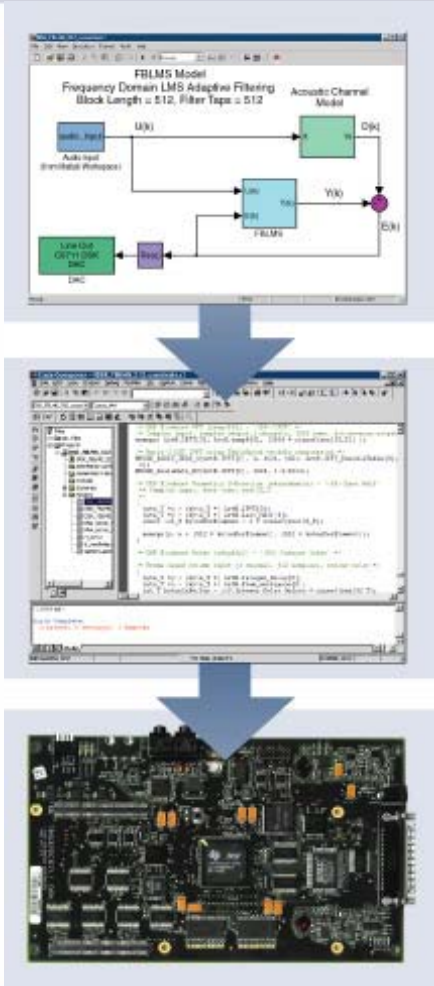

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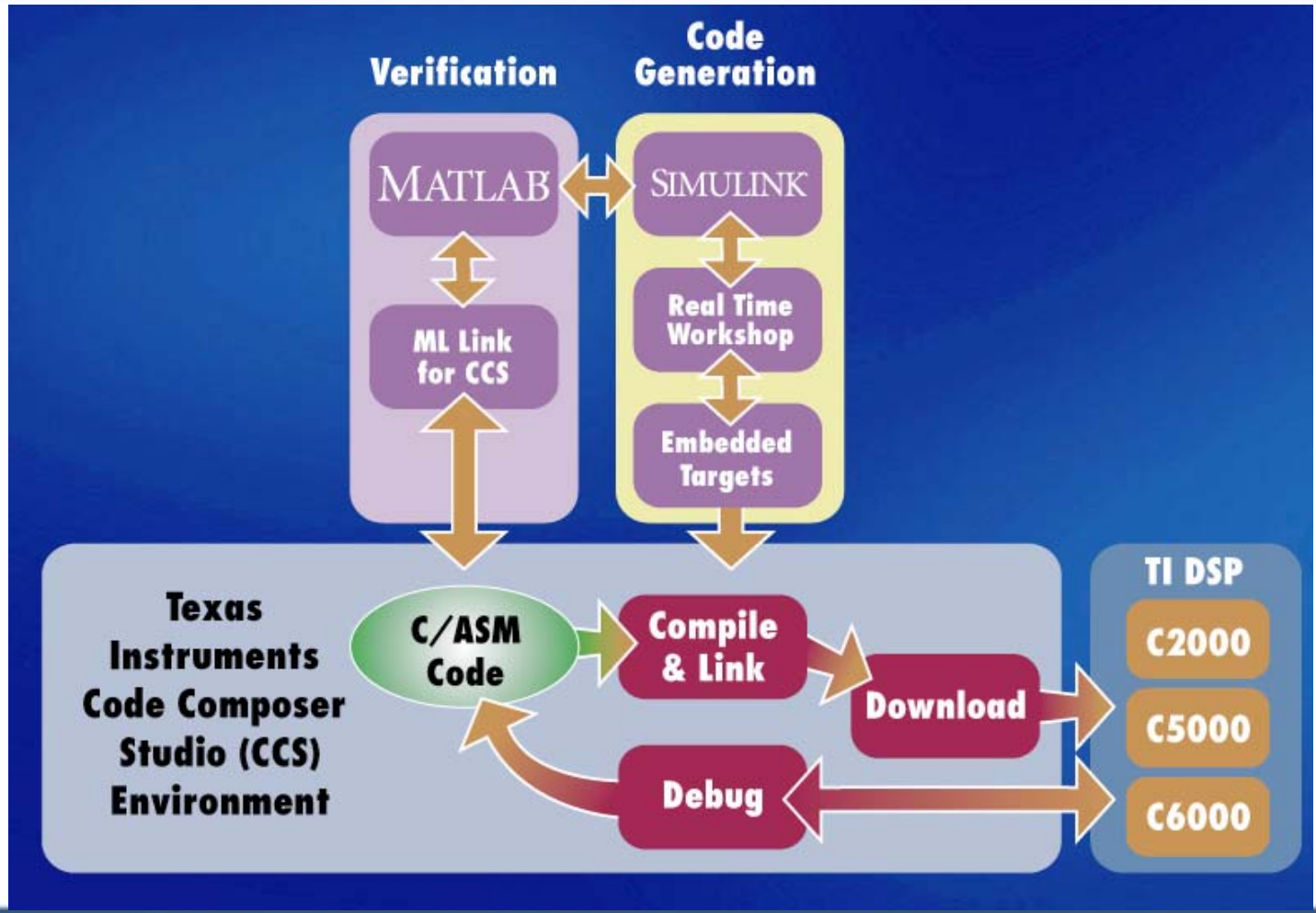
Software Flow To TI DSP



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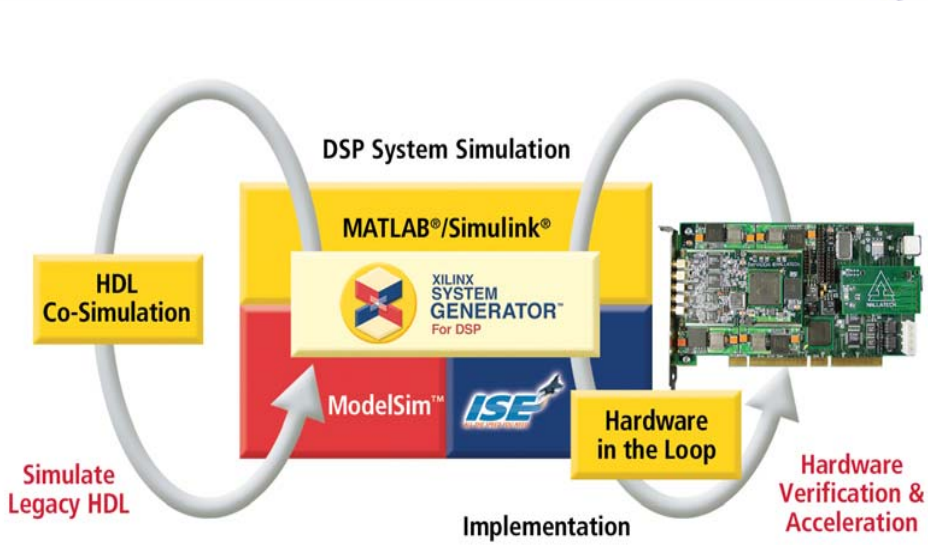

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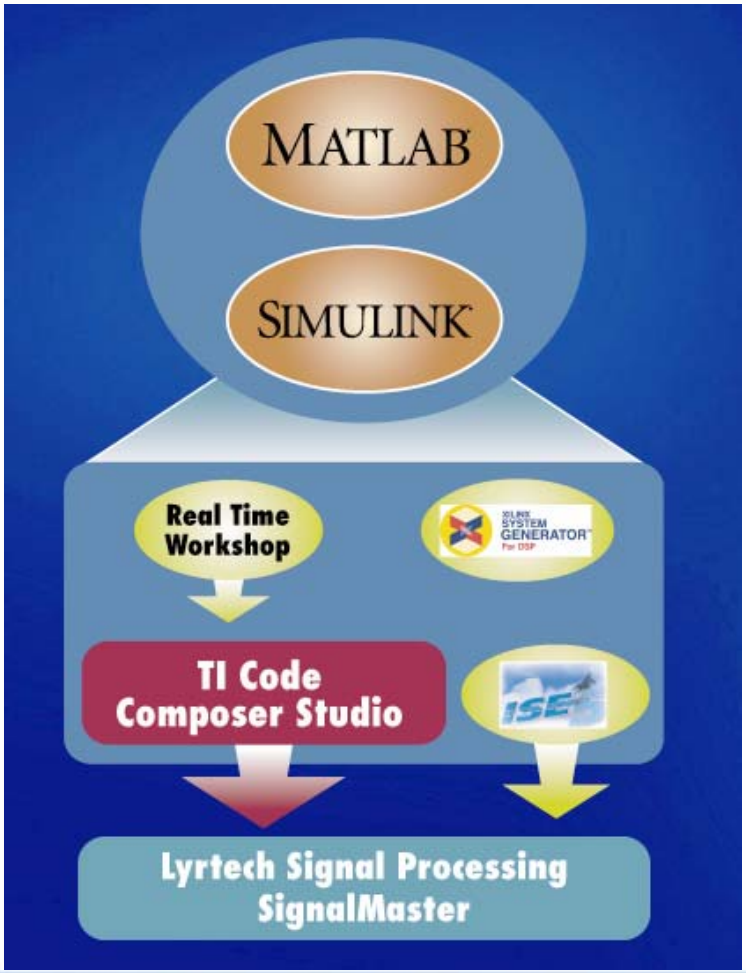

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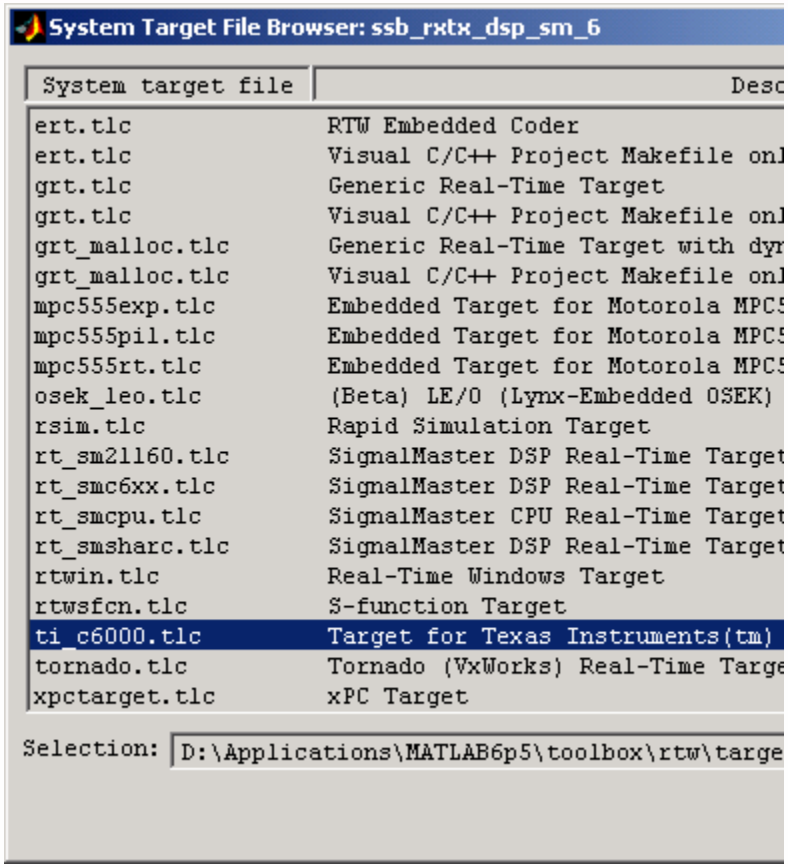

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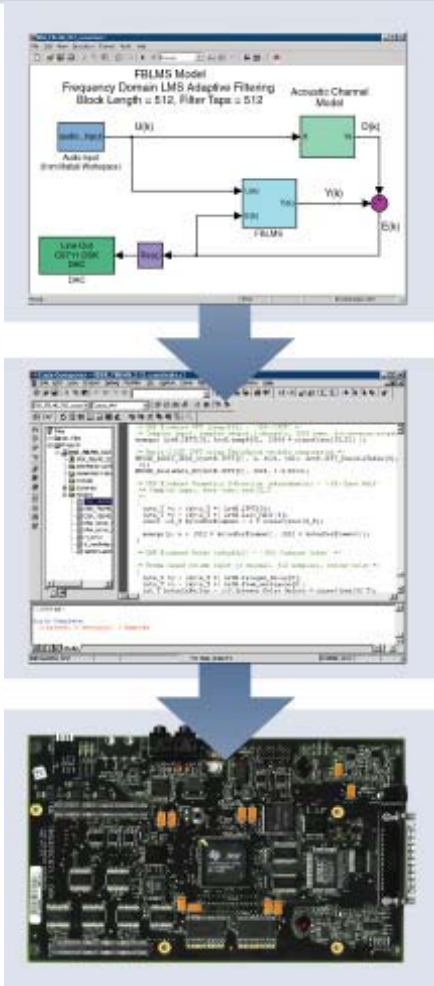

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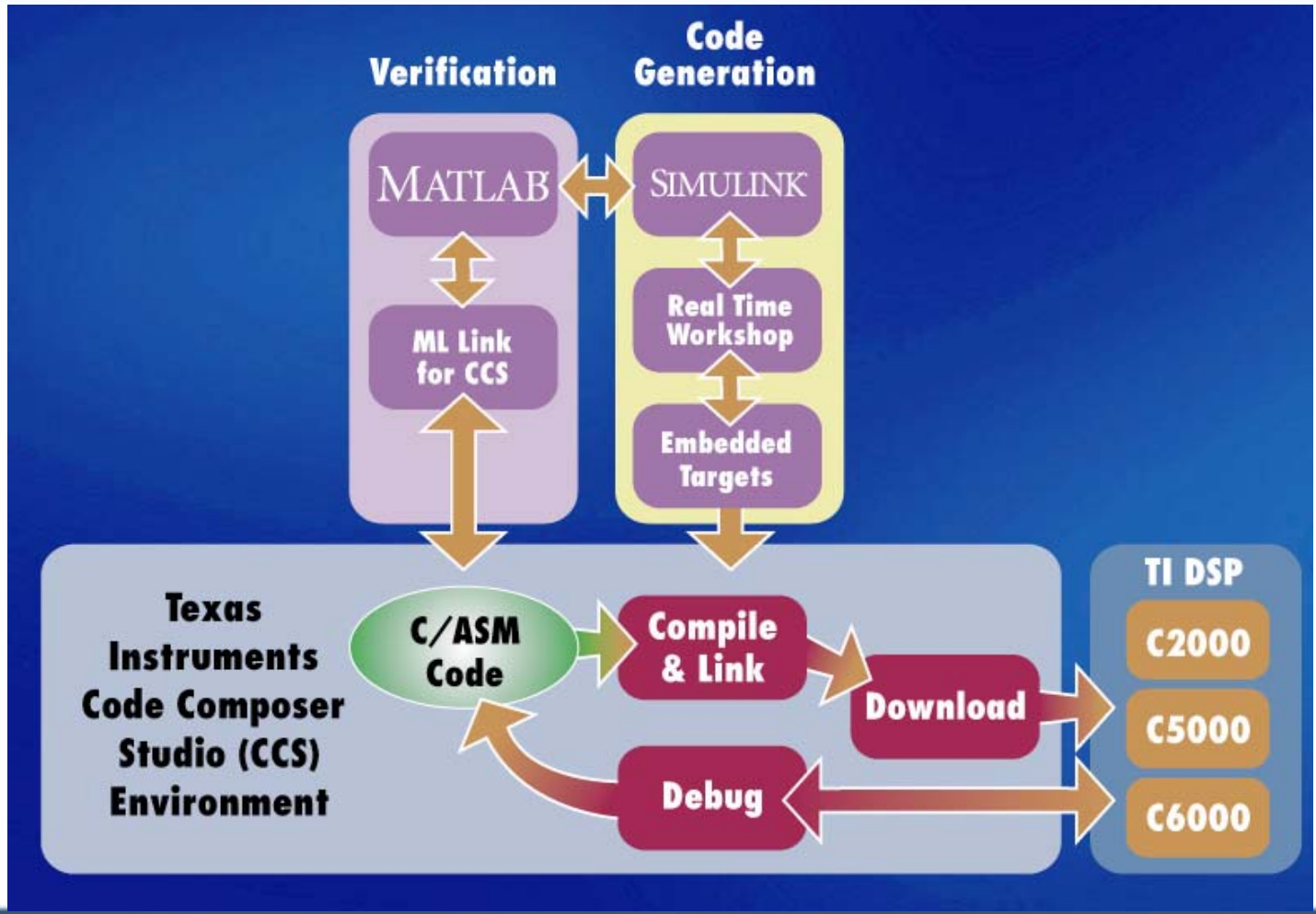

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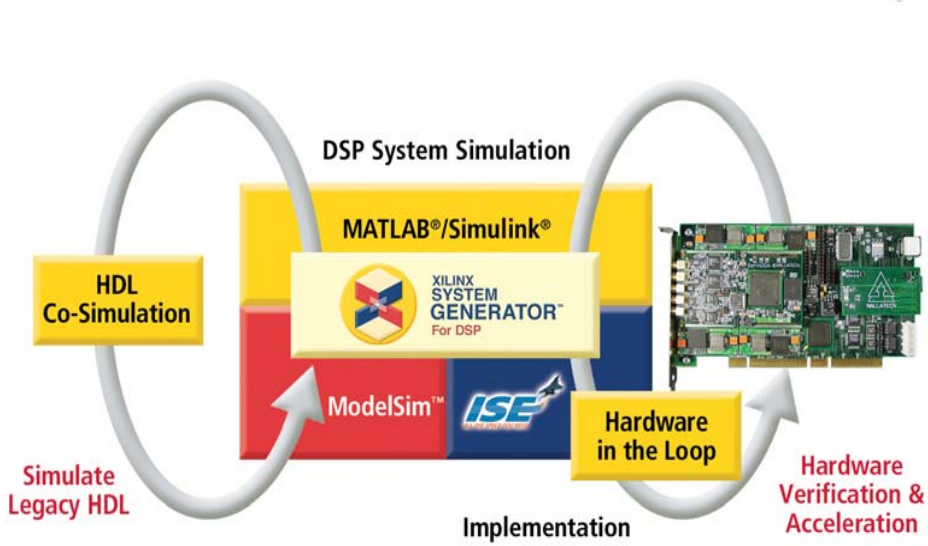

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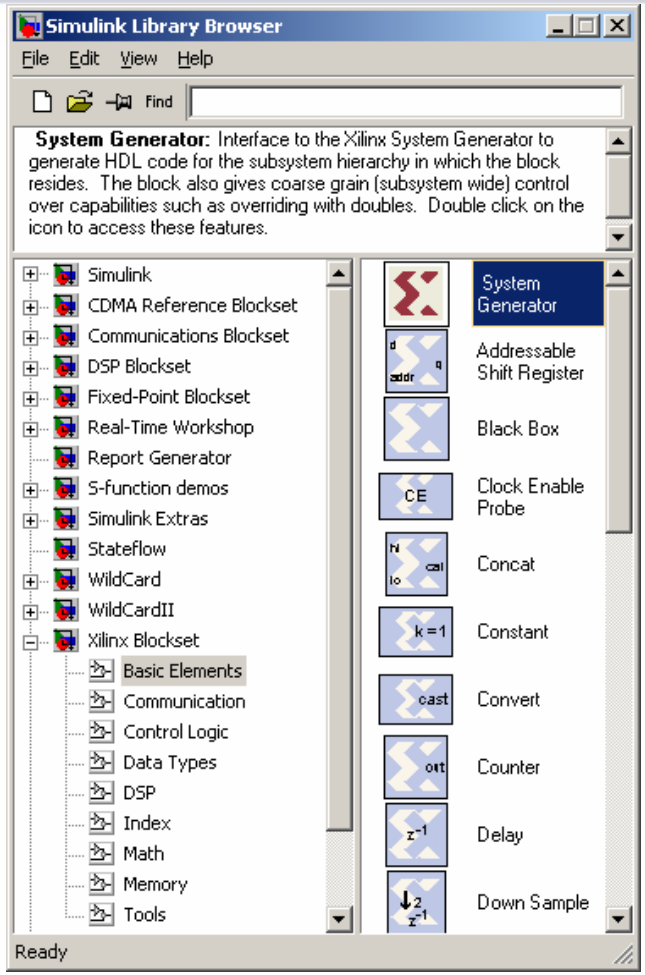
Xilinx Blockset

- **Basic elements**
  - Counters, delays, up/down samplers,…
- **Communication**
  - Error correction blocks, AWGN,…
- **Control Logic**
  - Microcontrollers, FSMs, m-code,…
- **Data Types –** Converters, gateways,…
- **DSP –** Filters, FFT, DDS, FDATool,…
- **Math –** Multiply, add, compare,…
- **Memory –** RAM, ROM, registers,…
- **Tools –** FDATool, ModelSim,…



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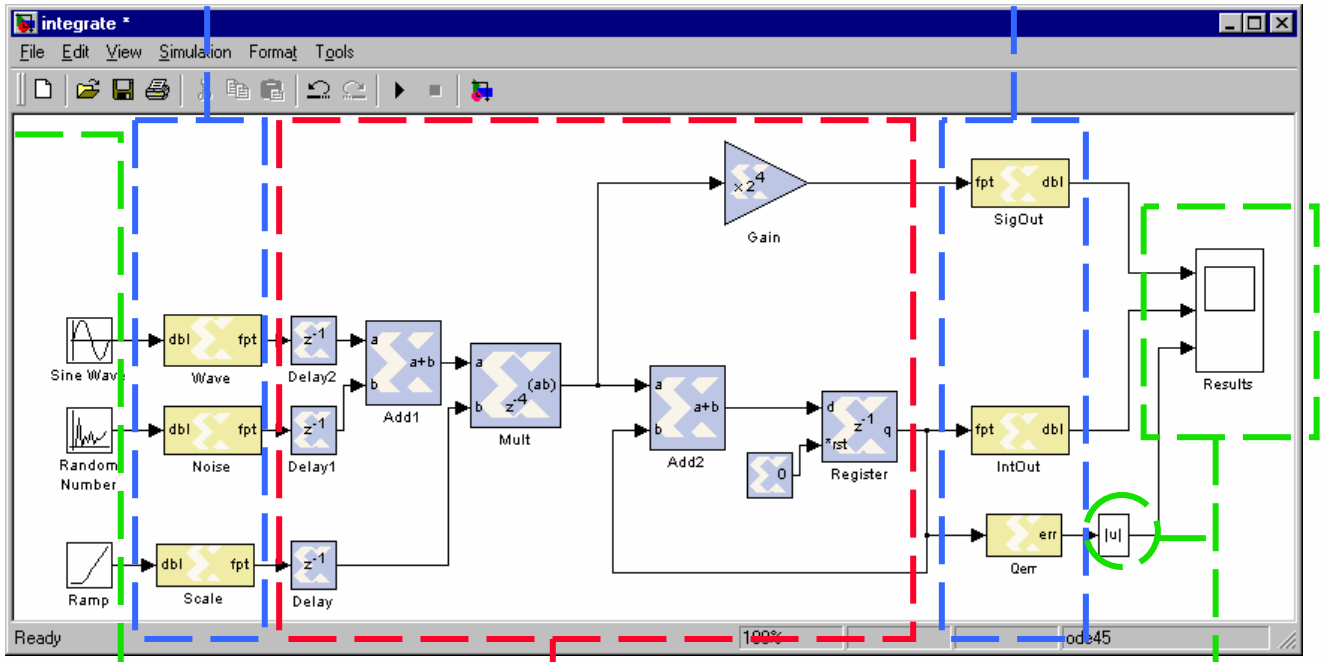
Creating a System Generator Design

IO blocks used as interface between the Xilinx blockset and other Simulink blocks



Simulink sources

SysGen blocks realizable in hardware

Simulink sinks & library functions

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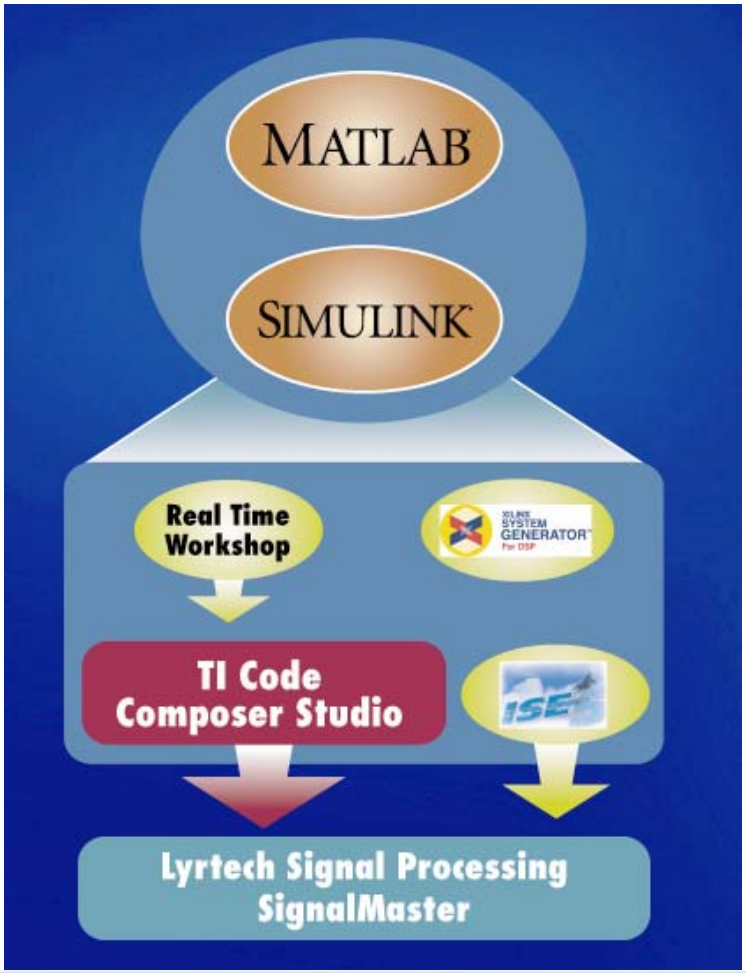
Hardware Implementation Flow



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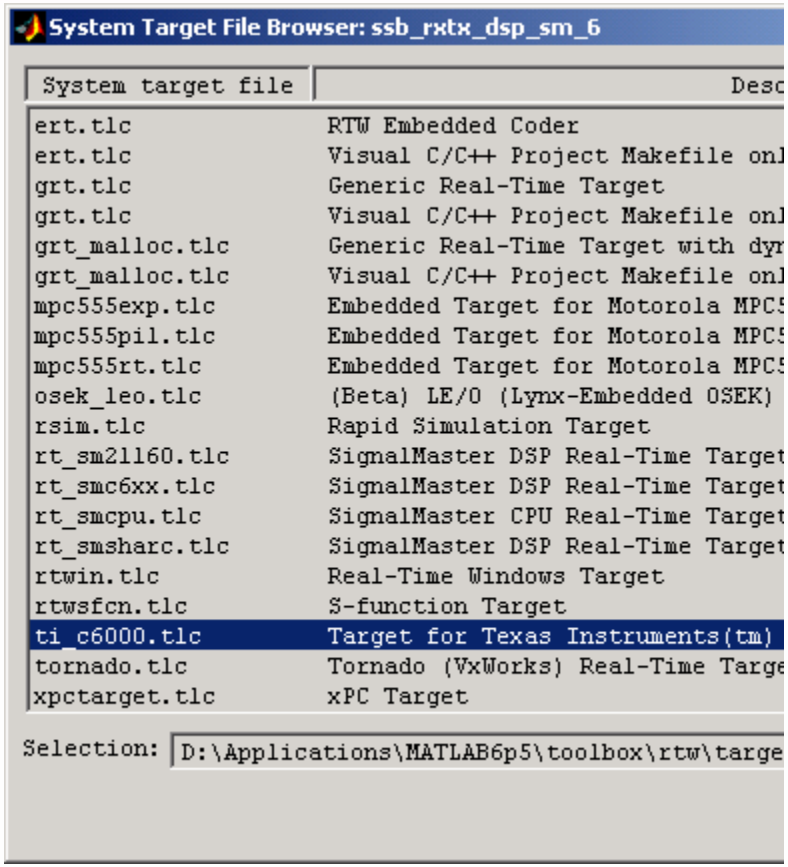

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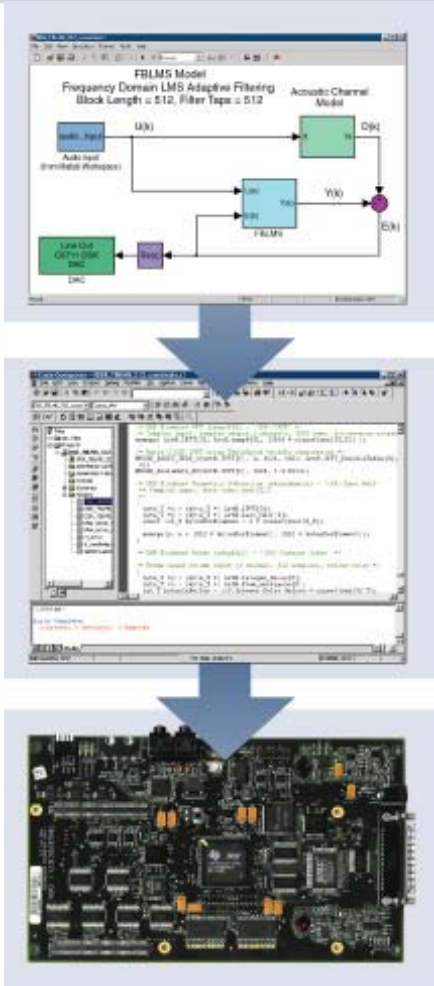

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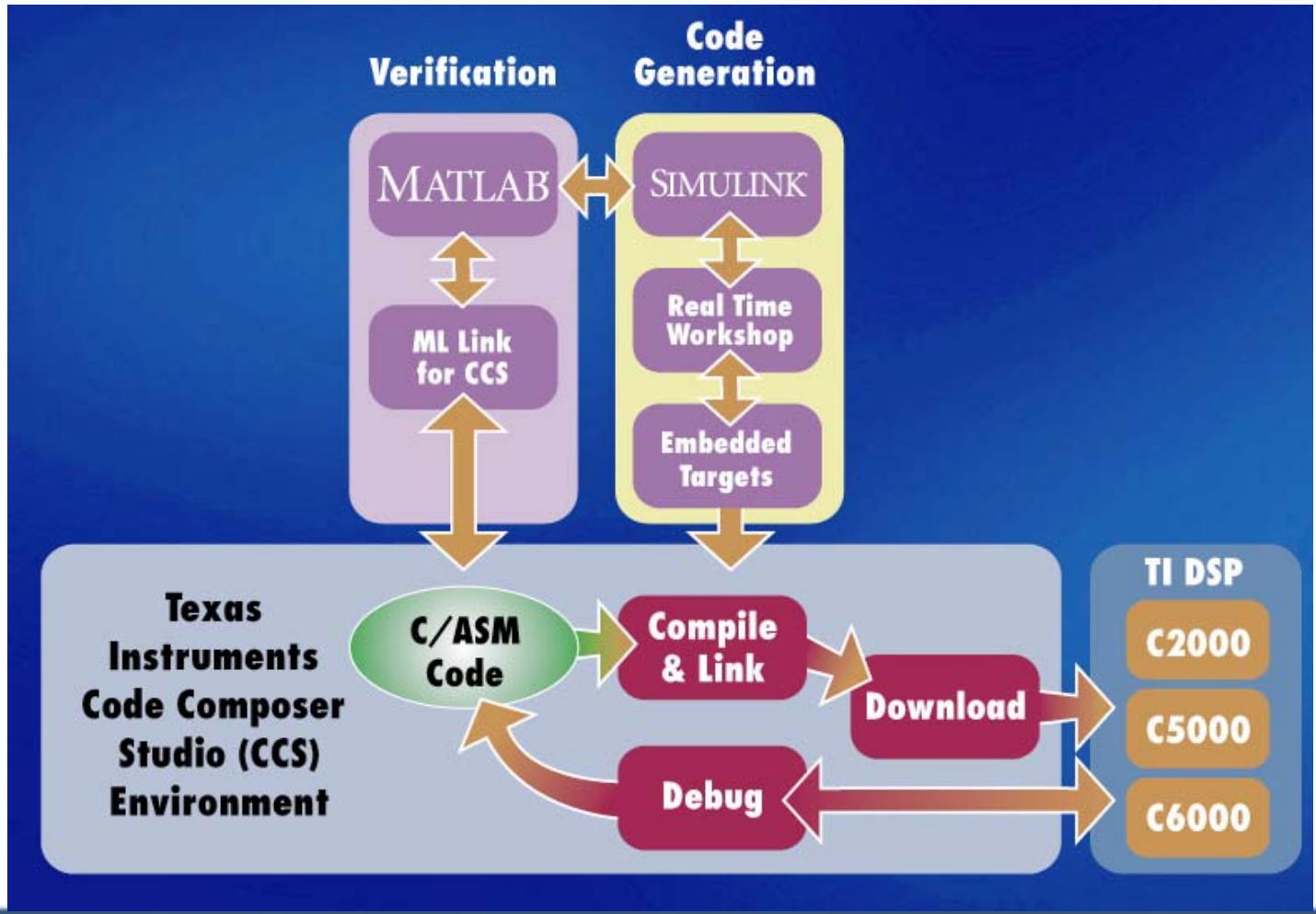

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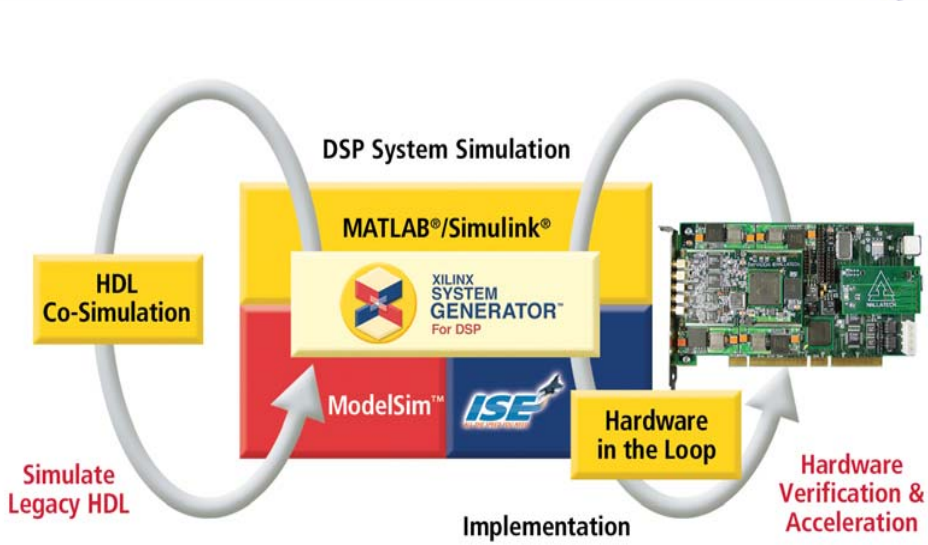

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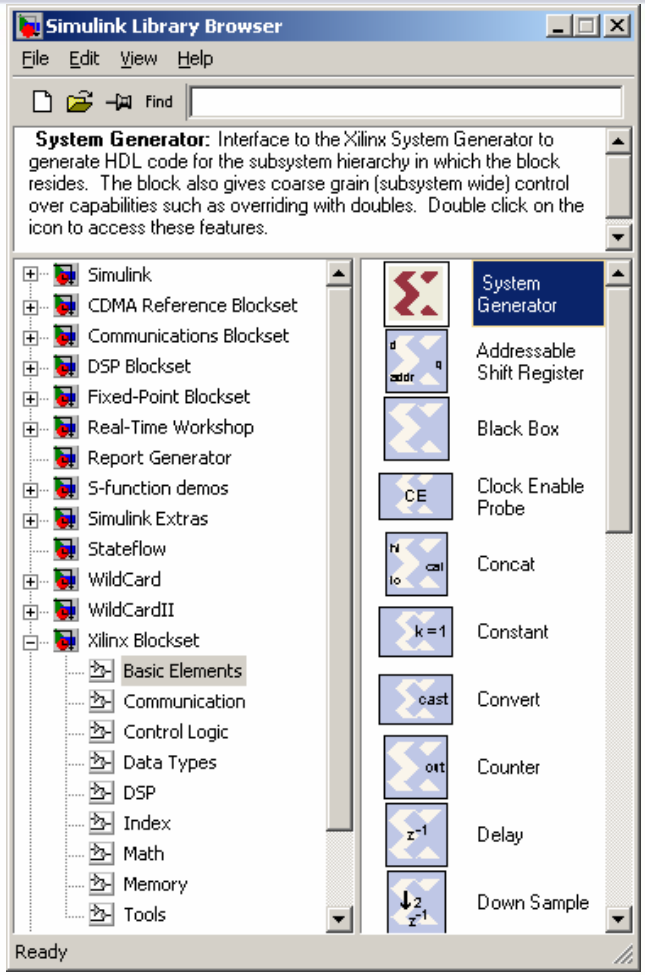

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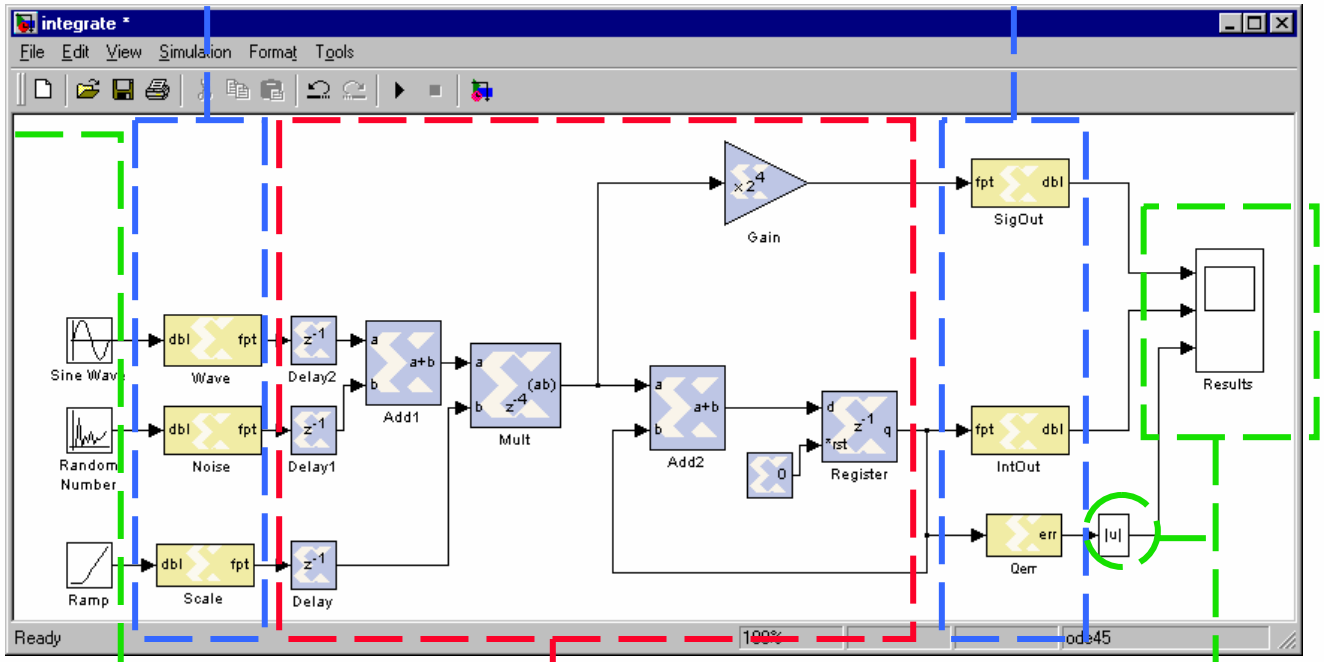

Simulink sources

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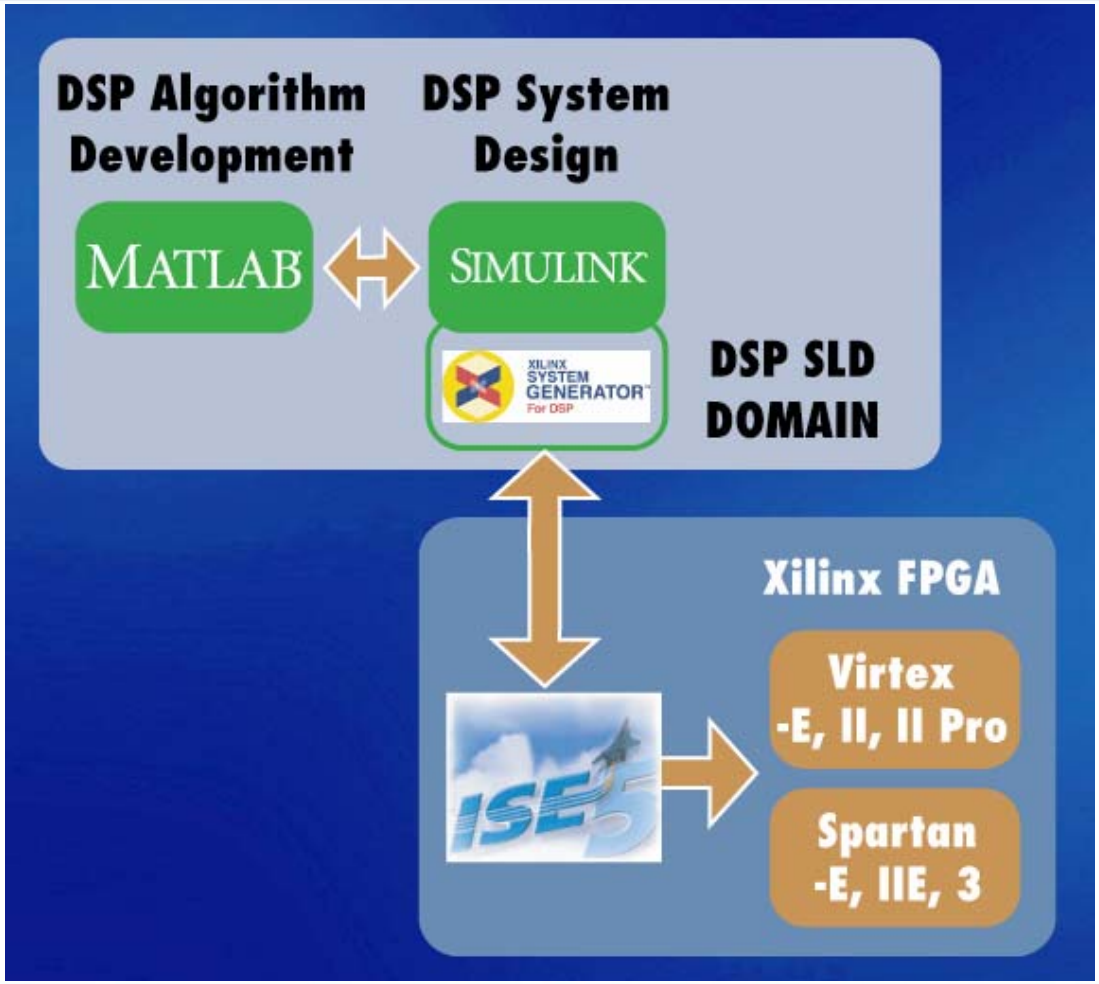
Software Flow To Xilinx FPGAs



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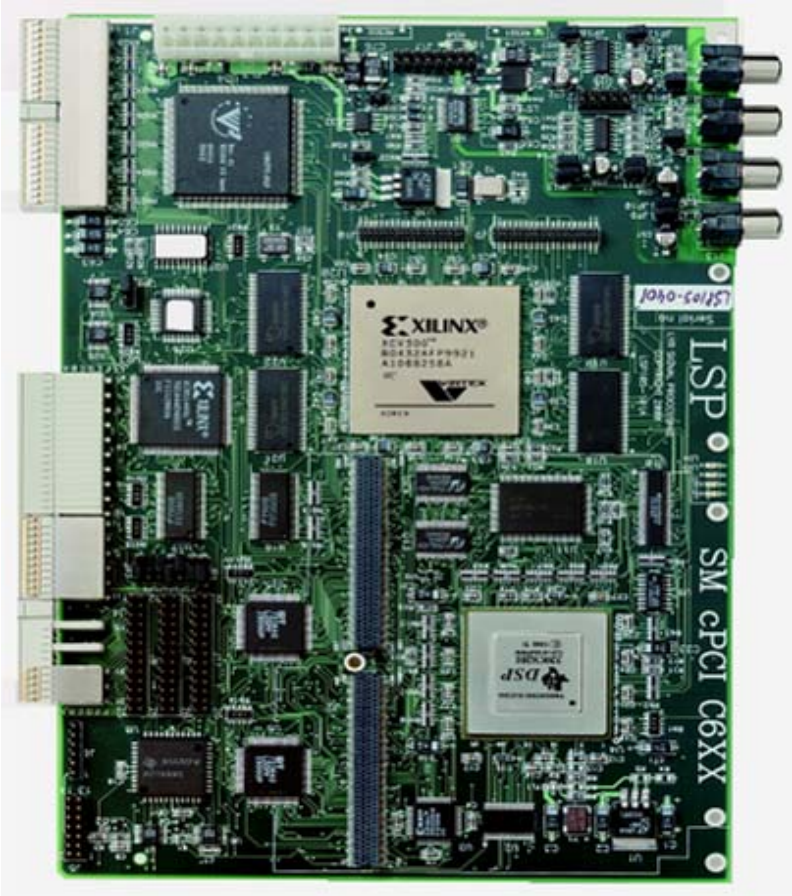
Development Hardware



- Annapolis Micro Systems
- Bittware
- LYRtech Signal Processing
- Nallatech
- Sundance
- TI DSK & EVM
- And more….

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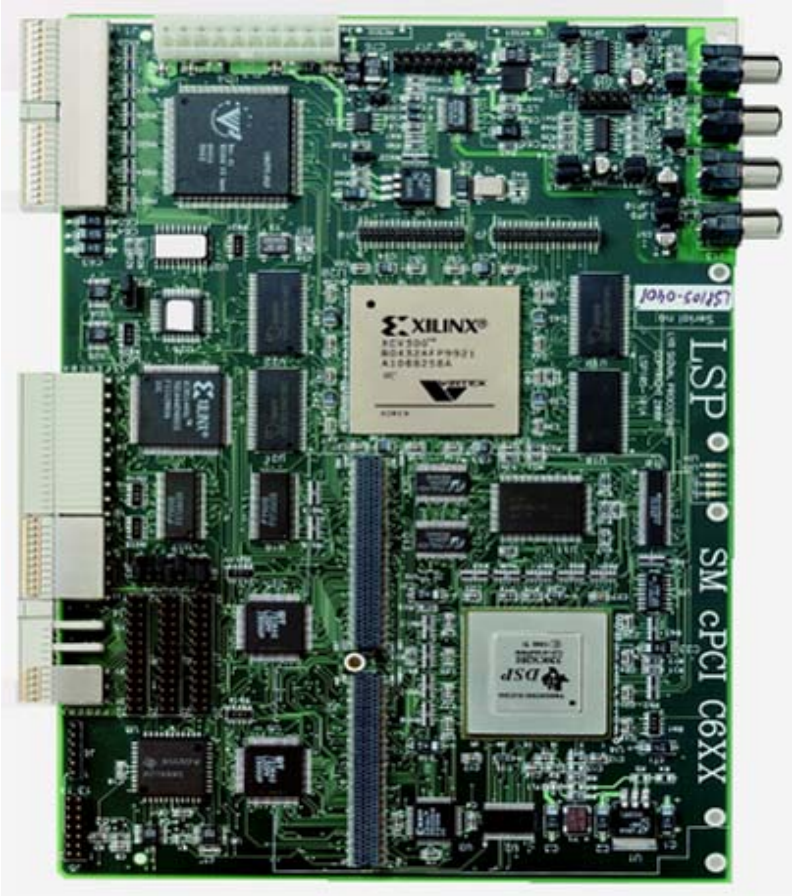
Development Hardware



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Case Study: SSB Software Defined Radio

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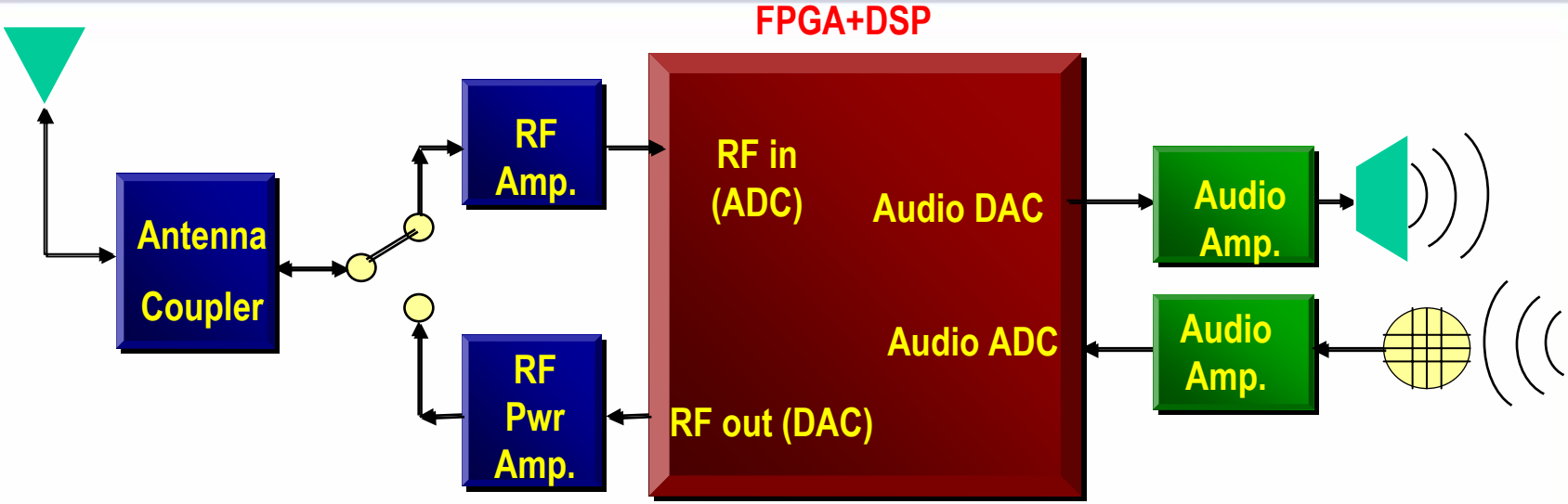
Complete Communication Link



- FPGA for radio frequency processing (64 MSPS In, 64 MSPS Out)
  - Frequency translation
  - Filtering and sample rate conversion
  - Possibly spread spectrum
- DSP for audio rate processing and control
  - Demodulation
  - Encryption / decryption
  - User interface and control

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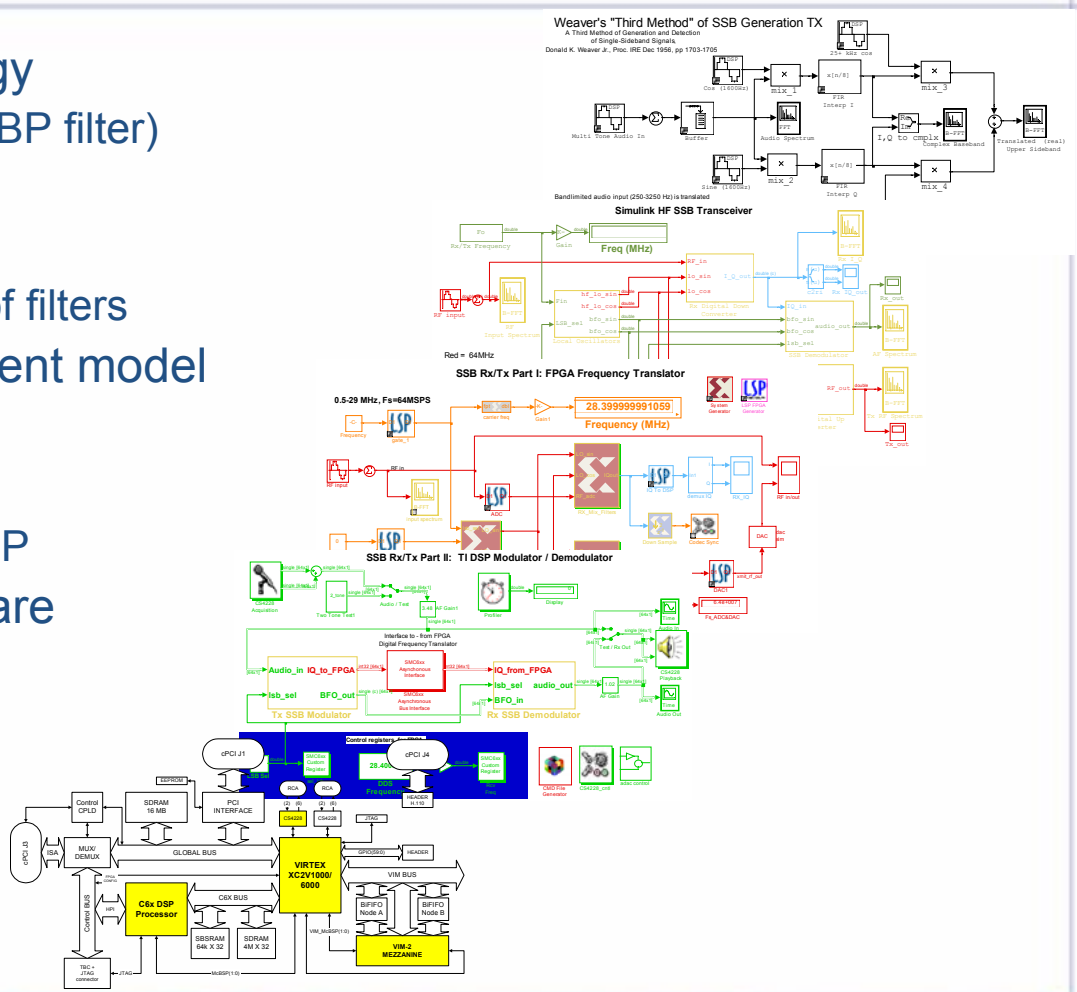
Design Process

- Select basic system topology
  - **Weaver's** (not phasing or BP filter)
- Design digital filters
  - Multi rate design
  - Verify cascade response of filters
- Create hardware independent model
- Partition design
  - RF processing → FPGA
  - Audio processing → TI DSP
- Implement on target hardware



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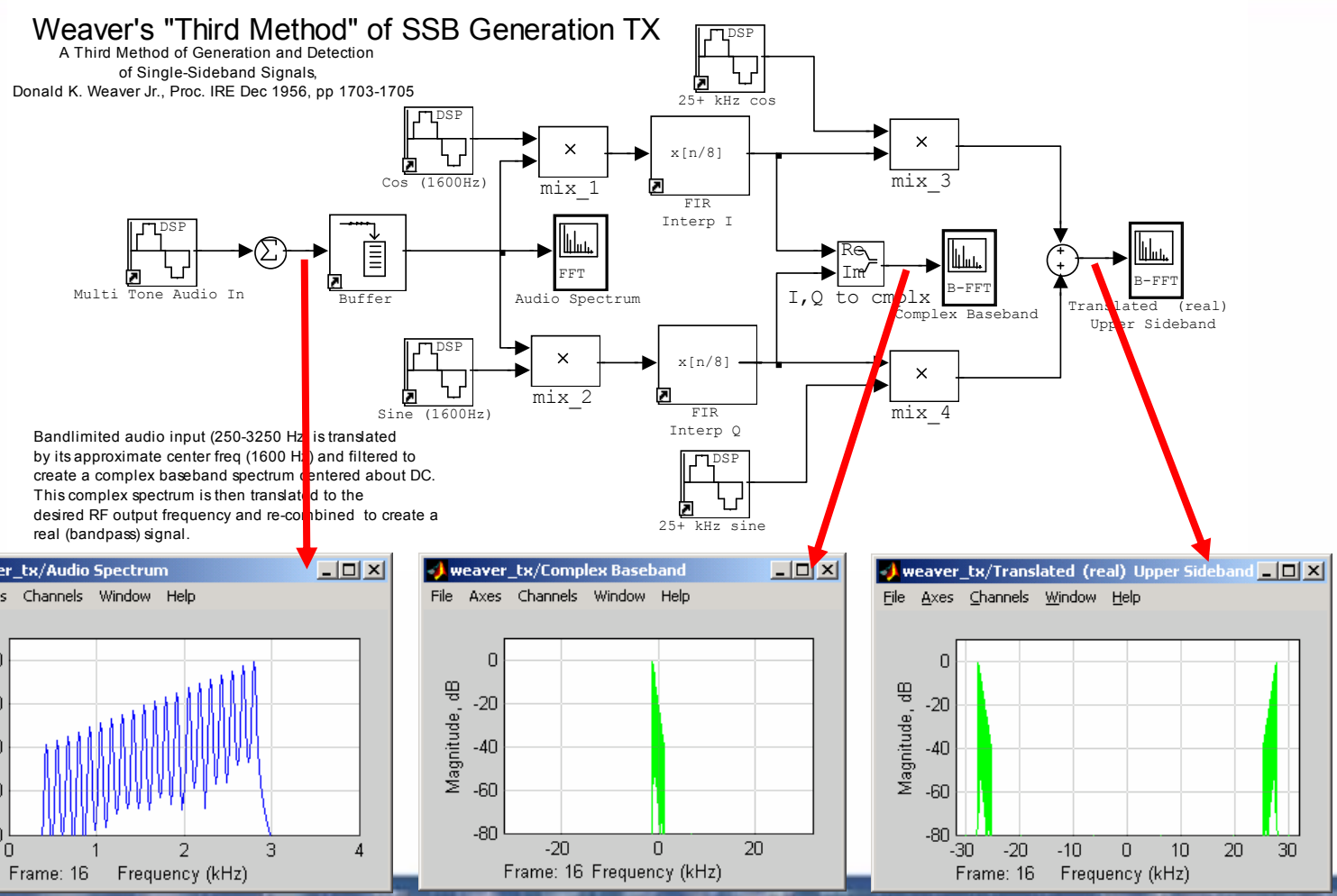
Weaver Topology



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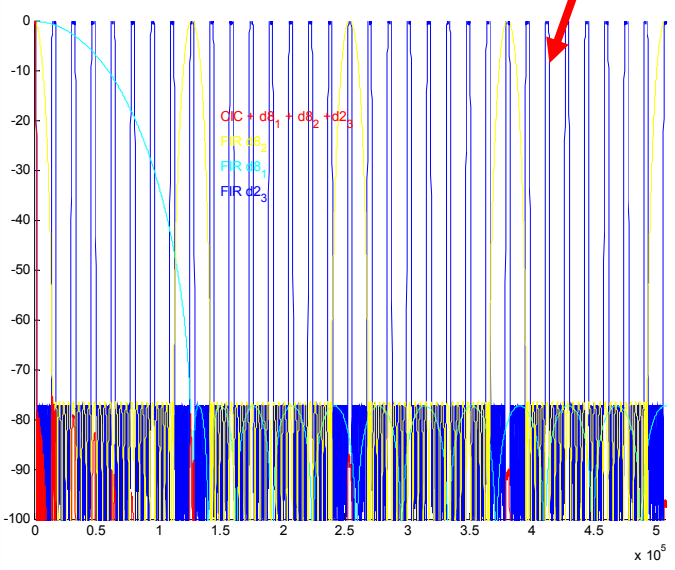
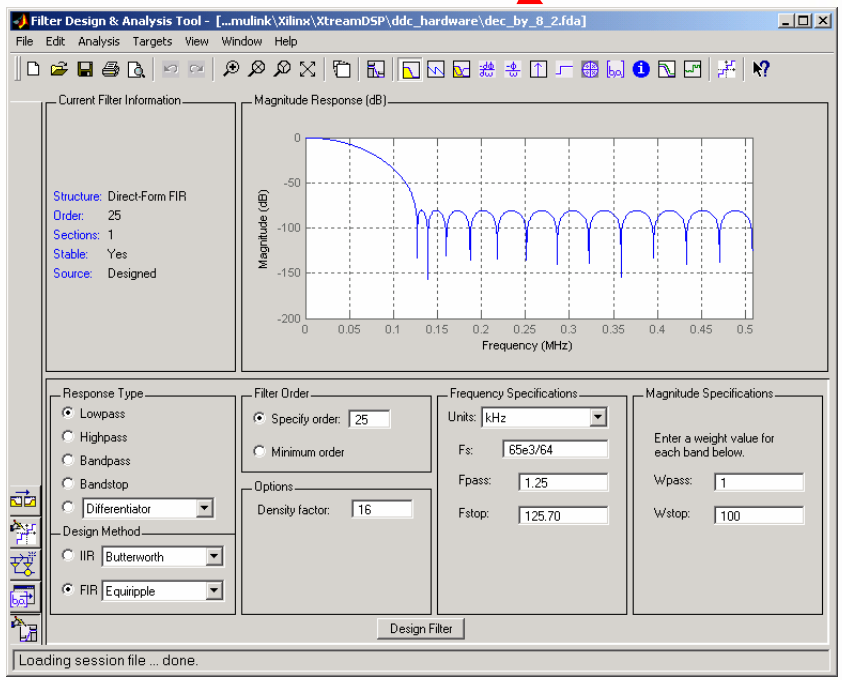
Multirate Filter Design

- Need overall decimation / interpolation of circa 8000 (64MHz/8000) = 8000 Hz
- Mandates a multi-stage multi-rate design
- Determine coefficients with filter design and analysis tool
- Use MATLAB for composite filter response (D=64*8*8*2=8192)
  - D=64 Cascaded Integrated Comb
  - D=8 FIR (25 tap)
  - D=8 FIR (30 tap)
  - D=2 FIR (54 tap)





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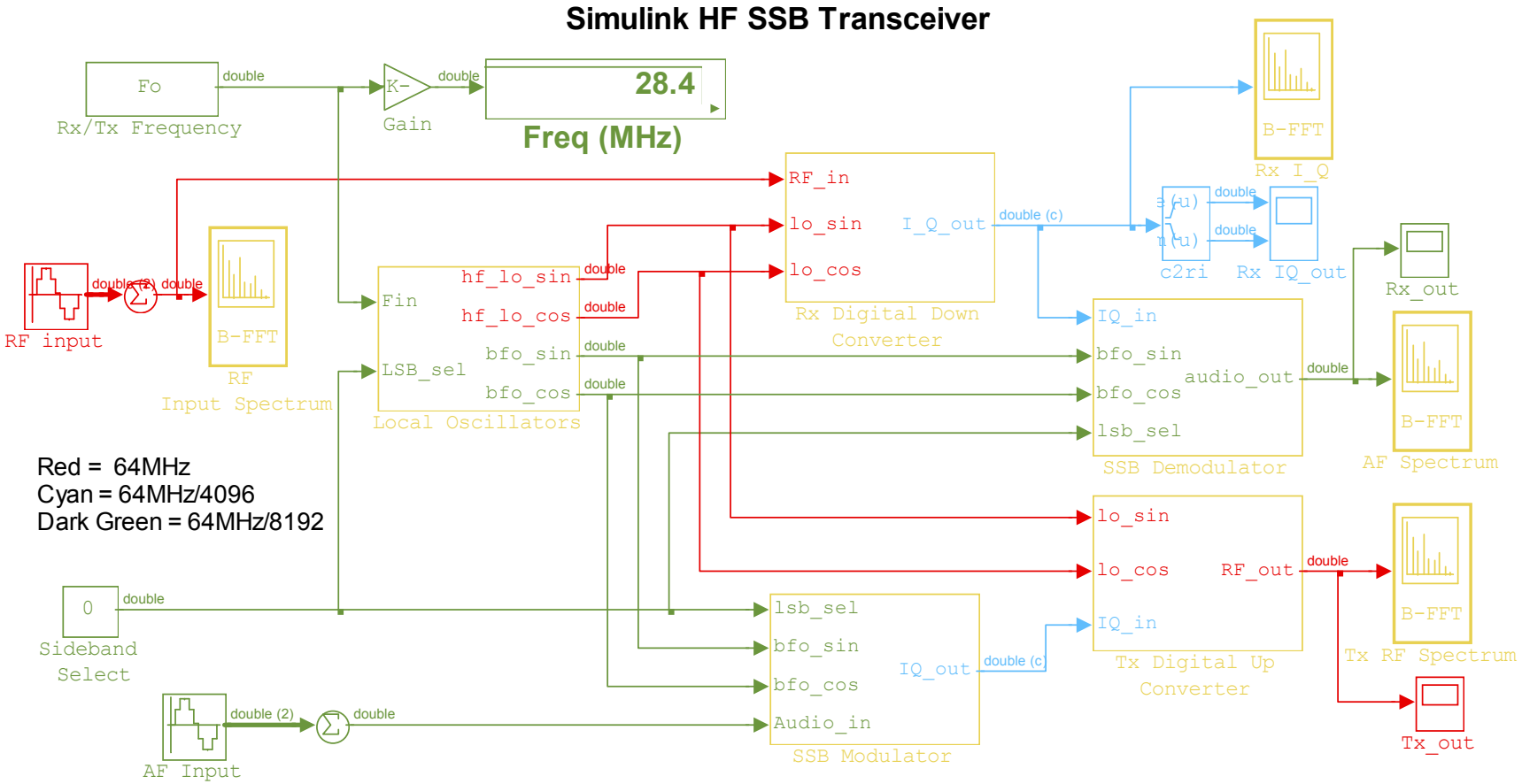
Hardware Independent Design



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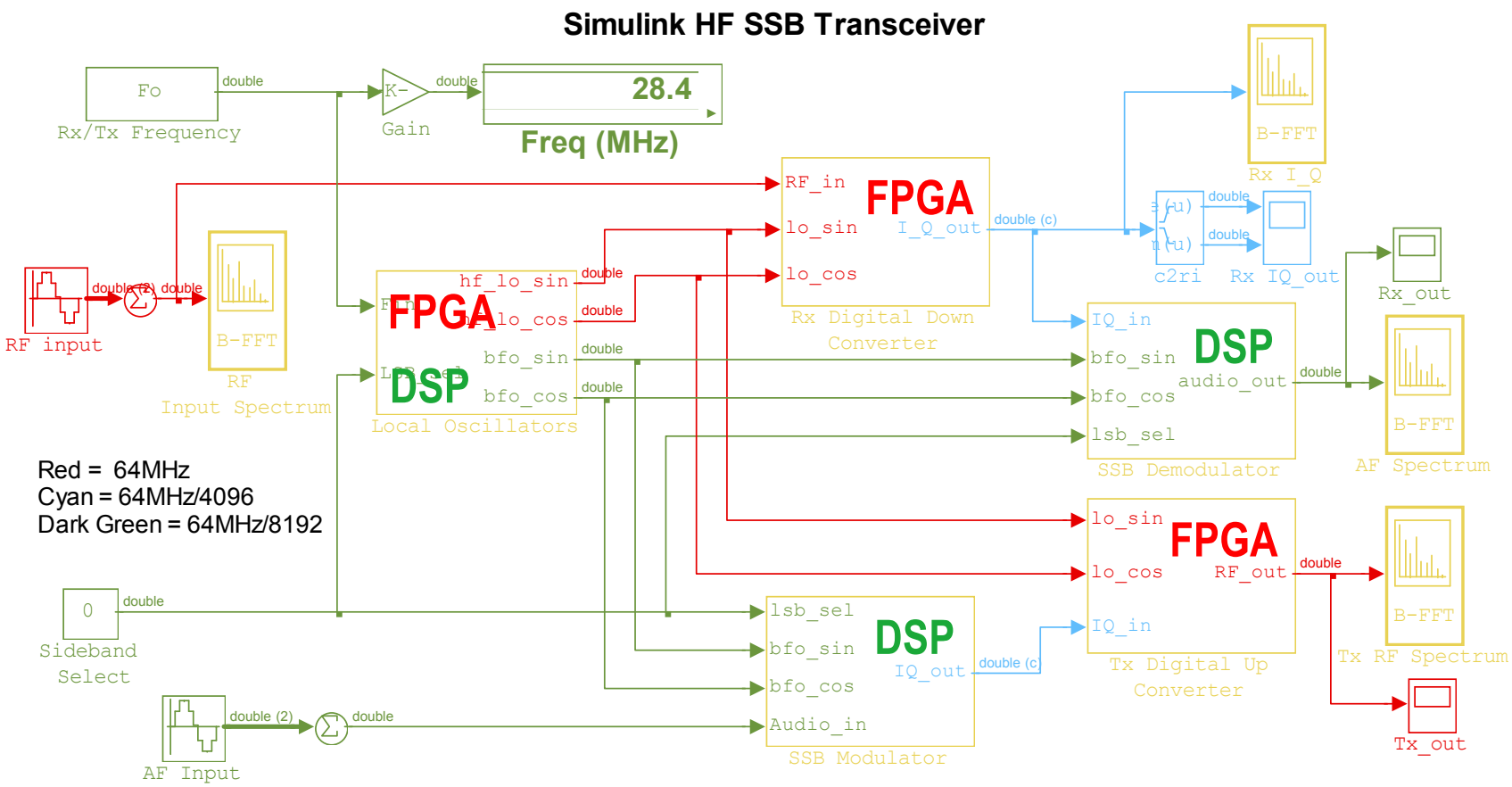
Partition the Design



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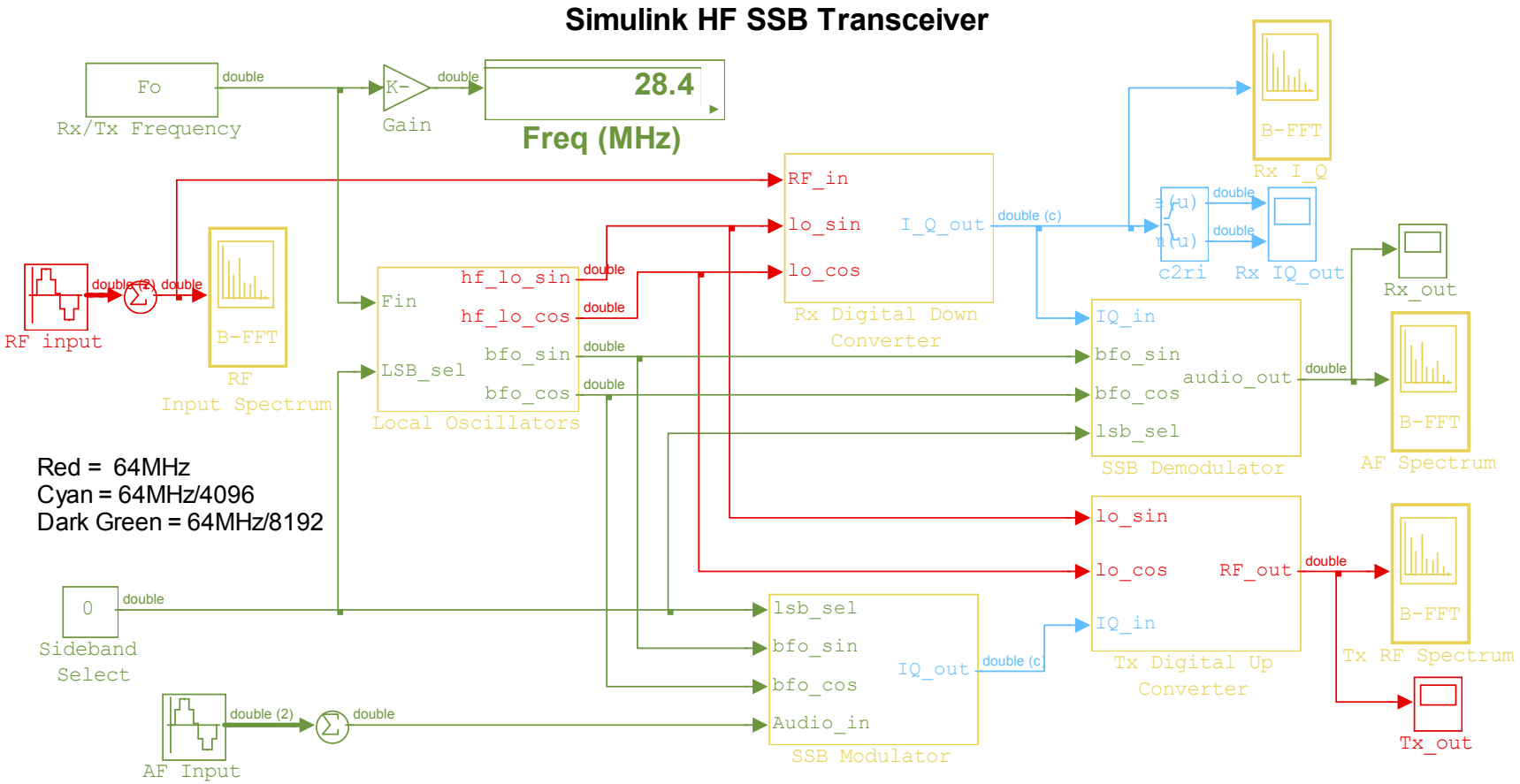
Hardware Independent Design



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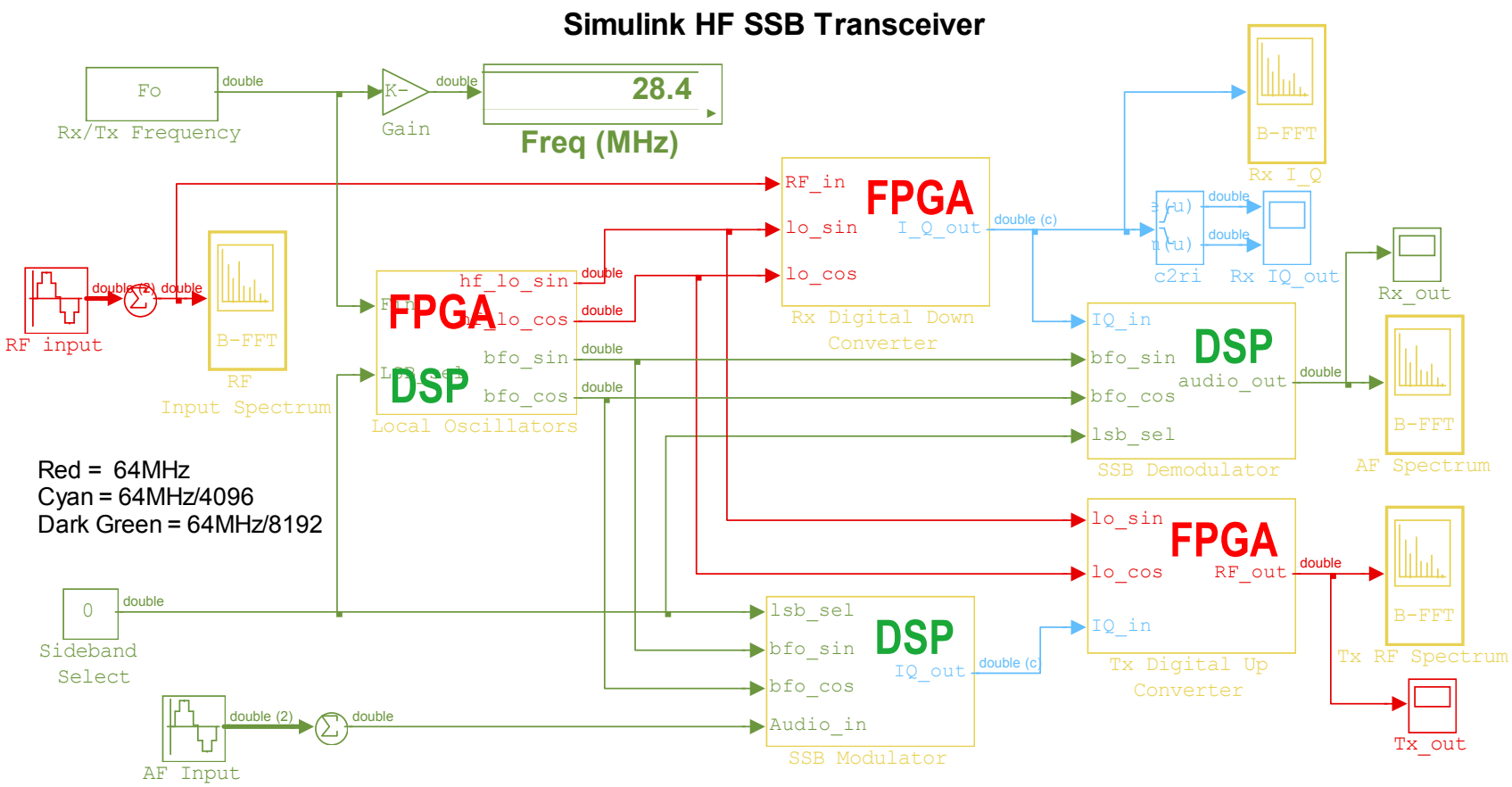
Partition the Design



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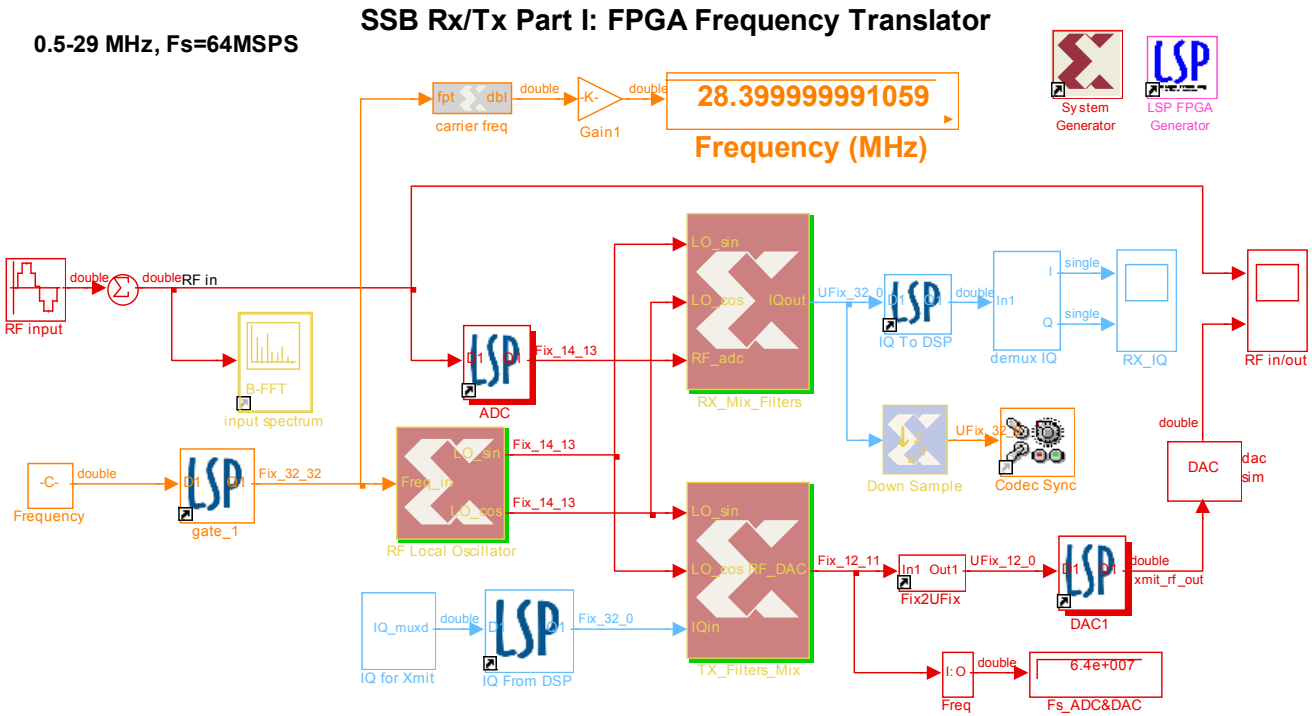
Part I: FPGA Frequency Translator

- Data rates
  - Rx: 64 MSPS in, 2 x 15.625 KSPS out (I/Q)
  - Tx: 2 x 15.625 KSPS in (I/Q), 64 MSPS out
- Gateways to and from TI C6701 DSP



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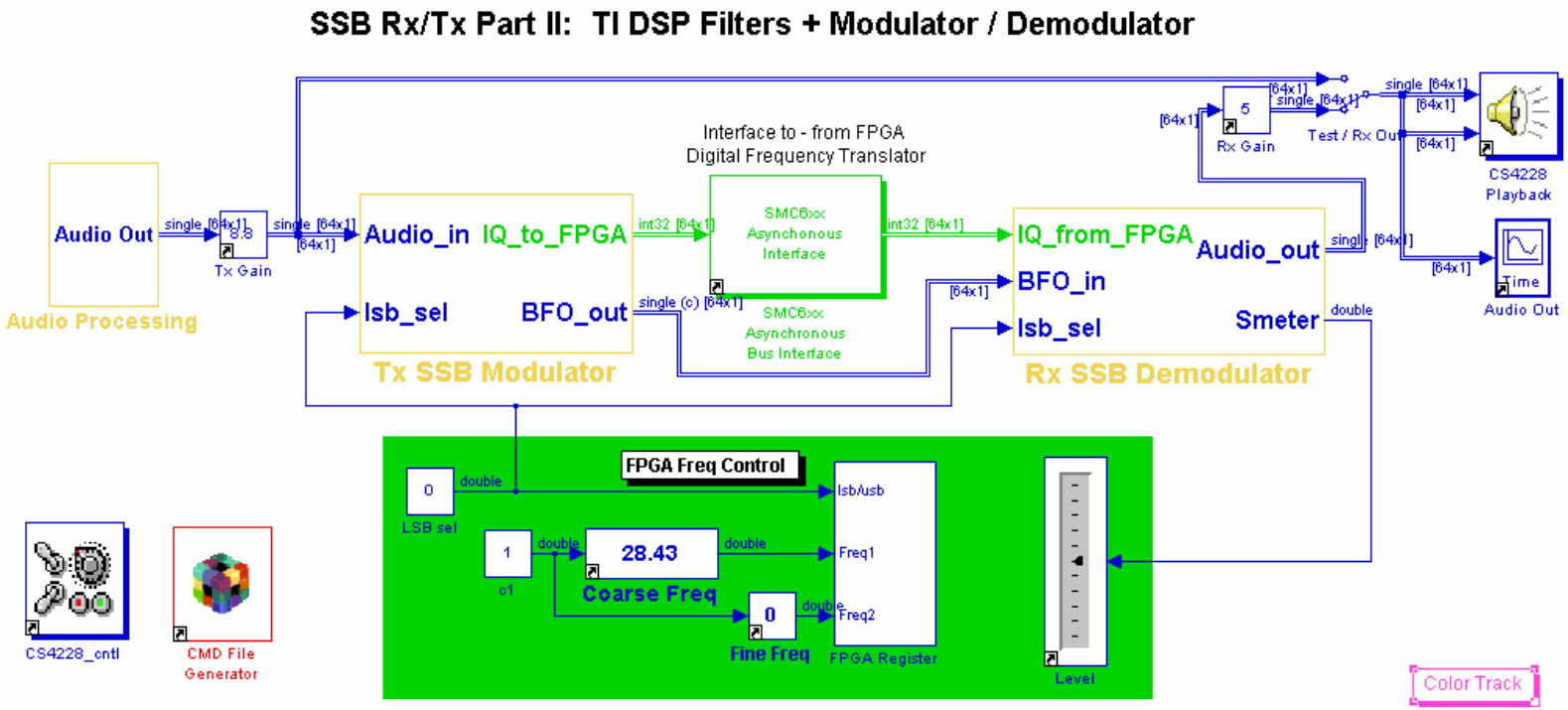
Part II: TI C6701 DSP Mod / Demod

- Automated code generation (Real Time Workshop)
- Gateways to / from FPGA
- Block diagram becomes test and debug GUI



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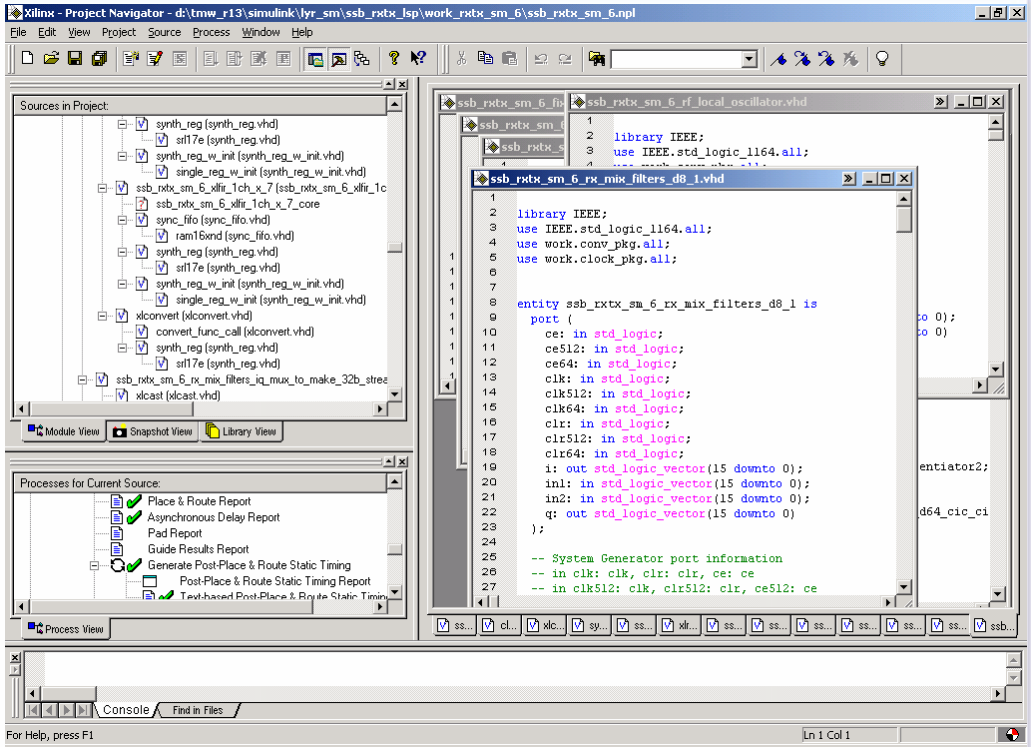
Code Statistics

- VHDL source
  - 167 files, 945 KB
  - 95% of xc2v1000 fabric
  - 128 MSPS throughput
- C source
  - 18 files, 243 KB
  - 22% of CPU horsepower
  - 80 KSPS throughput



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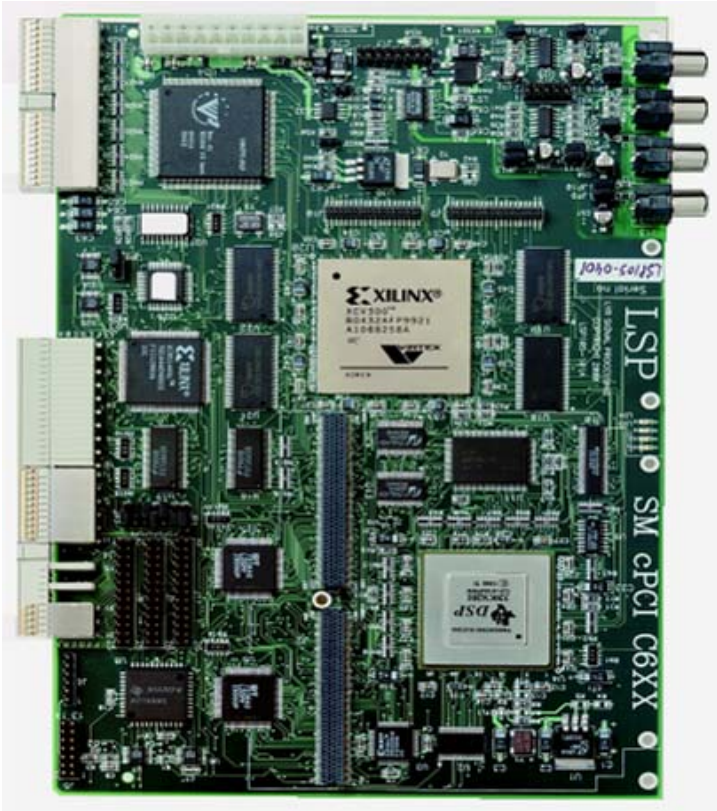
Development Hardware: Lyrtech SignalMaster



- Texas Instruments' C6701
- Xilinx XC2V1000
- DSP memory
  - 16MB SDRAM
  - 256 kB SBSRAM
- Codec
  - On board CS4228 CODEC from Crystal
  - 96kHz, 24-bit ADC and DAC
- 64Msps 14 bit ADC & DAC

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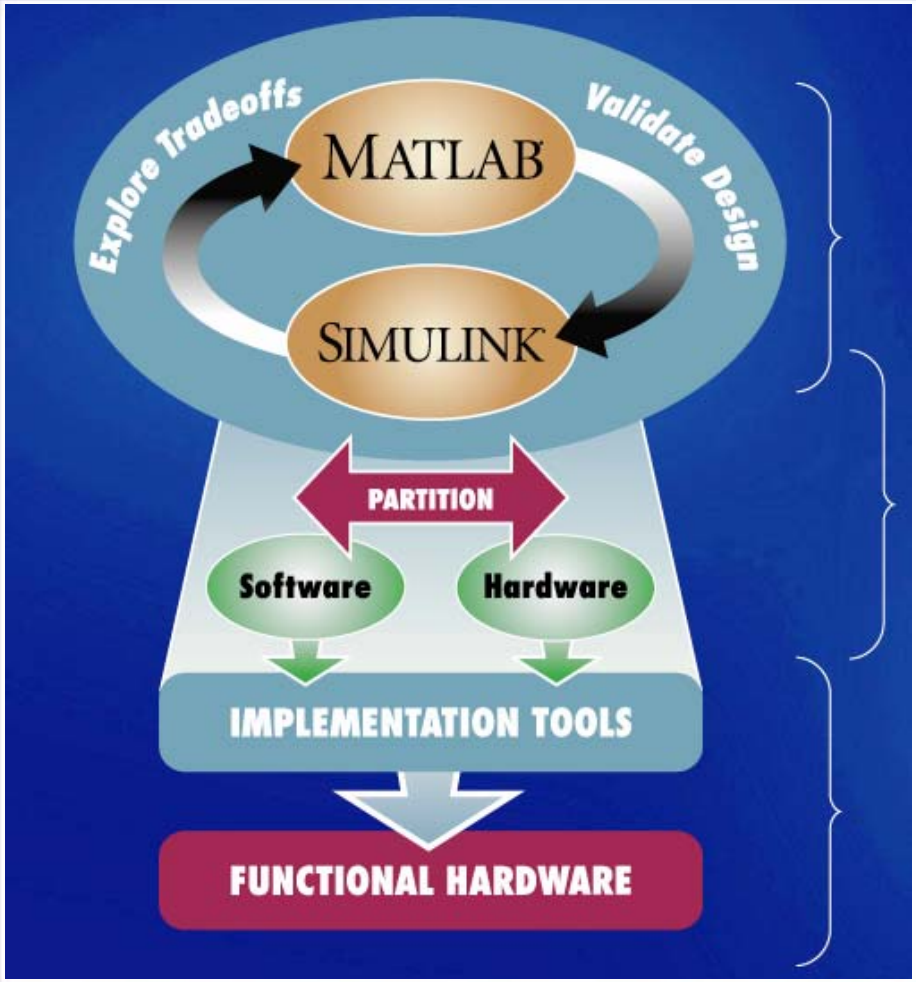
MathWorks Products for System-Level Design



- Create and validate design
- Detect design flaws early
- Reduce risk and time-to-market
- Use Simulink model as reference and executable specification

- Partition Design
- Add Implementation Detail

- Complete design flow to hardware (FPGA + DSP)

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Thank You

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