FPGA Co-Processors in SDR Signal Processing

Agenda

- Applications of FPGA-Based Co-Processors SDR
- Considerations for Co-Processor Design
- Development Tools & Methodologies Available from Altera to Build Co-Processors
  - SOPC Builder
  - DSP Builder
- FPGA Co-Processor Development Examples
  - QAM Modulator
  - FIR Filter

Techniques of Implementing of SDR System Reconfiguration

- Using parameterized radio (and protocol) modules
- Exchange of (a) single component(s) within a module
- Exchange of complete radio modules or protocol layers

Using parameterized radio (and protocol) modules

- Applicable within a standard
  - CDMA2000 – Spreading factors, Viterbi parameterization
  - 3GPP – spreading factor, Viterbi parameterization
- Not Applicable across widely varying standards
  - GSM, 3GPP – Need to replace entire physical layer
  - GSM, CDMA2000 – Need to replace entire network layer - GSM-MAP and ANSI-41

Exchange of (a) single component(s) within a module

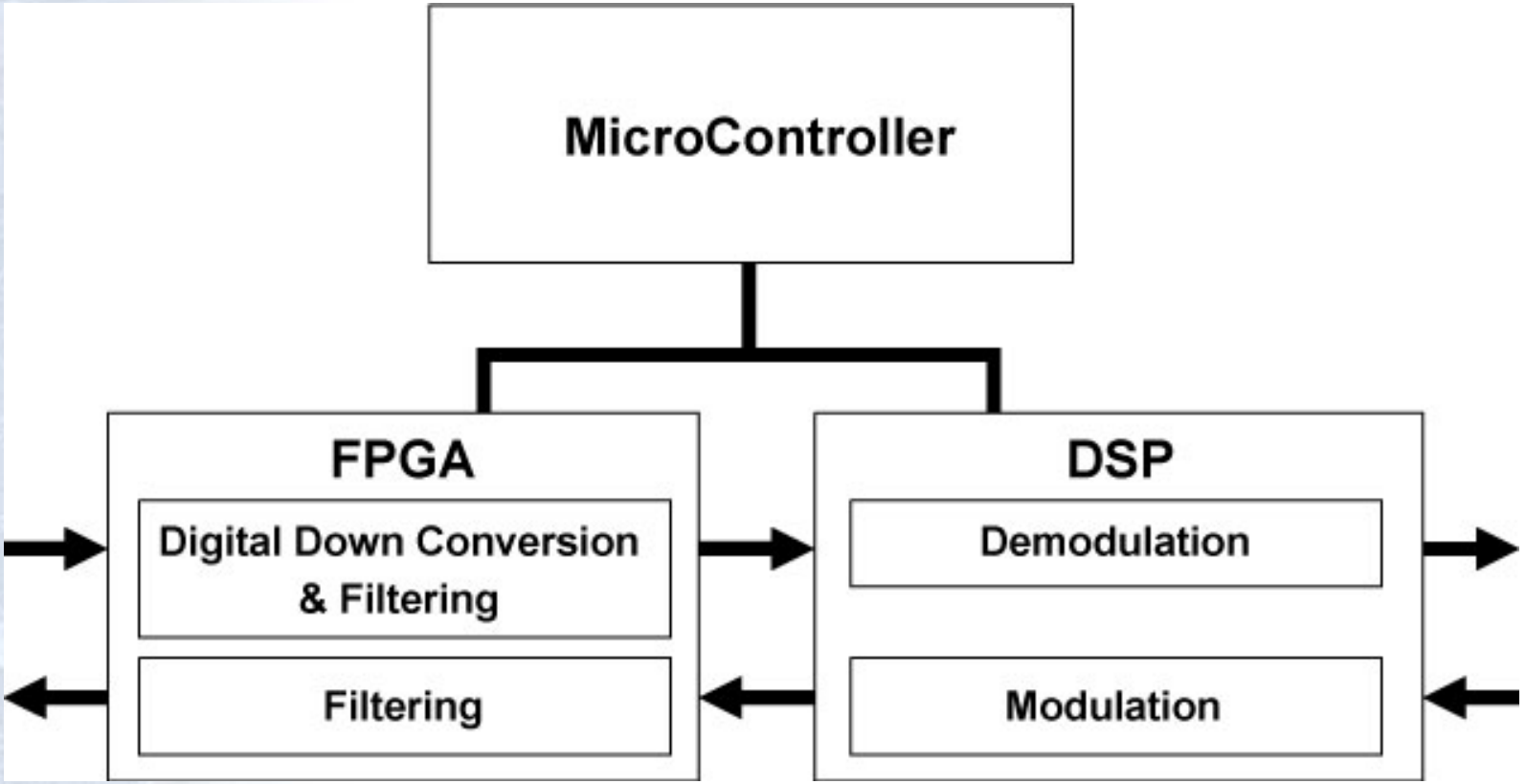
- Applicable within a standard
  - 3GPP – Turbo, Viterbi decoding
  - GSM/EDGE – Transceiver chain

- Not Applicable across widely varying standards
  - GSM, 3GPP – Need to replace entire physical layer
  - GSM, CDMA2000 – Need to replace entire network layer - GSM-MAP and ANSI-41

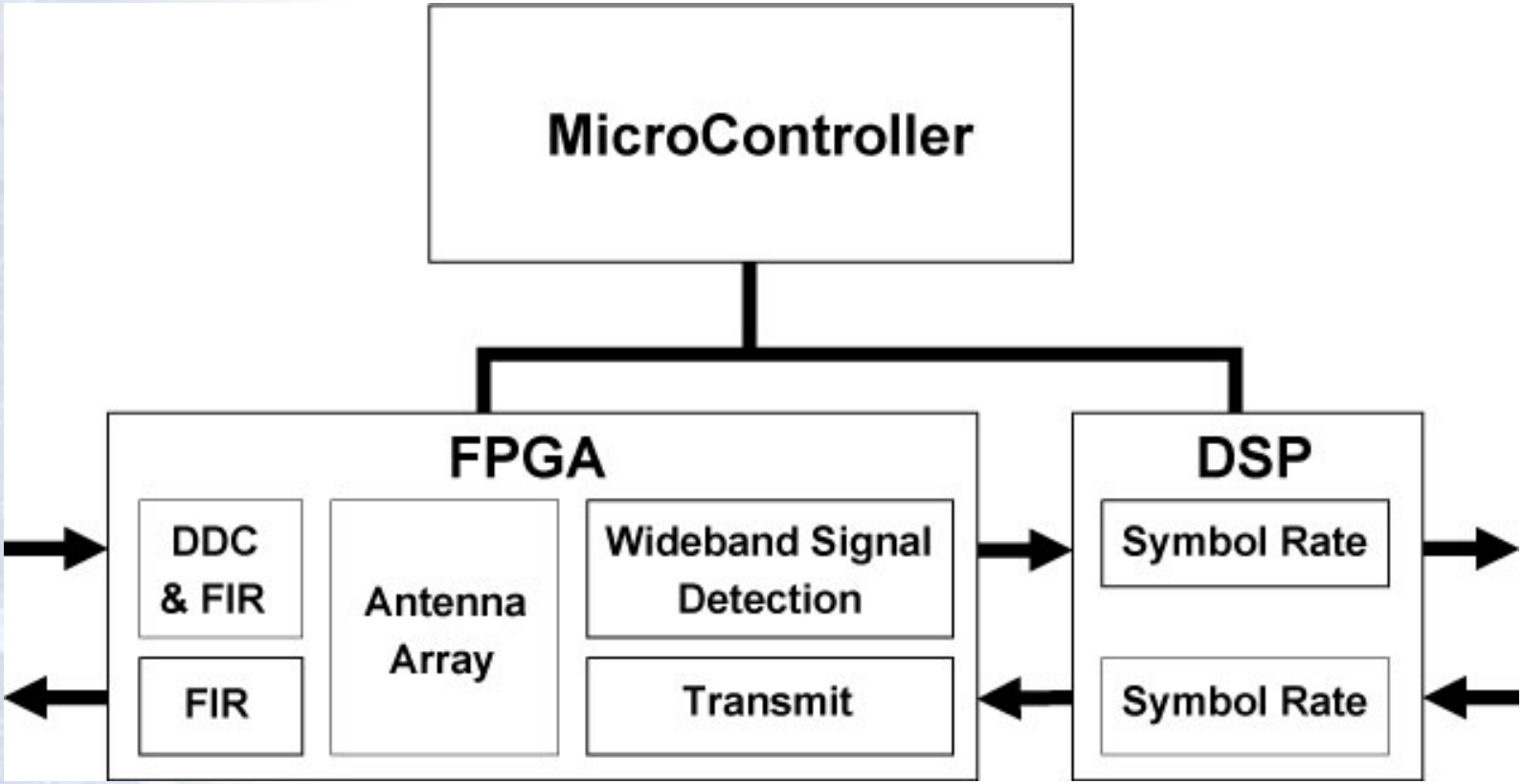
Exchange of complete radio modules or protocol layers

- Applicable across radio standards
  - GSM to EDGE to 3GPP to CDMA2000 to WIFI to ….
  - GSM-MAP to ANSI-41

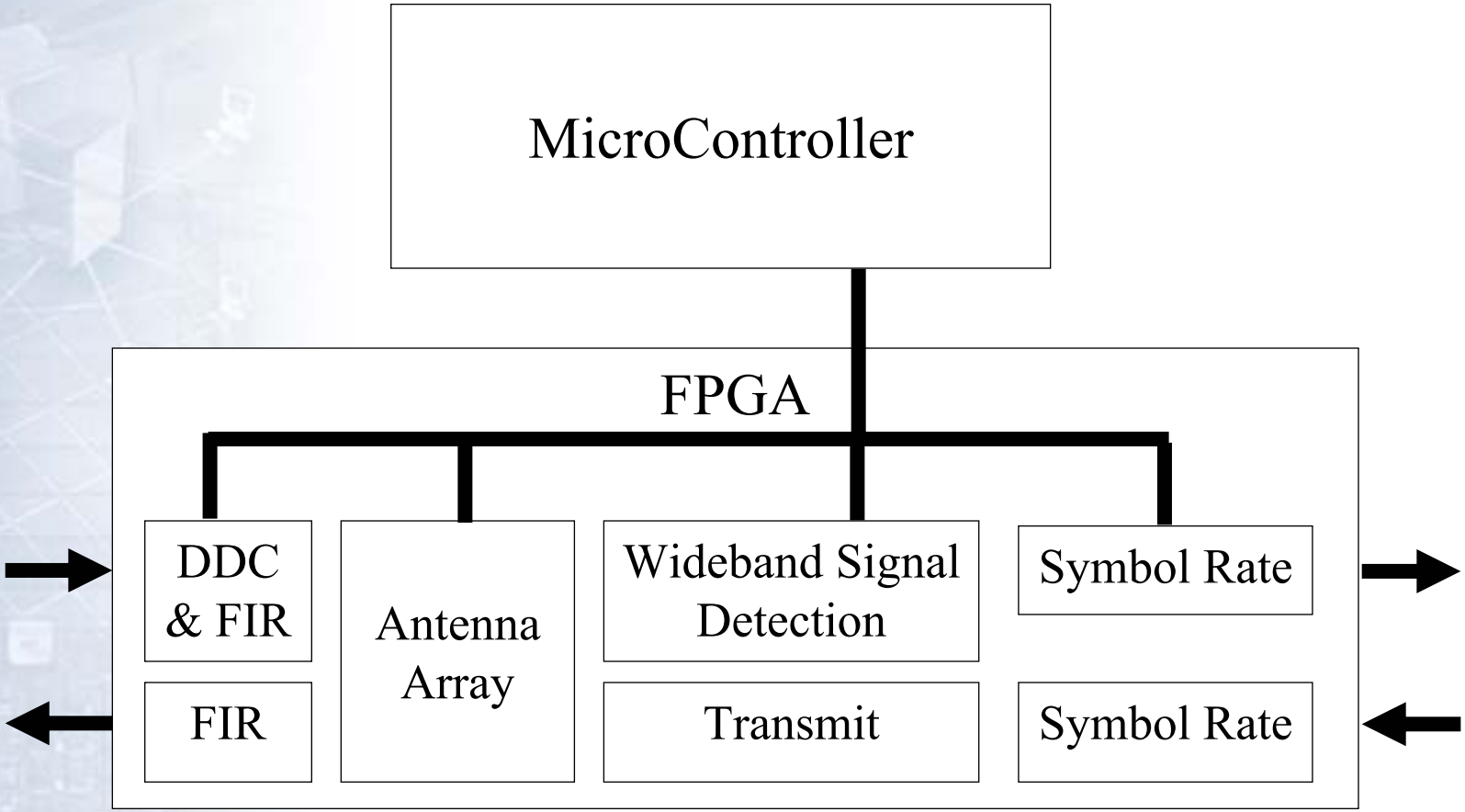
Narrowband System Partitioning



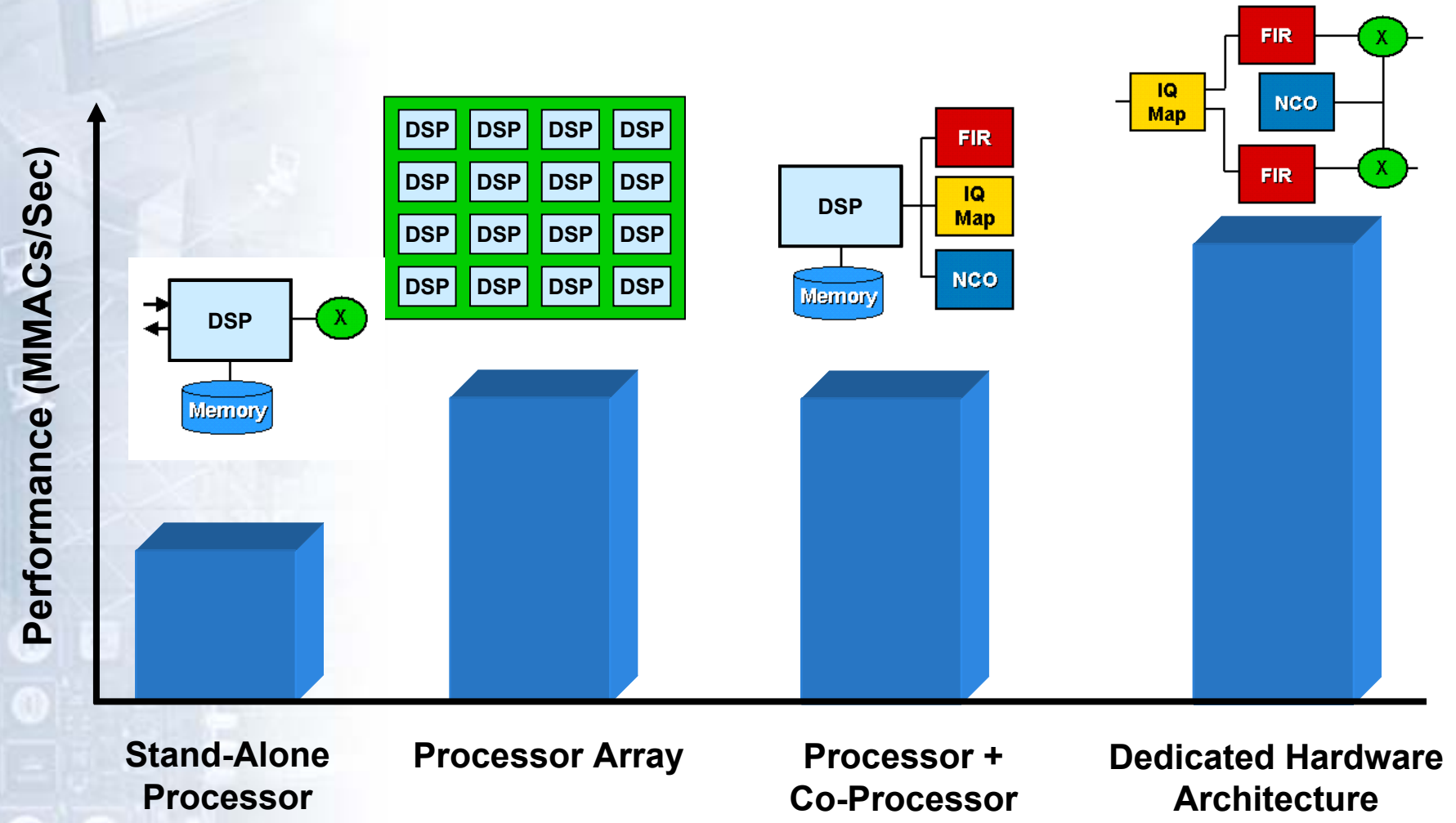
Wideband System Partitioning



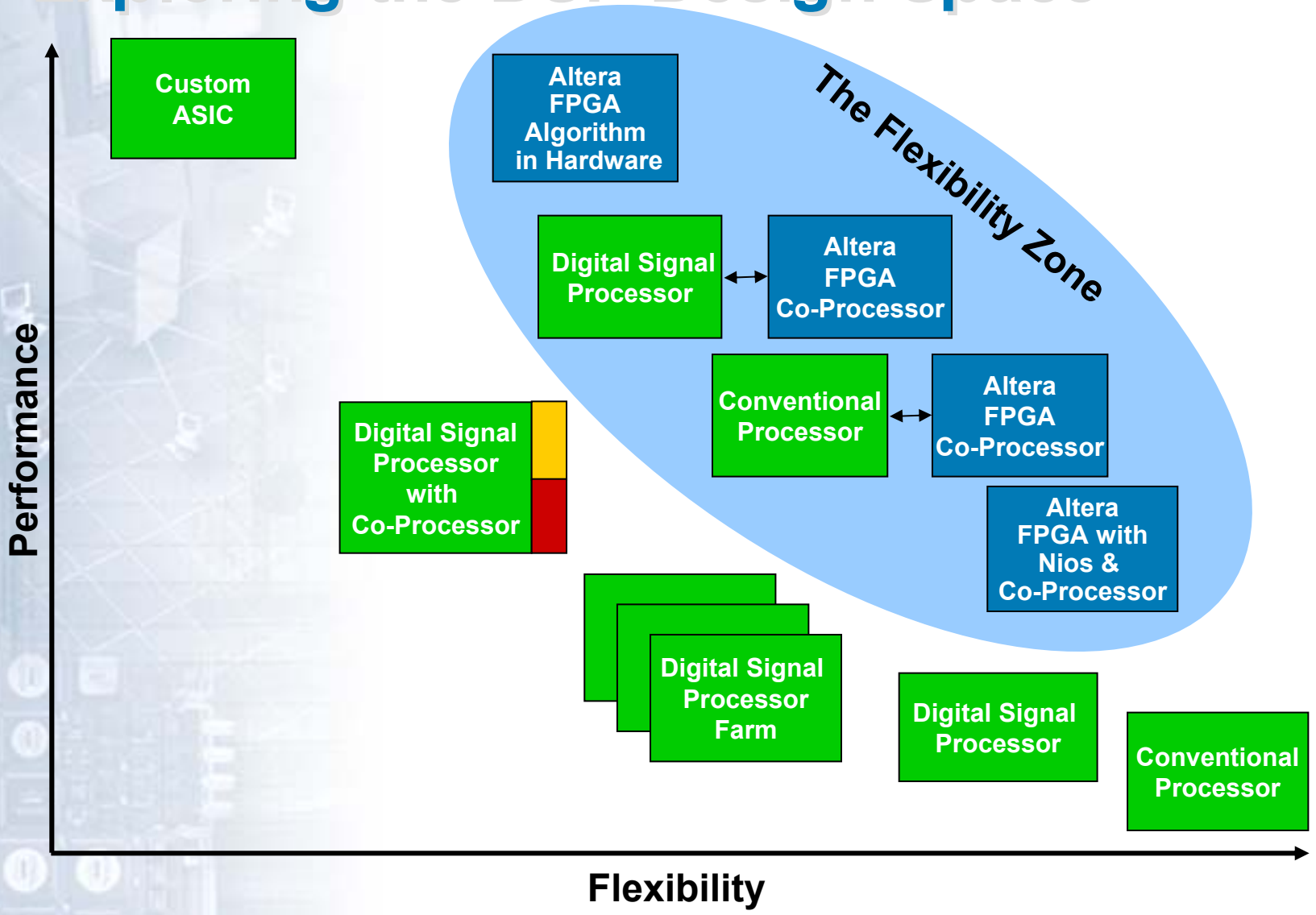
FPGA Based SDR Radio



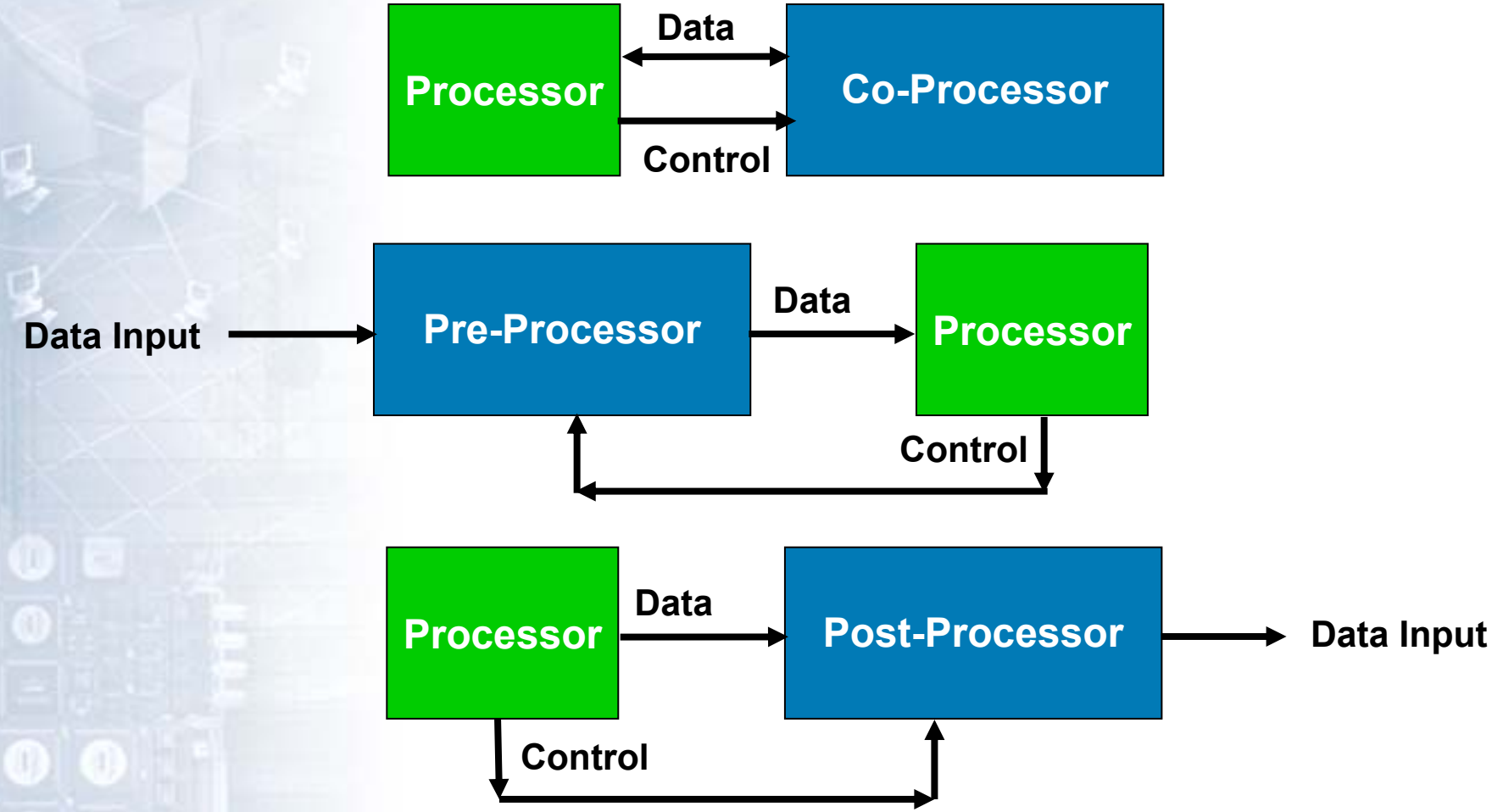
DSP System Architecture Options



Exploring the DSP Design Space

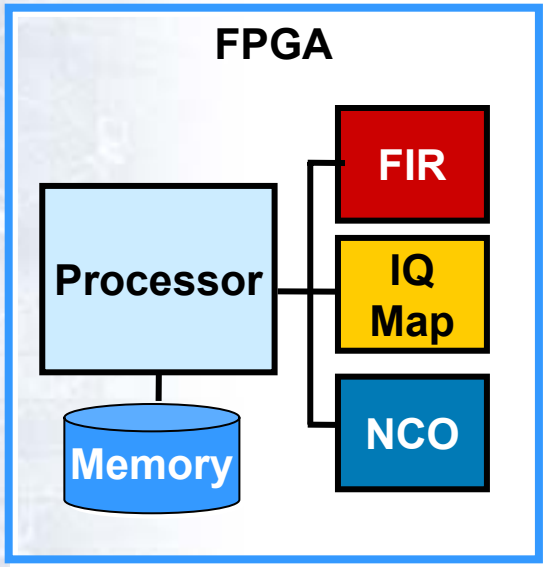


Co-Processing, Pre-Processing and Post-Processing

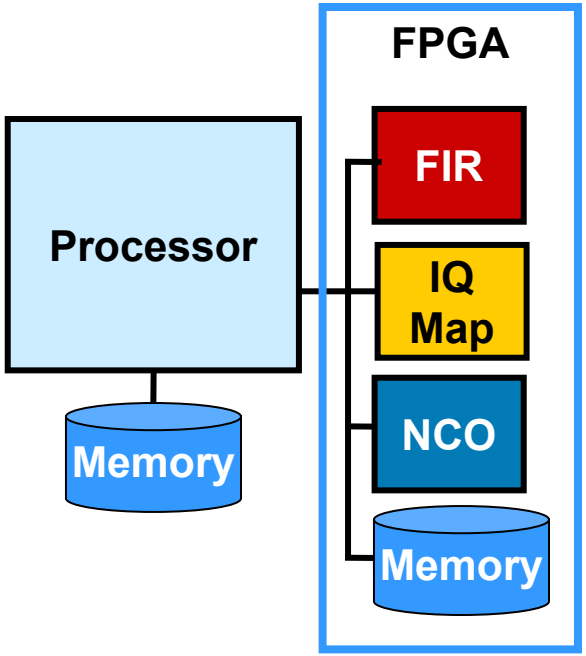


Co-Processing on FPGAs

Processor on FPGA

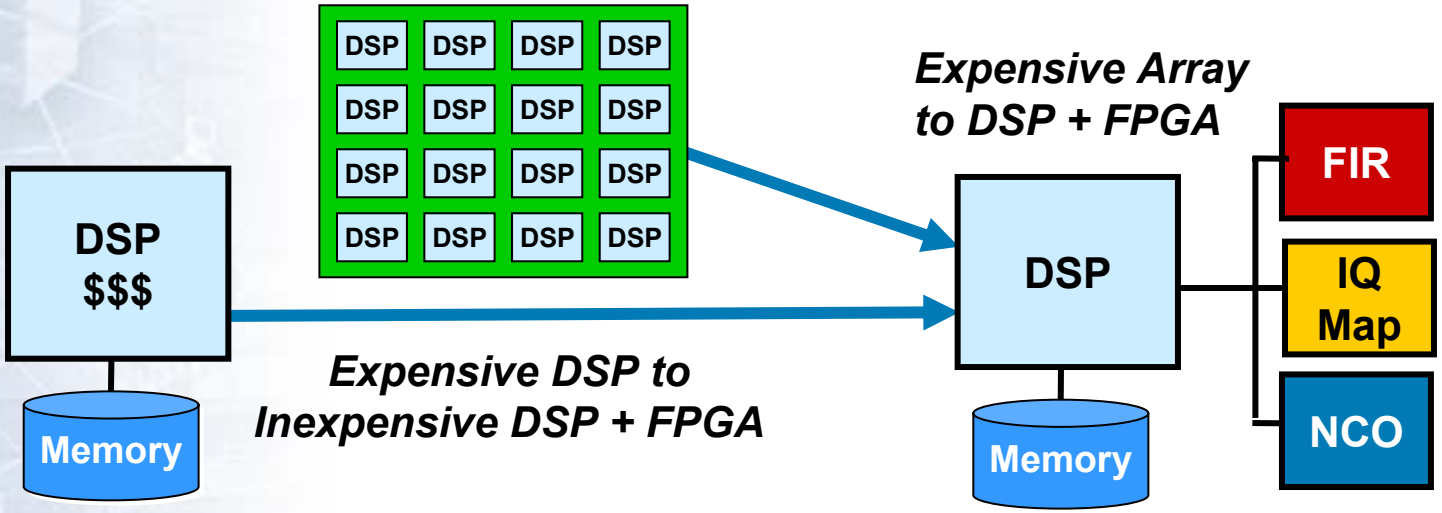


Processor External to FPGA



When Do FPGA Co-Processors Reduce System Cost?

- Off-Loading Algorithms to Co-Processor Reduces Number or Cost of Digital Signal Processors



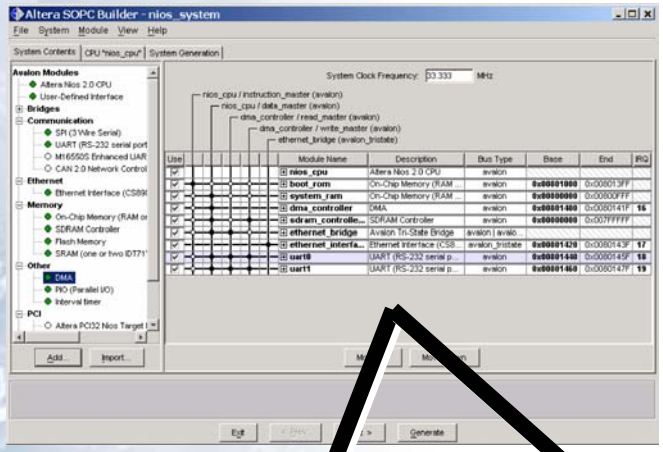
- Applications
  - Algorithms with Large Amount of Digital Signal Processing & Small Amount of Control Processing

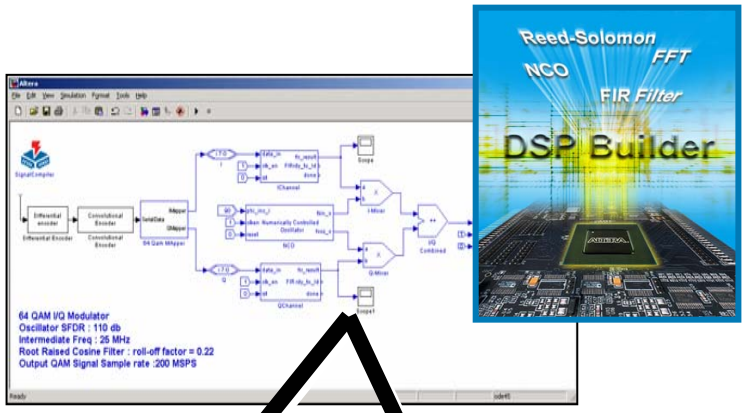
FPGA Co-processor Design Tools and IP

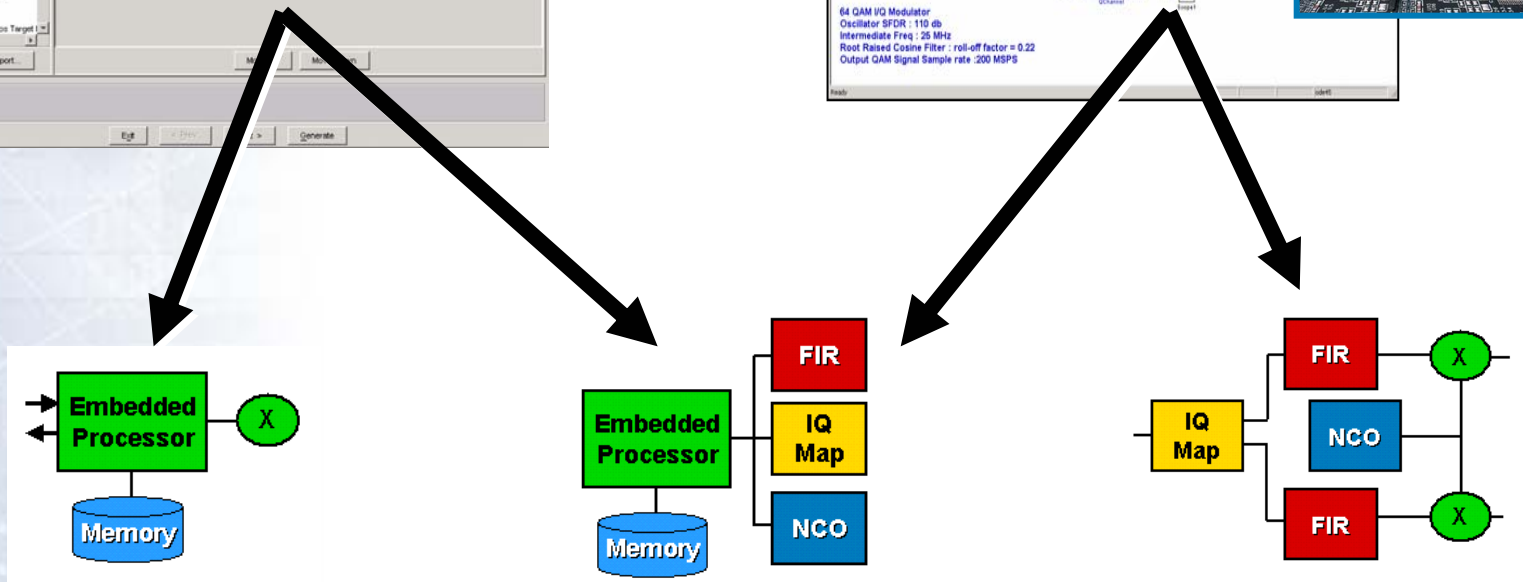
FPGA Co-Processor Design Tools

SOPC Builder

DSP Builder







Stand-alone Processor

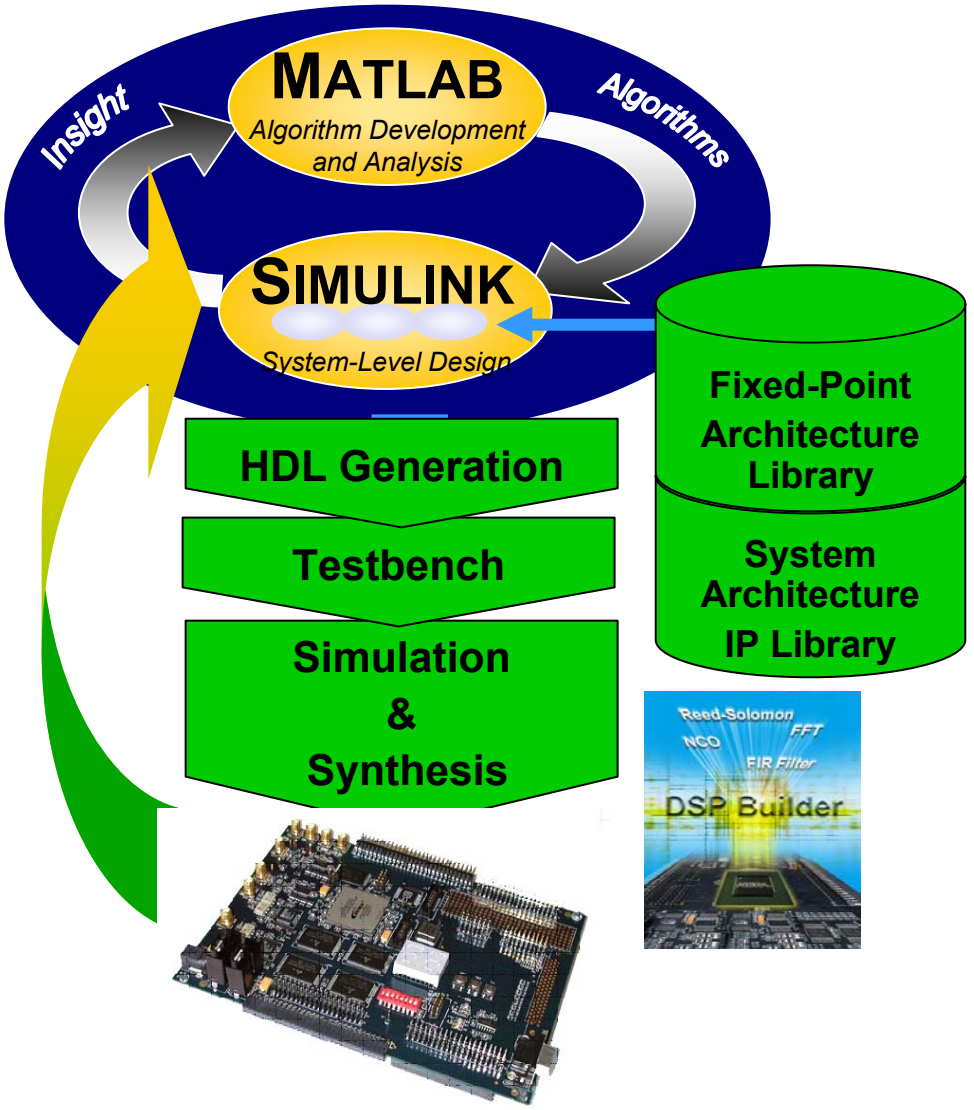
Processor + Co-Processor

Dedicated Hardware Architecture

DSP Builder

Altera® DSP Builder

- Fixed-Point Hardware Architecture Library
- System Architecture IP Library
- Automatic HDL Generation
- Automatic Testbench Generation
- Integrated Link to Altera Development Boards
- Real-Time Link from Development Board Back to Simulink
- Link to SOPC Builder and Nios Custom Instruction



Model Technology
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QUARTUS II

Synplicity

exemplar
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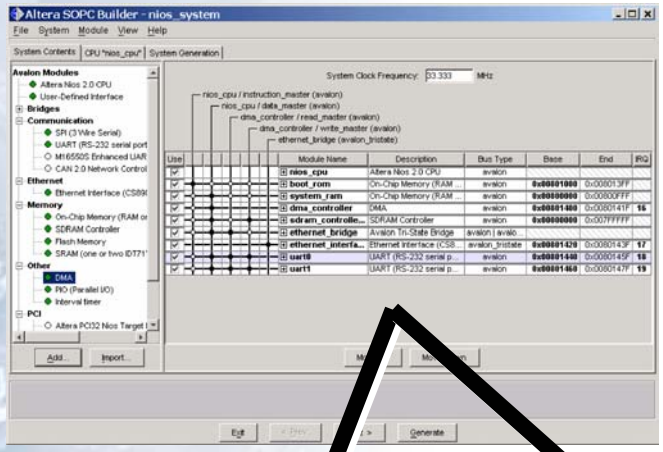
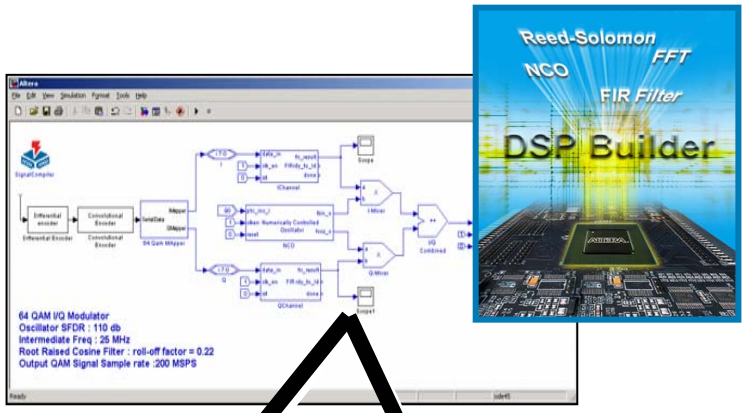
ALTERA®

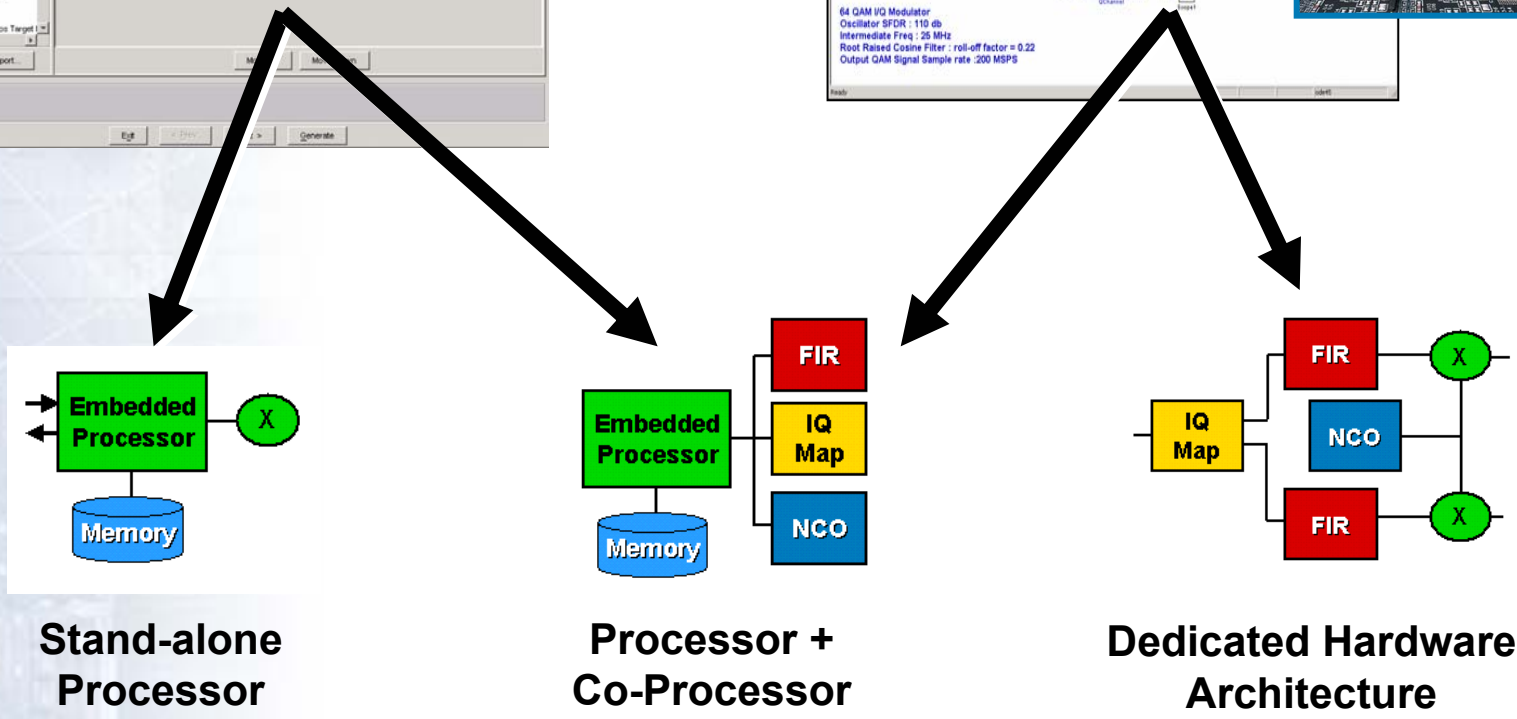
FPGA Co-Processor Design Tools

SOPC Builder

DSP Builder





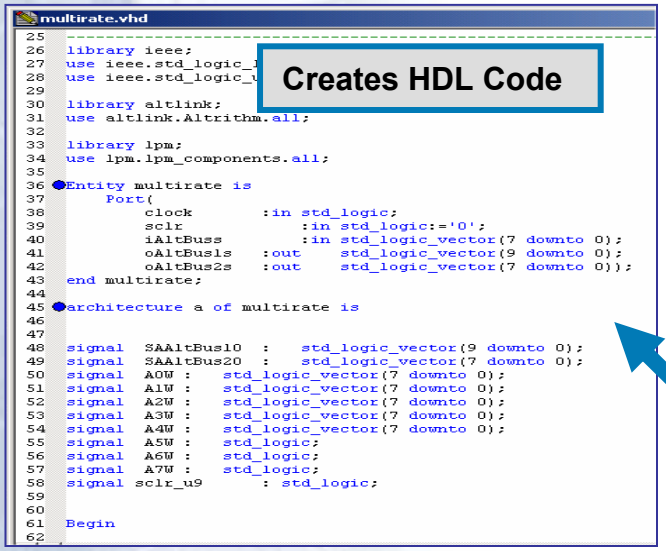


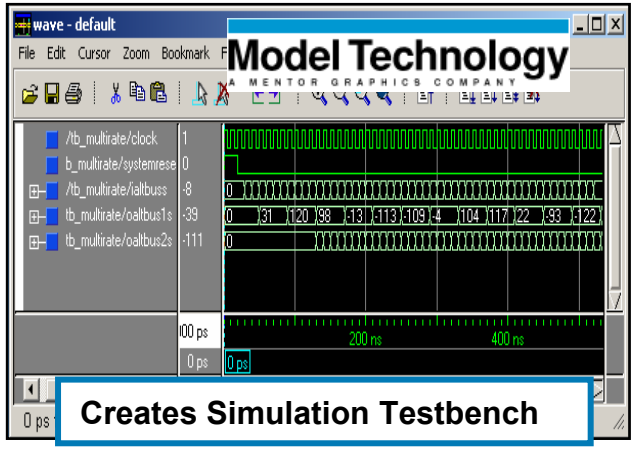
Stand-alone Processor

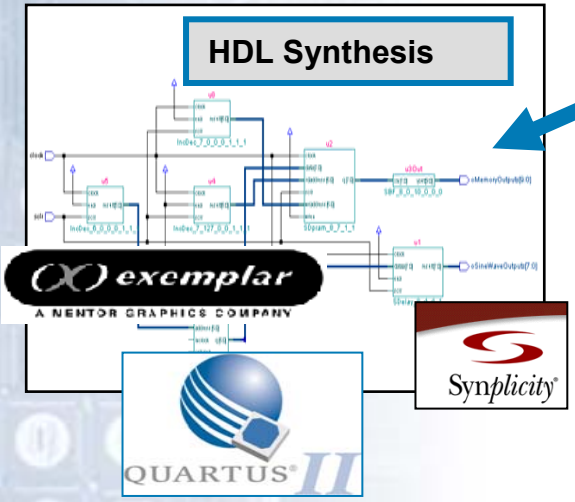
Processor + Co-Processor

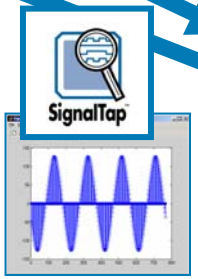
Dedicated Hardware Architecture

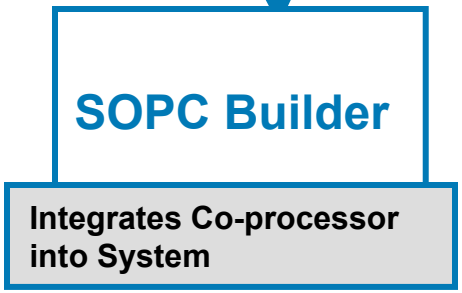
Datapath/Co-processor Design using DSP Builder





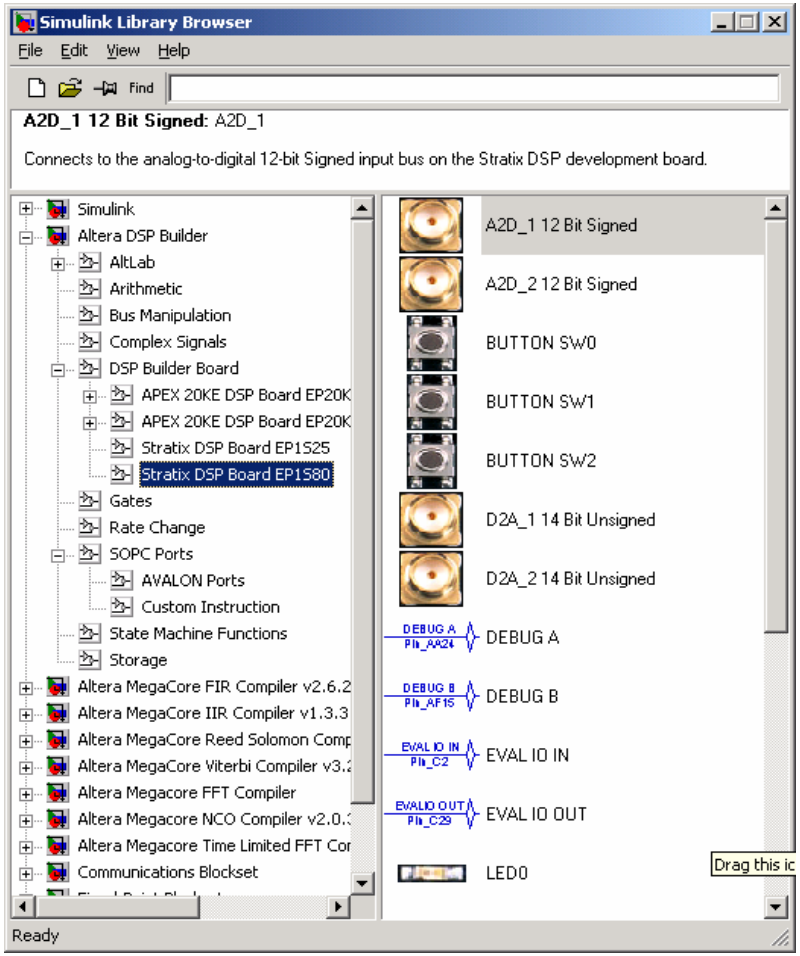




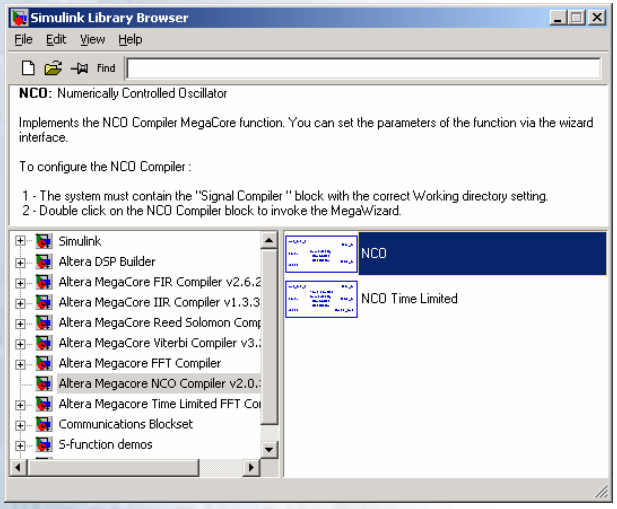


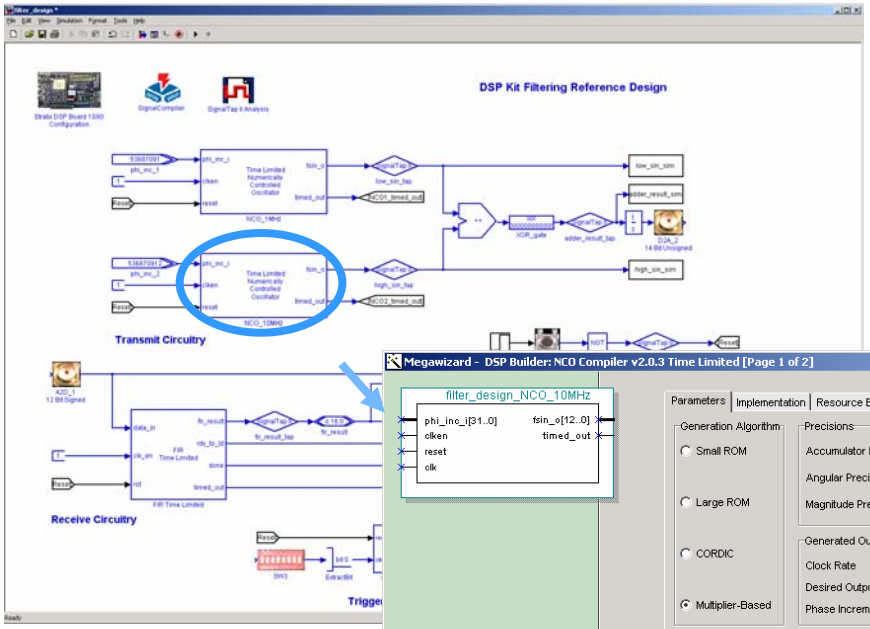
Library Components

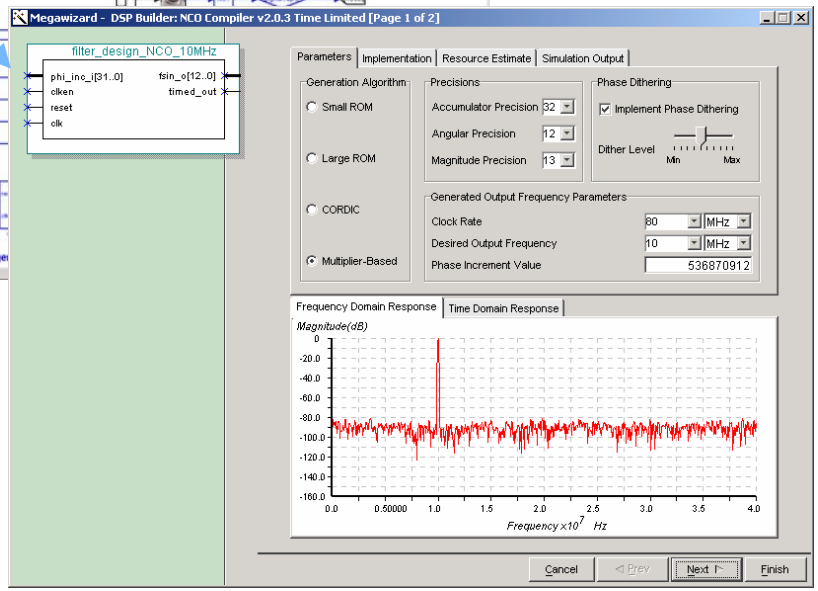
- Altera Library
- Arithmetic
- Bus Manipulation
- Complex Signals
- DSP Board
- Logical Components
- MegaCore IP
- Rate Change
- SOPC Ports
- State Machine
- Storage



IP MegaCore Functions



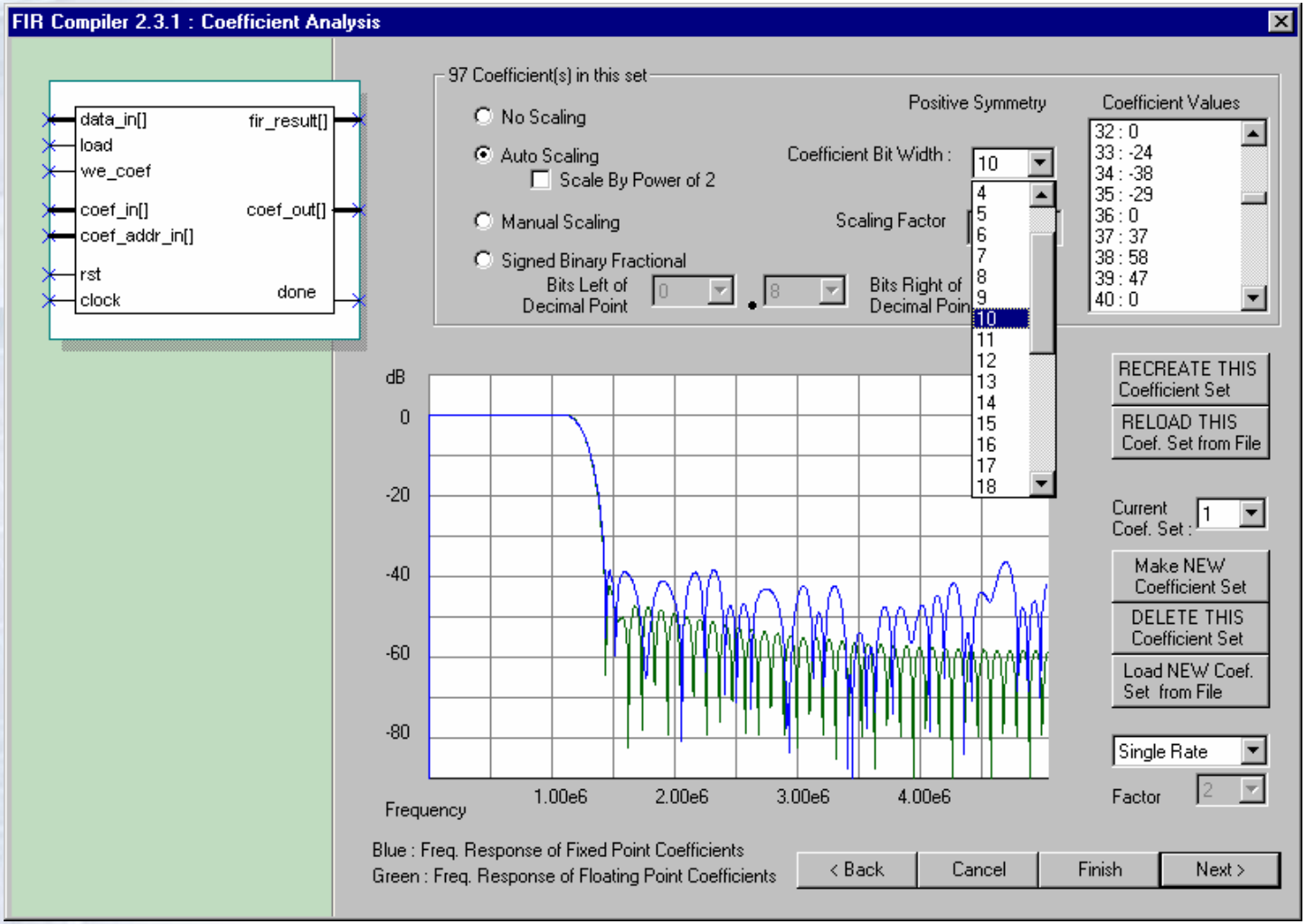




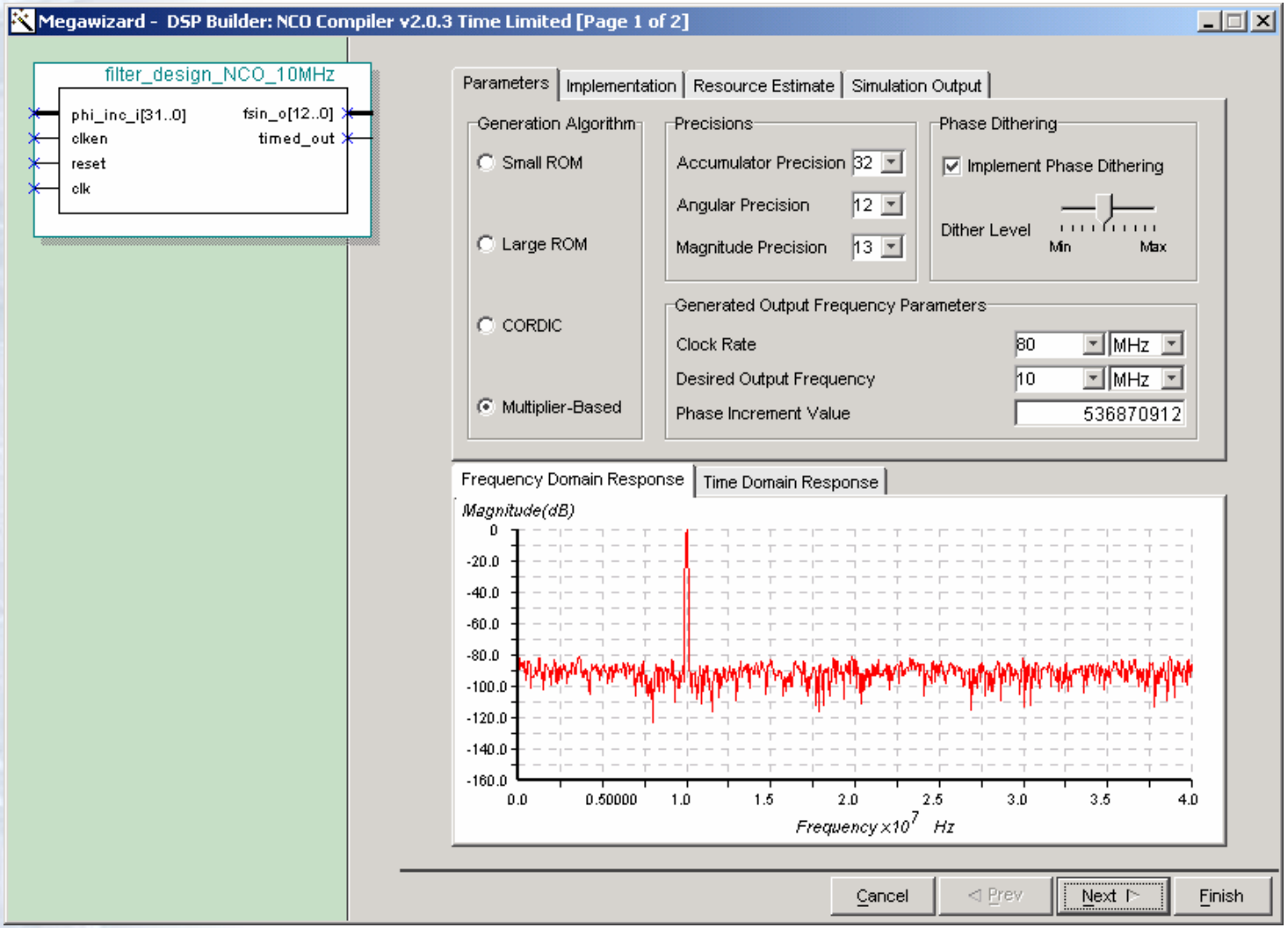
DSP Builder MegaCores

- FIR
- Reed Solomon
- Viterbi
- FFT
- NCO

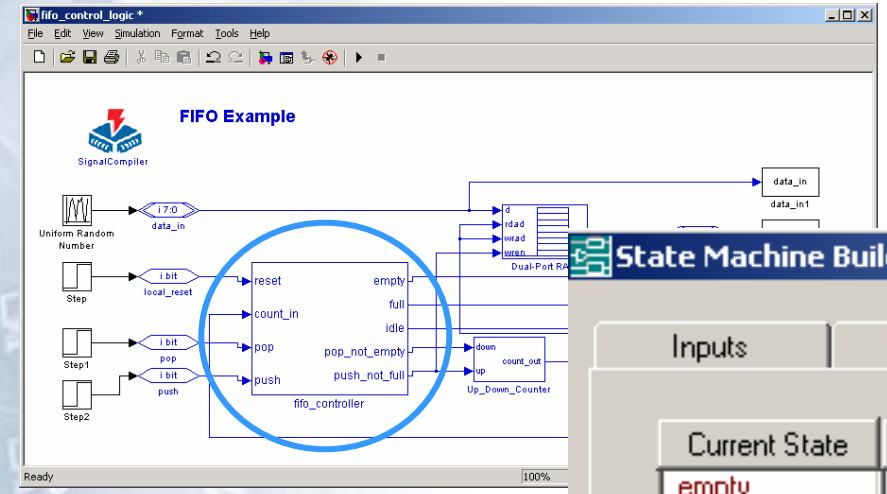
FIR MegaCore Function

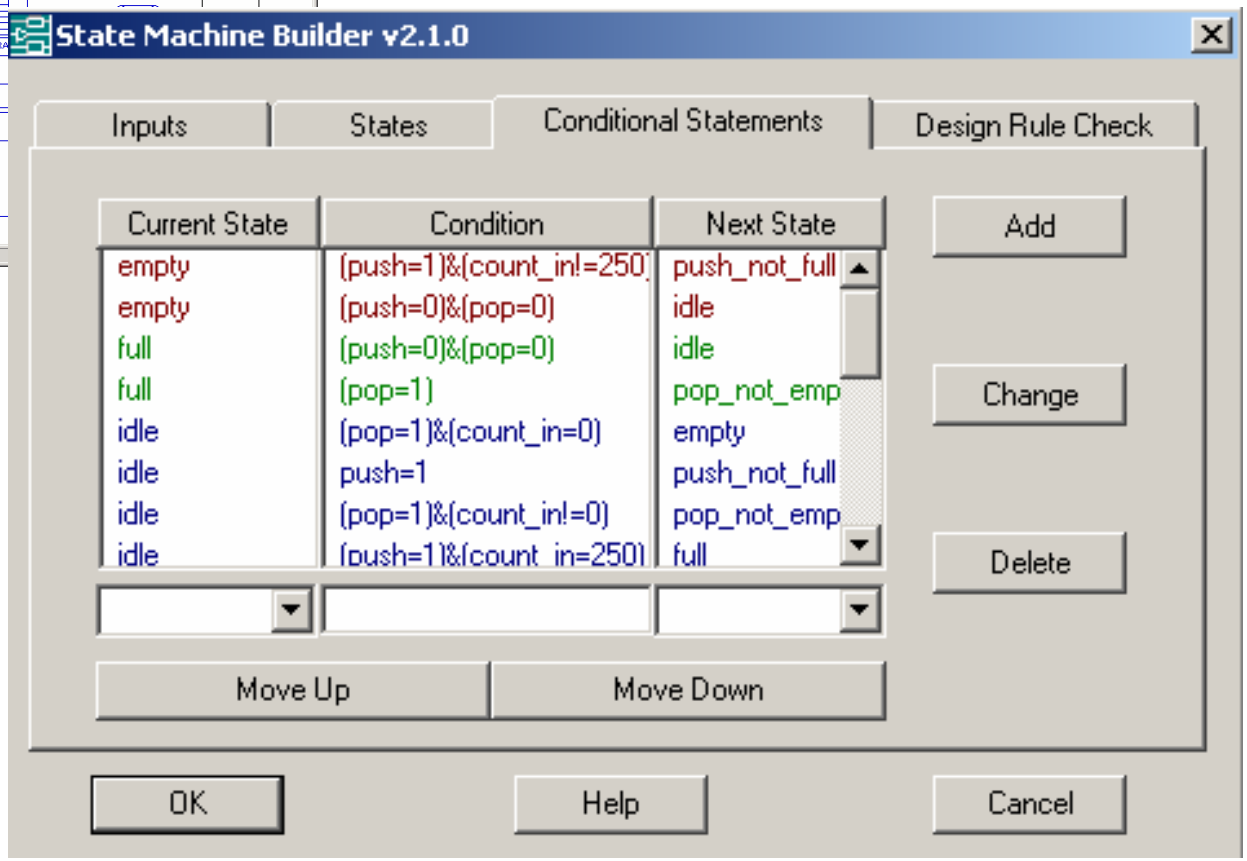


NCO MegaCore Function



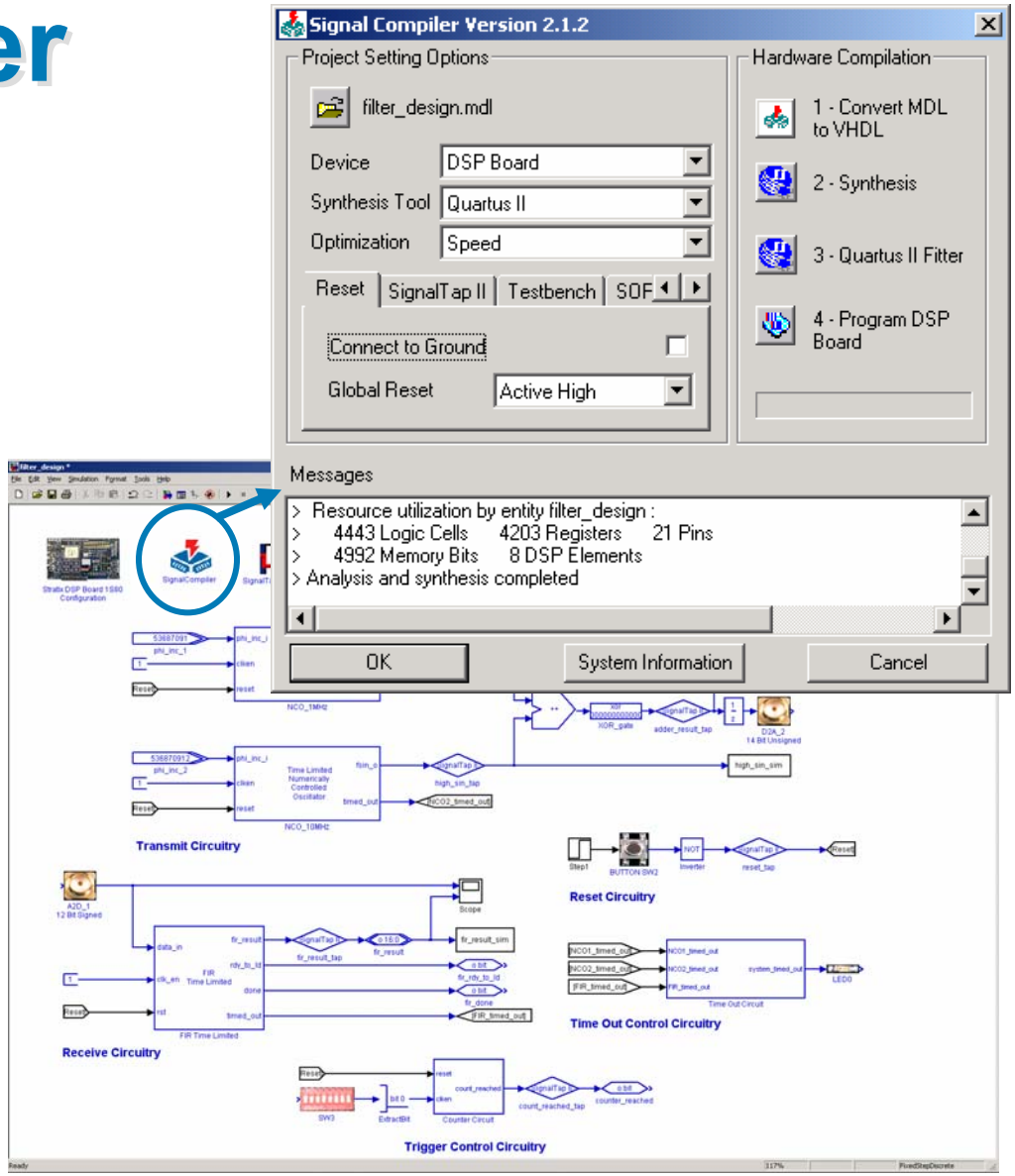
State Machine Builder





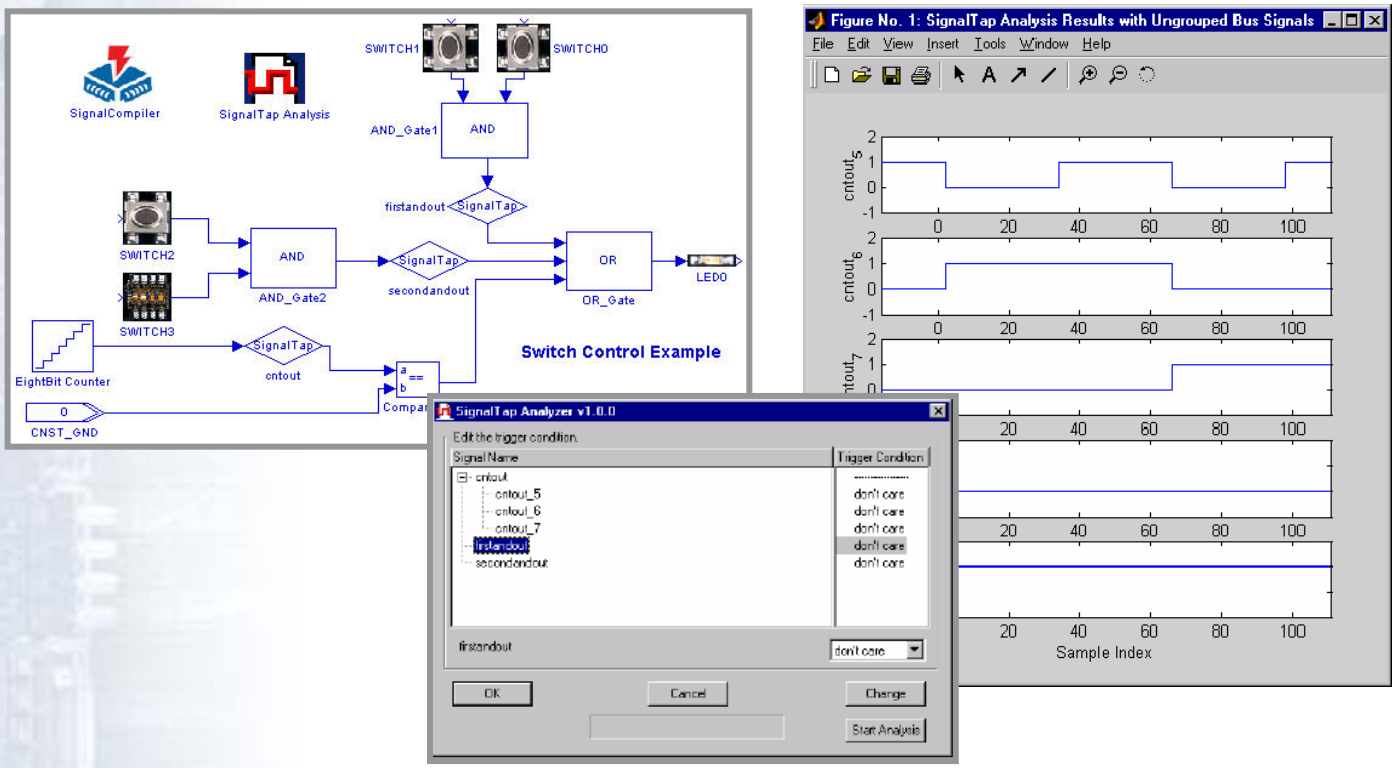
SignalCompiler

- Generates VHDL Design Files
- Generates Tool Command Language (TCL) Scripts
- Generates Testbench
- Enables Parameterization of IP Blocks
- Launch Hardware Compilation from the Simulink Cockpit



SignalTap II Logic Analyzer

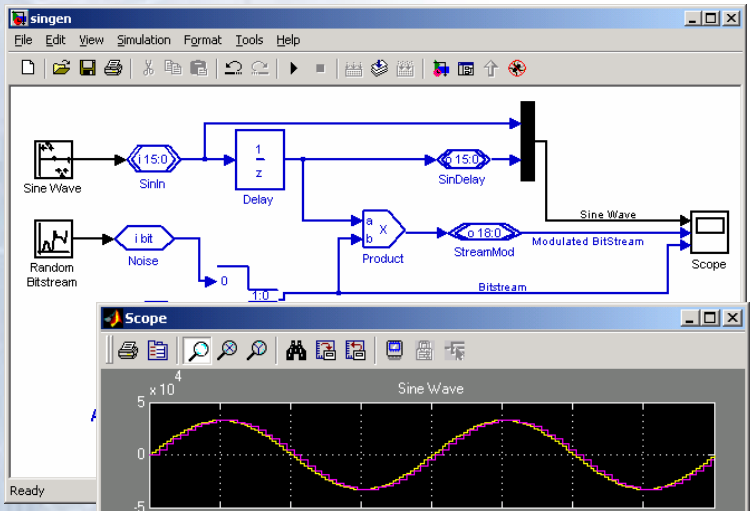
- Built-In SignalTap II Interface to DSP Builder
- Captures Signal Activity from Internal Device Nodes
- Displays Captured Data in MATLAB/Simulink

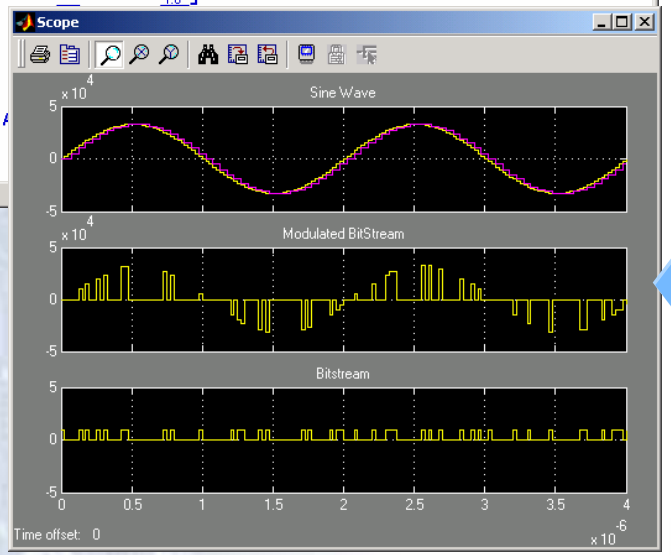


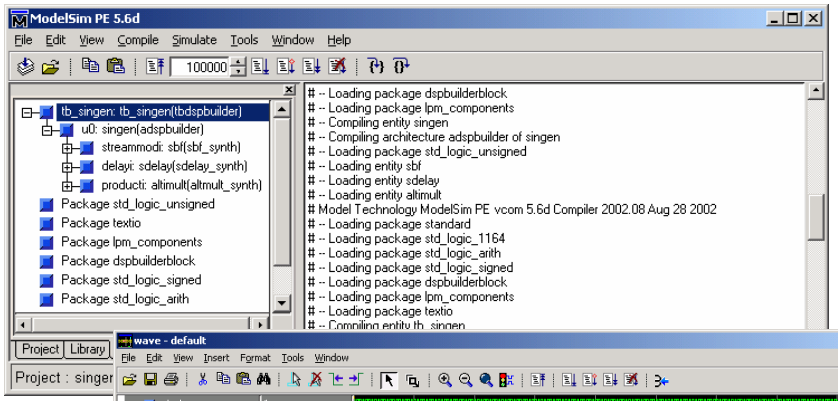
Automated Link to RTL Simulator

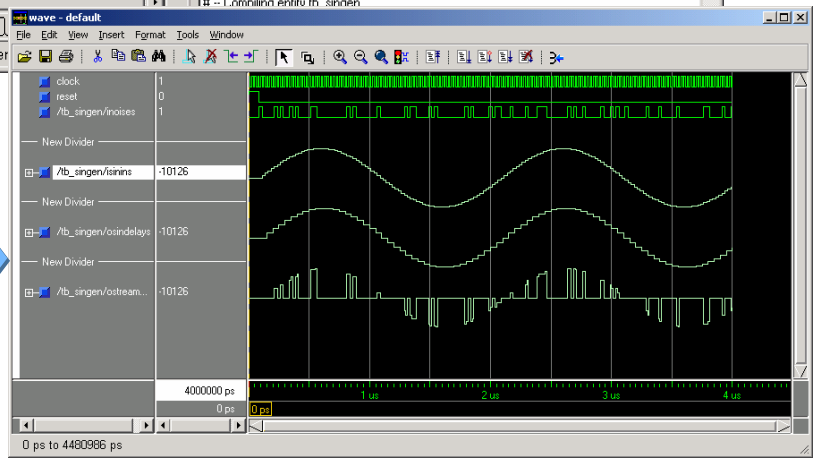
SIMULINK Domain

ModelSim Domain







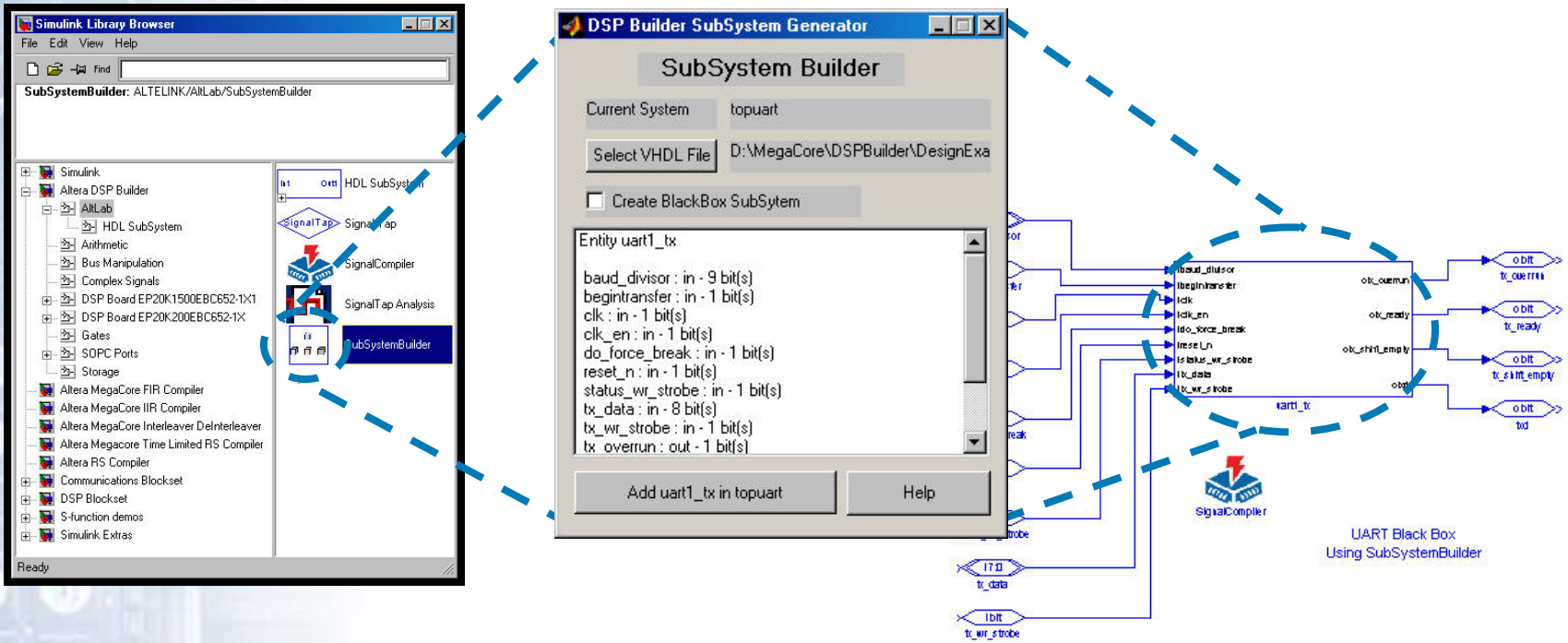


Compare

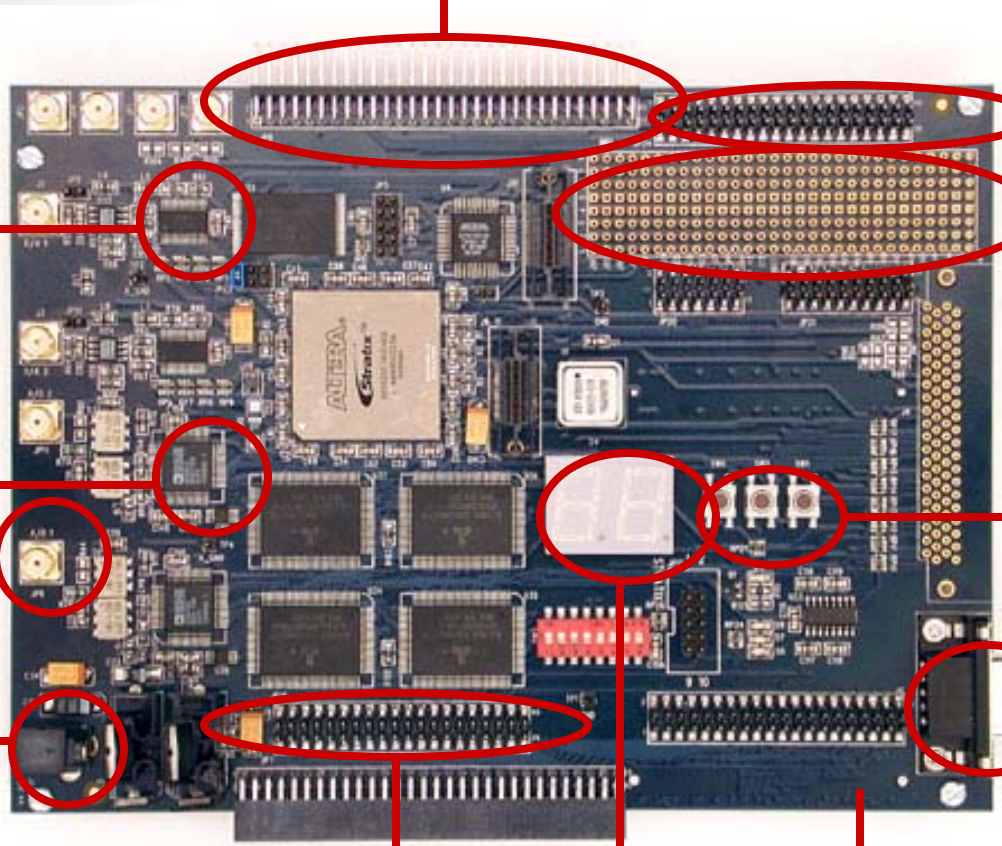
SignalCompiler

Sub-System Builder

- Import Existing VHDL Design into Simulink
- Simulink Simulation Options
  - Convert into DSP Builder Blocks or MATLAB Functions
  - Treat VHDL Design as Black Box



Stratix 1S25/1S80 DSP Development Board



80-pin I/O Connector

Altera Nios Expansion Prototype Connector

14-bit, 165 Mhz D/A

Prototyping Area

12-bit, 125 Mhz A/D

Push Button Switches

SMA Connector

5V Power Supply

9-pin RS232 Connector

40-pin Connector For Analog Devices Evaluation Boards

LEDs

Texas Instruments Connectors can be found on the underside of the board

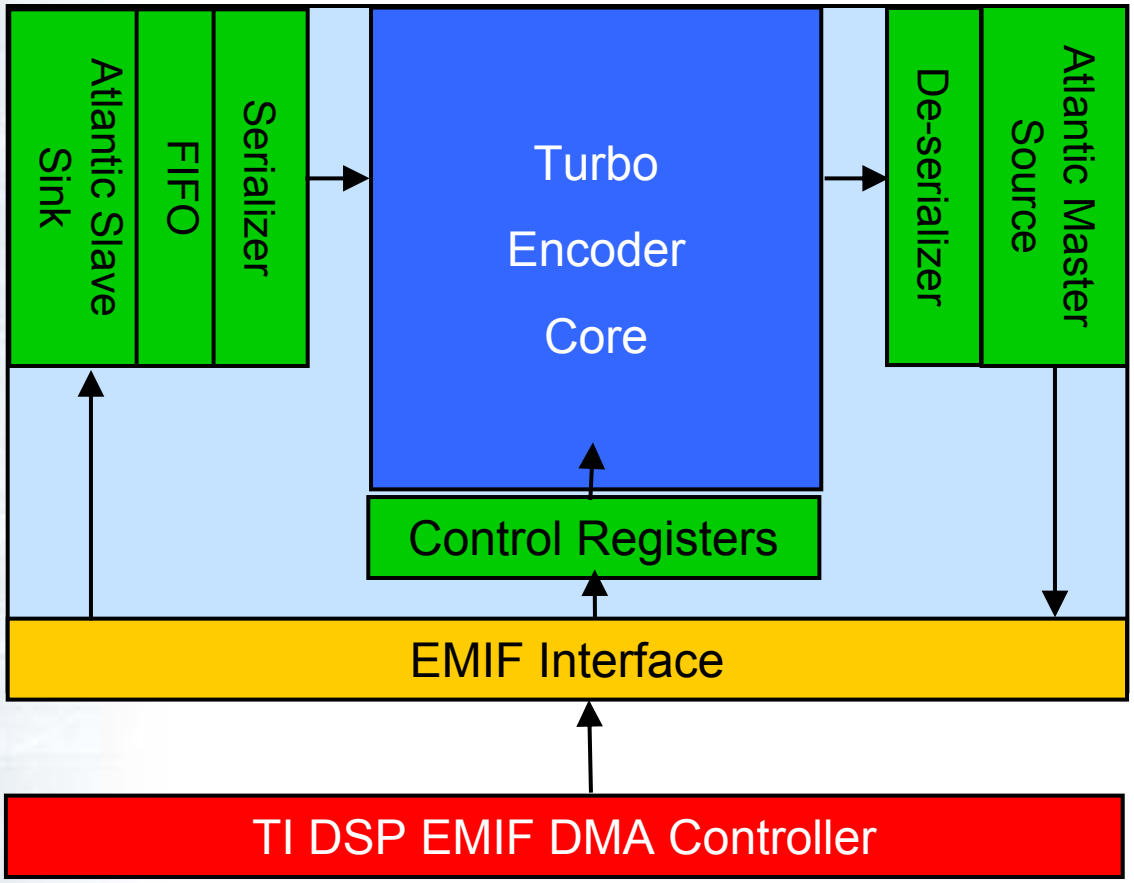
FPGA Co-processor Reference Design

Turbo Encoder for HSDPA

Turbo Encoder Co-processor Reference Design (TI Solution)

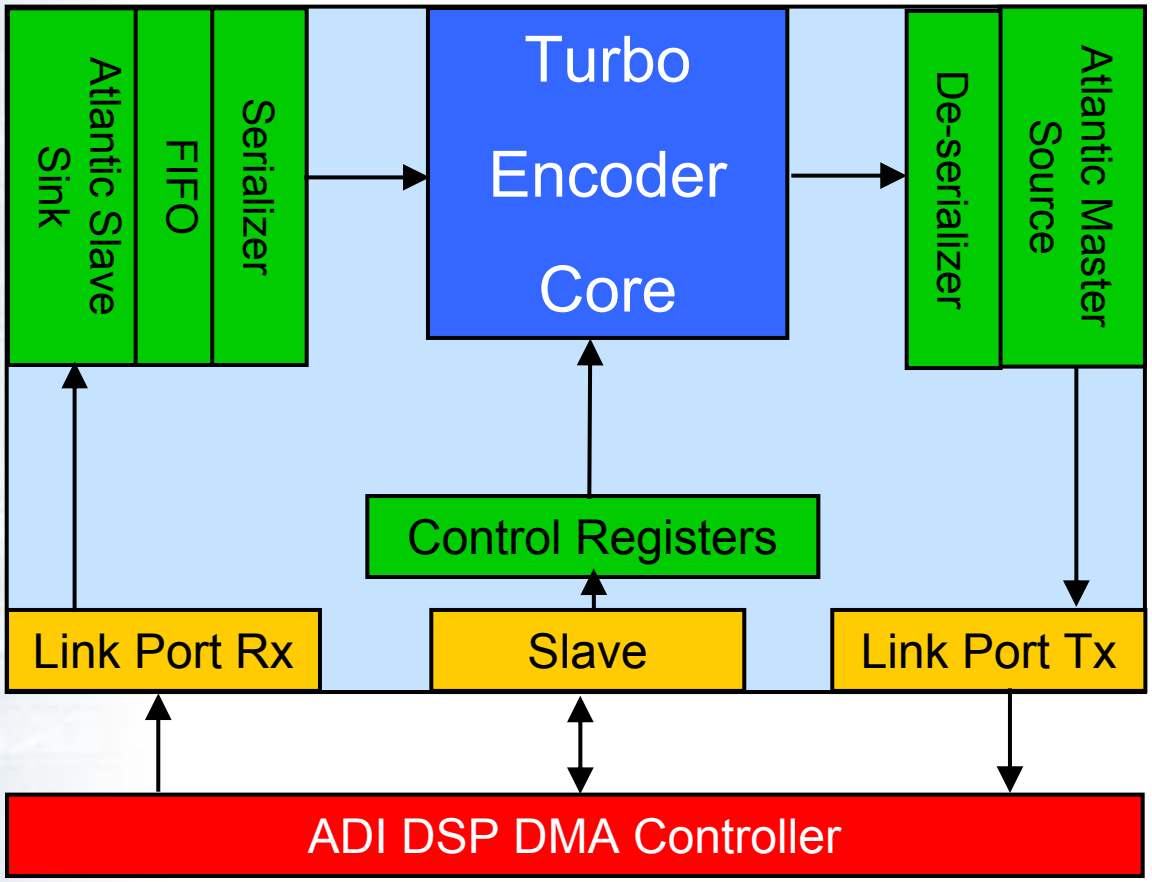
- Interface to TI DSP EMIF (External Memory Interface)
  - Other processor interfaces in development
- Uses DSP Processor's on-chip DMA
- Wrapper for Turbo Encoder MegaCore
  - Can select a different configuration (e.g. block size) for each data packet/block
- Software Libraries

Turbo Co-processor Block Diagram (TI Solution)



Turbo Core Wrapper

Turbo Co-processor Block Diagram (ADI Solution)



Turbo Core Wrapper

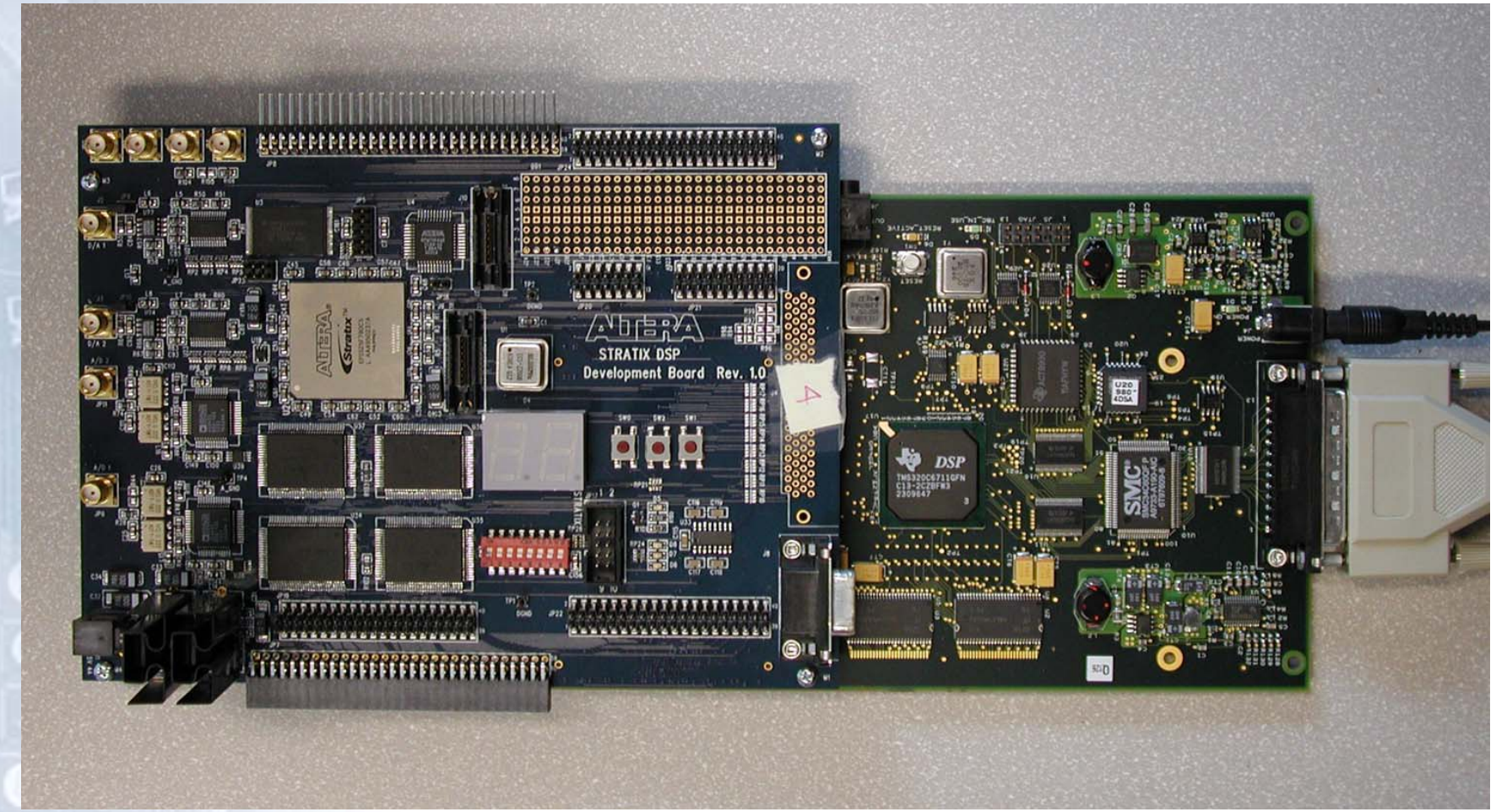
Data Buffering

- FIFOs in Atlantic slave sink store EMIF 64 byte bursts whilst being serialised into core
- Slave sink in receive converter has similar FIFO
- FIFOs introduce latency but
  - throughput is maintained
  - System bus not tied up during serialization/deserialization

TI Development Environment

- Stratix DSP Development Board plugs into EMIF slots of TI 6713 DSK (DSP Starter Kit)
- Limited to Asynchronous EMIF interface due to design of TI card
  - Customer designs may use synchronous Interface

TI Development Hardware



Software Environment

- Running on TI DSP
- Uses EDMA controller to transfer data
  - To and from accelerator
- Asynchronous, streaming, interface
  - Callback when packet is complete
  - Can submit 2nd packet before 1st is done
    - Callbacks occur in order

Header file

```
typedef void (* TXCALLBACK)(
    void * handle);
typedef void (* RXCALLBACK)(
    uchar * data,
    void * handle);
void turbo_encode(
    const uchar * data,
    uchar * output,
    uint bits,
    TXCALLBACK txcallback,
    RXCALLBACK rxcallback,
    void * handle);
```

Using the accelerator

- Call function for each packet
  - Packets can have any block size
- Data is sent to encoder
  - Queued if accelerator is already busy
- txcallback called when data has been sent
- rxcallback is called once results available
- Interface can be changed if desired

Cost Analysis Example (1)

14.4Mbits/s Turbo Encoder

Cyclone: $10.75

- 2600 LE equivalent cost Based on EP1C3T100C8 1k units (July 2003)

TI C64 DSP: $33.00

- 136/600 MHz based on 9.7cycles/bit (Source: TI)
- C6416/600MHz @ $145 1kunit pricing (Source: TI)

Cost Analysis Example (2)

58Mbits/s Turbo Encoder

Cyclone: $21.58

- 2600 LE equivalent cost Based on EP1C3T100C6 1k units (July 2003)

TI C64 DSP: $136.00

- 563/600 MHz based on 9.7cycles/bit (Source: TI)
- C6416/600MHz @ $145 1kunit pricing (Source: TI)

TI Reference Design Summary

- Contents
  - Turbo Encoder MegaCore (OpenCore)
  - TI EMIF Interface
  - Wrapper
  - DSP Software Libraries
- Expected Availability
  - September 2003

ADI Reference Design Summary

- Contents
  - Turbo Encoder MegaCore (OpenCore)
  - ADI Link Port Interface
  - Wrapper
  - DSP Software Libraries
- Expected Availability
  - Q1 2004

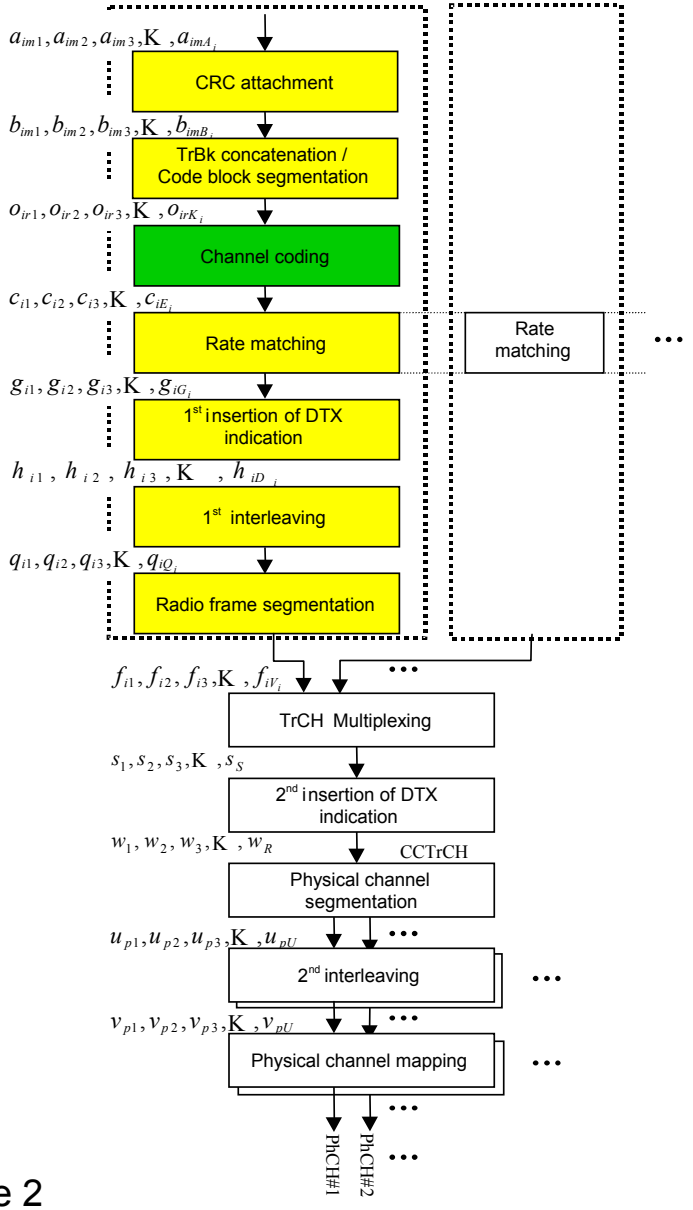
Future HSDPA Functionality

Currently implemented:

- Channel coding

Future additions:

- CRC attachment
- Rate Matching
- DTX generation
- Interleaving

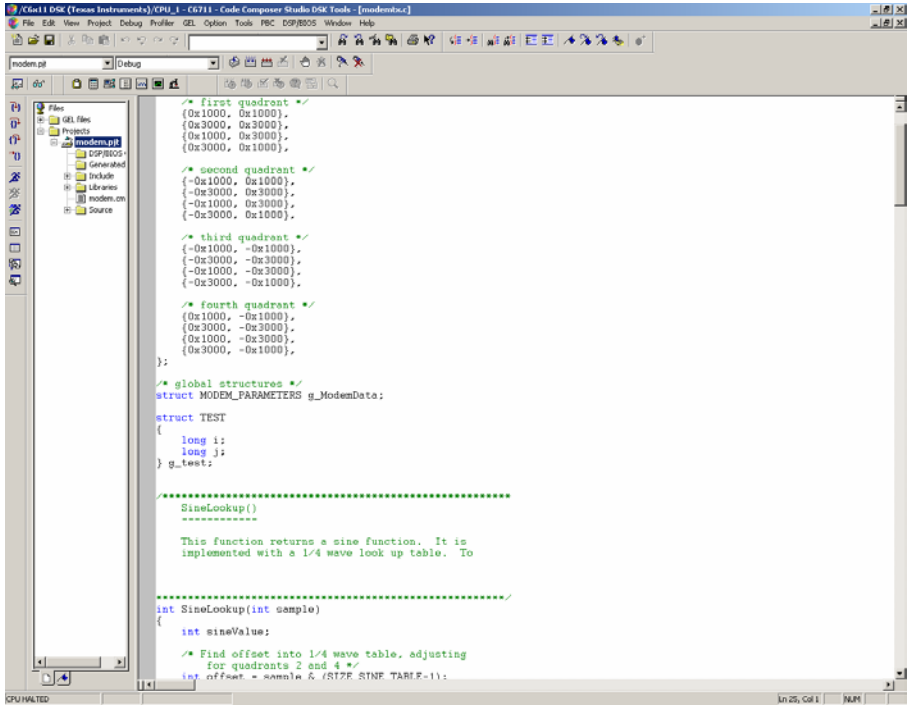


Source: 3GPP TS 25.212 V5.3.0 (2002-12), page 12, figure 2

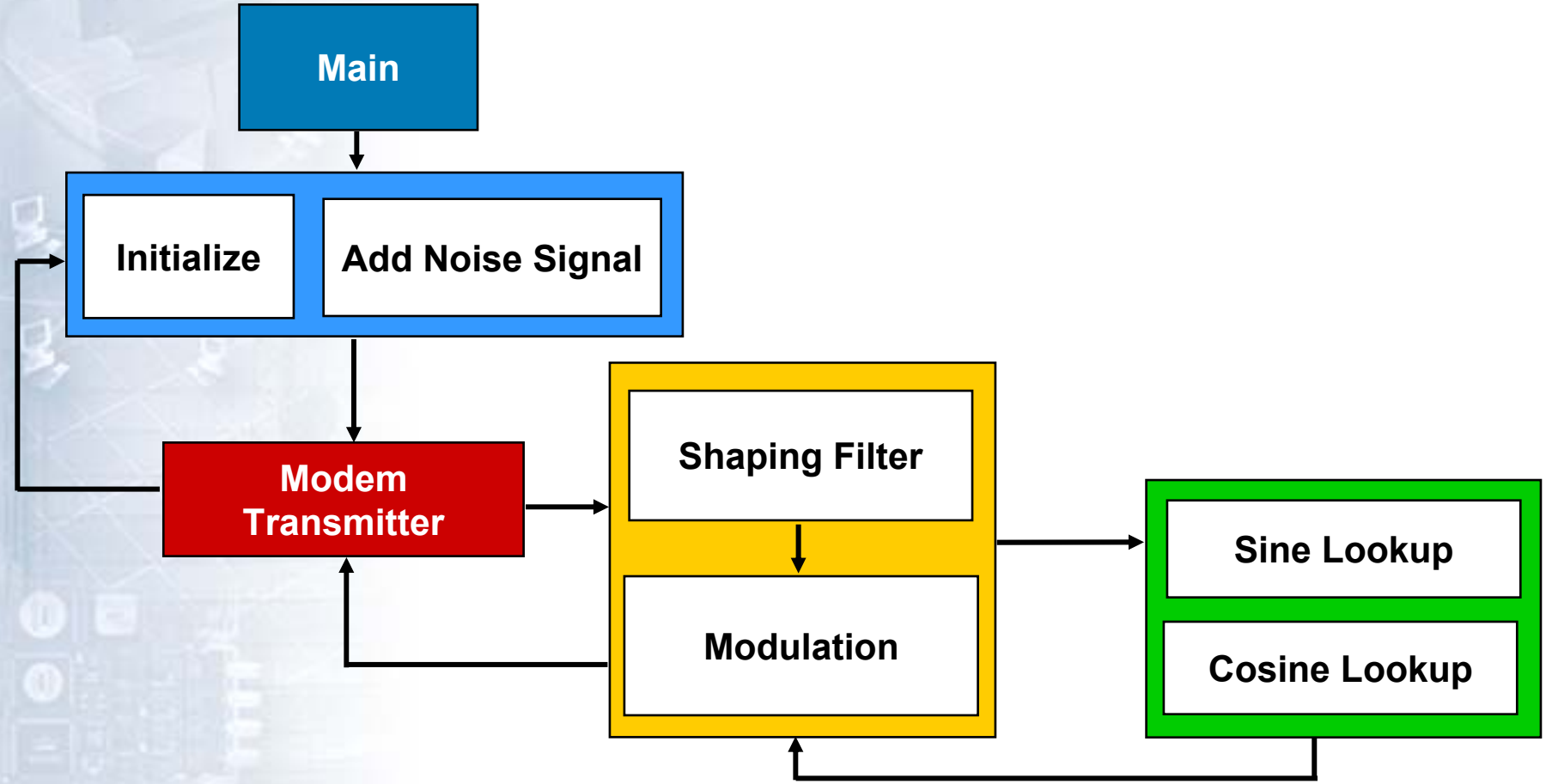
QAM Modulator Co-Processor Design Example

Modem Reference Design

- Installed with Code Composer Studio As a Tutorial
  - C:\ti\tutorial\dsk6711\modem
- Used to Demonstrate CCS Functionality
- 16 QAM TX Modem

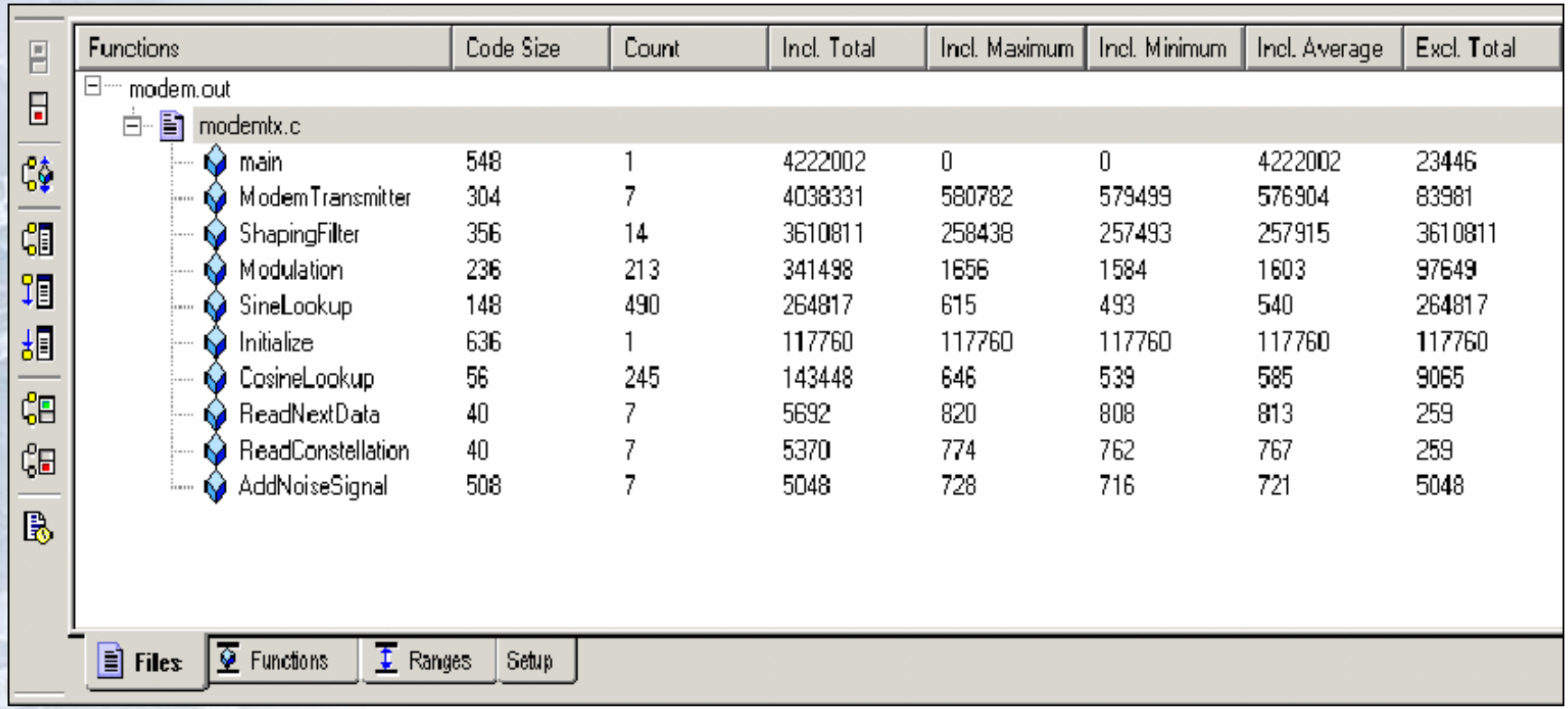


Modem Design Overview



Modem Design Code Profile

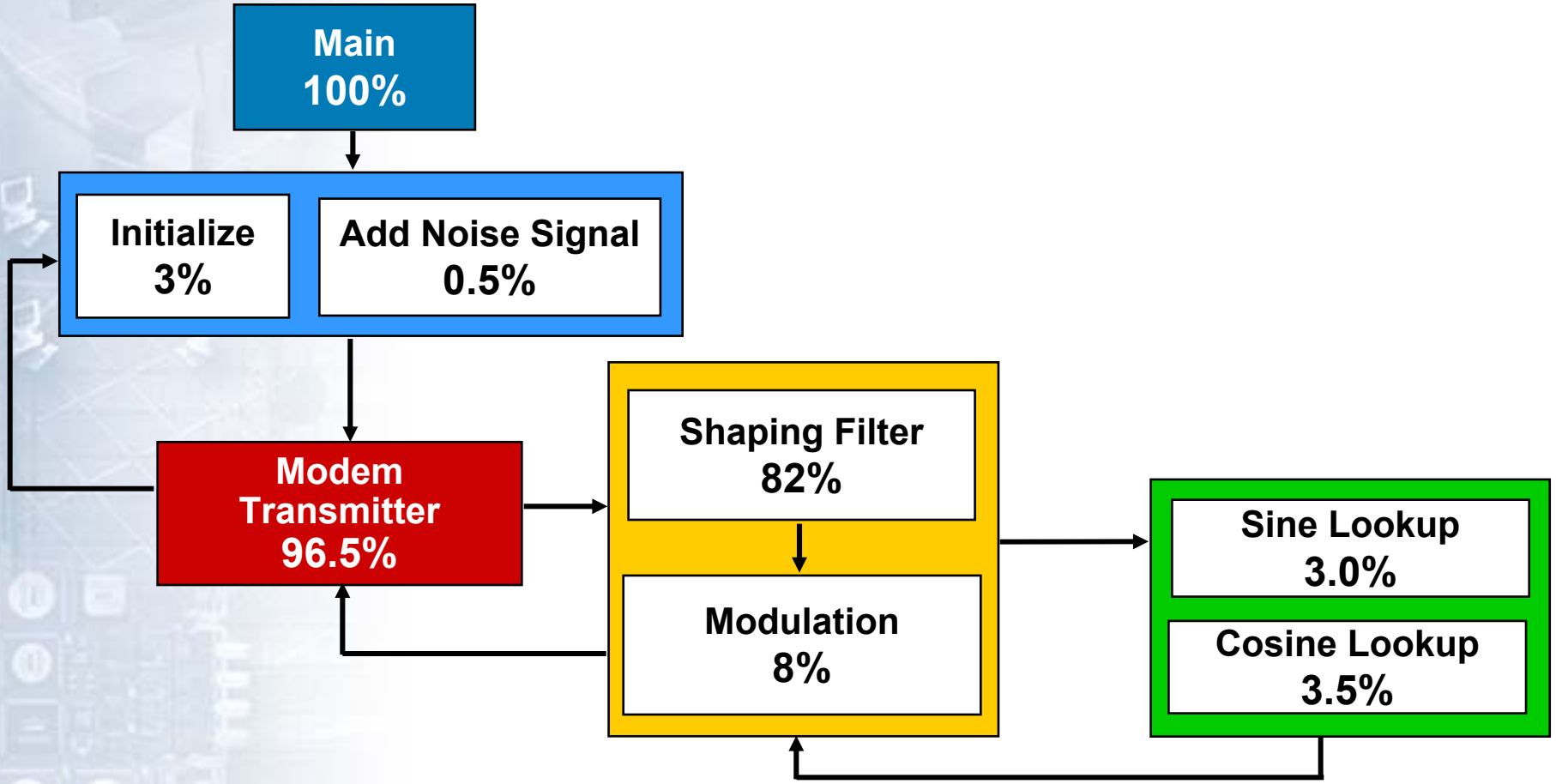
TI Code Composer Studio Profiling Output



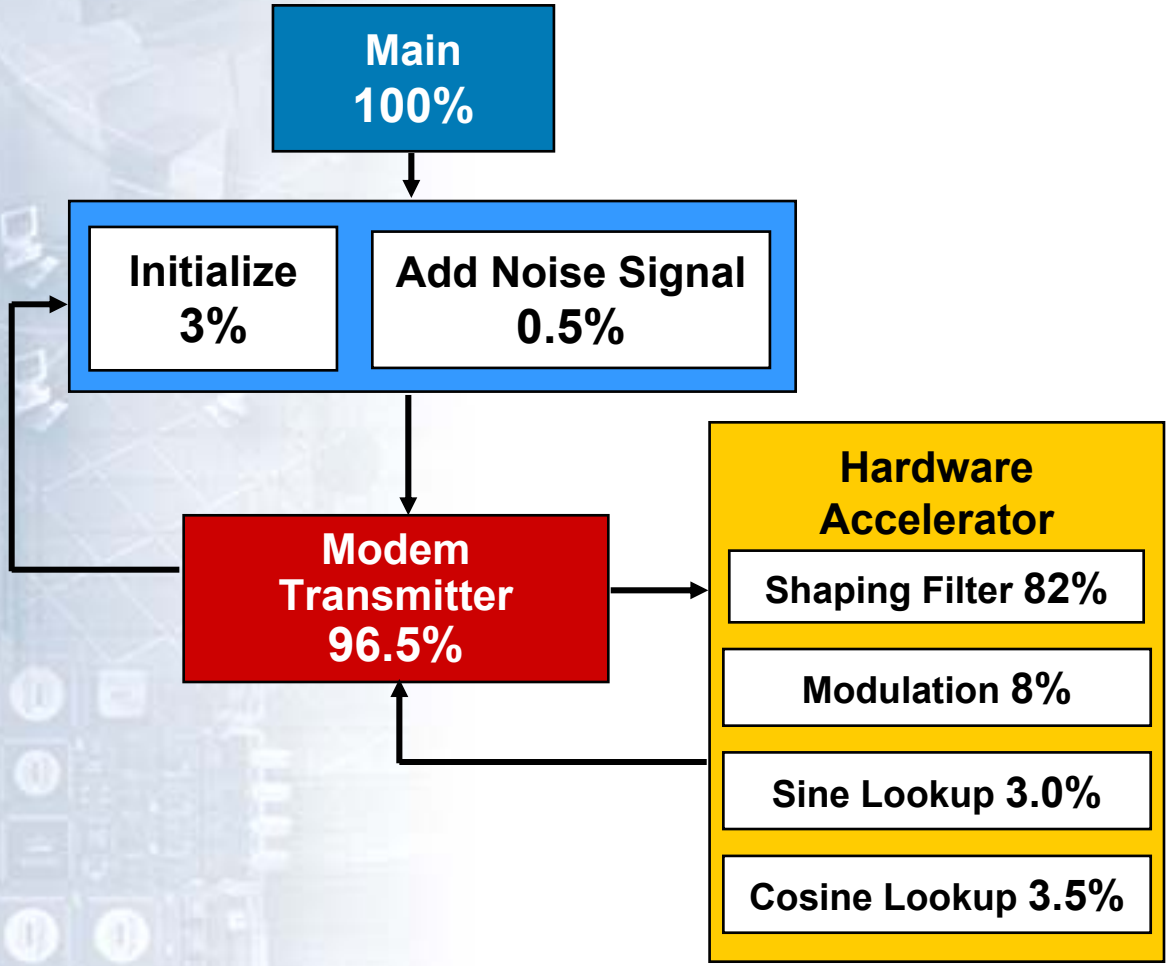
Functions	Code Size	Count	Incl. Total	Incl. Maximum	Incl. Minimum	Incl. Average	Excl. Total
modem.out							
modemtx.c							
main	548	1	4222002	0	0	4222002	23446
ModemTransmitter	304	7	4038331	580782	579499	576904	83981
ShapingFilter	356	14	3610811	258438	257493	257915	3610811
Modulation	236	213	341498	1656	1584	1603	97649
SineLookup	148	490	264817	615	493	540	264817
Initialize	636	1	117760	117760	117760	117760	117760
CosineLookup	56	245	143448	646	539	585	9065
ReadNextData	40	7	5692	820	808	813	259
ReadConstellation	40	7	5370	774	762	767	259
AddNoiseSignal	508	7	5048	728	716	721	5048

Files | Functions | Ranges | Setup

Modem Design Code Profile

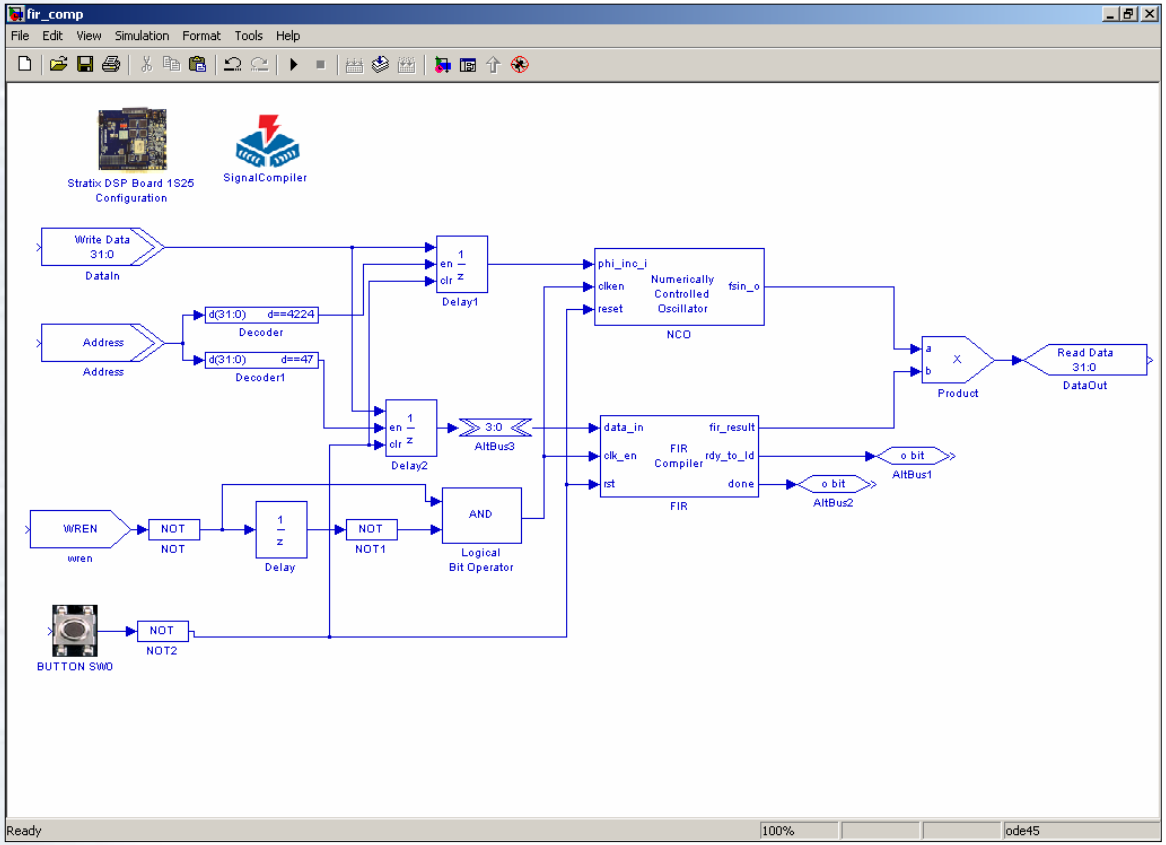


Modem Design Hardware/ Software Petition

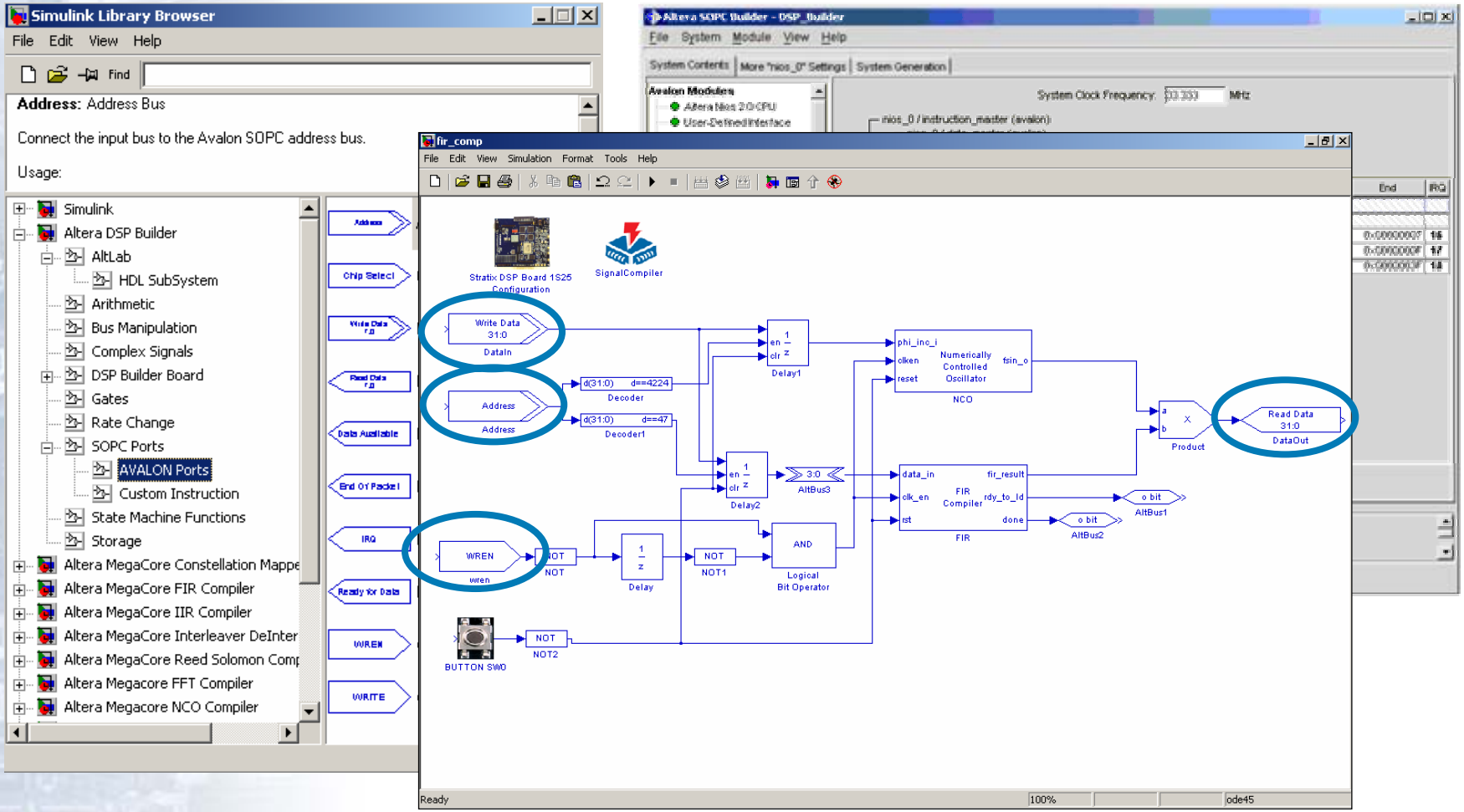


Modulator Co-Processor

DSP Builder Used to Build Hardware DSP Data Path

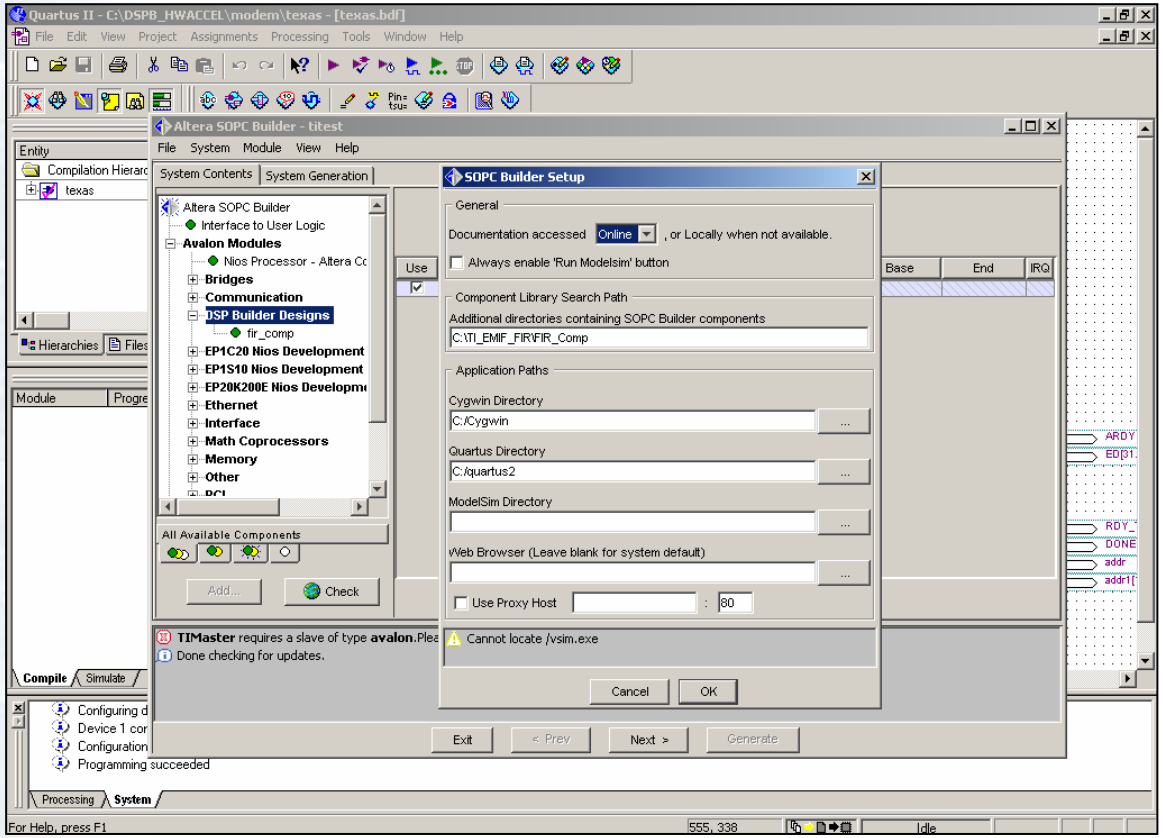


Avalon™ Interface in SOPC Builder



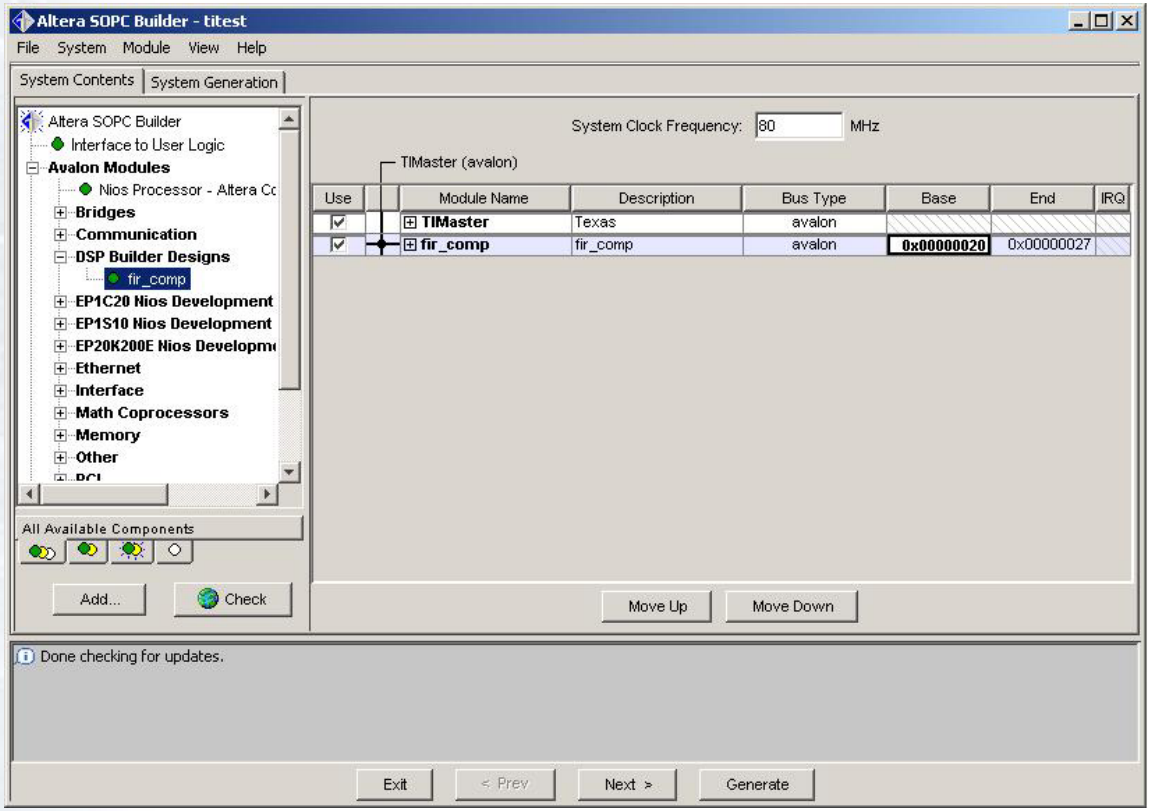
DSP Builder— SOPC Builder Import

Import DSP Builder Generated Co-Processor into SOPC Builder



SOPC Builder Integration

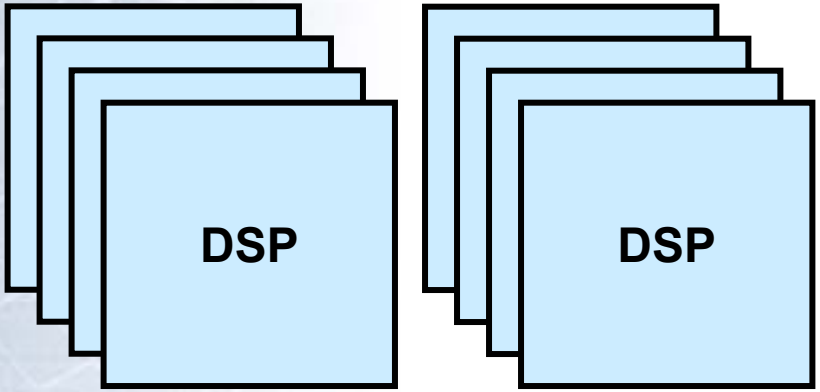
Modem Co-Processor (fir_comp) Integrated with TI EMIF I/F (TIMaster)



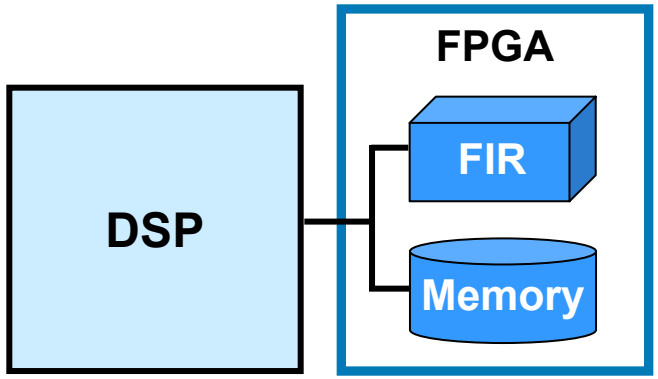
FIR Filter Co-Processor Design Example

Driving Down System Costs

Multi-Processing DSP



Digital Signal Processor + FPGA Co-Processor



FIR Co-Processor Design Example

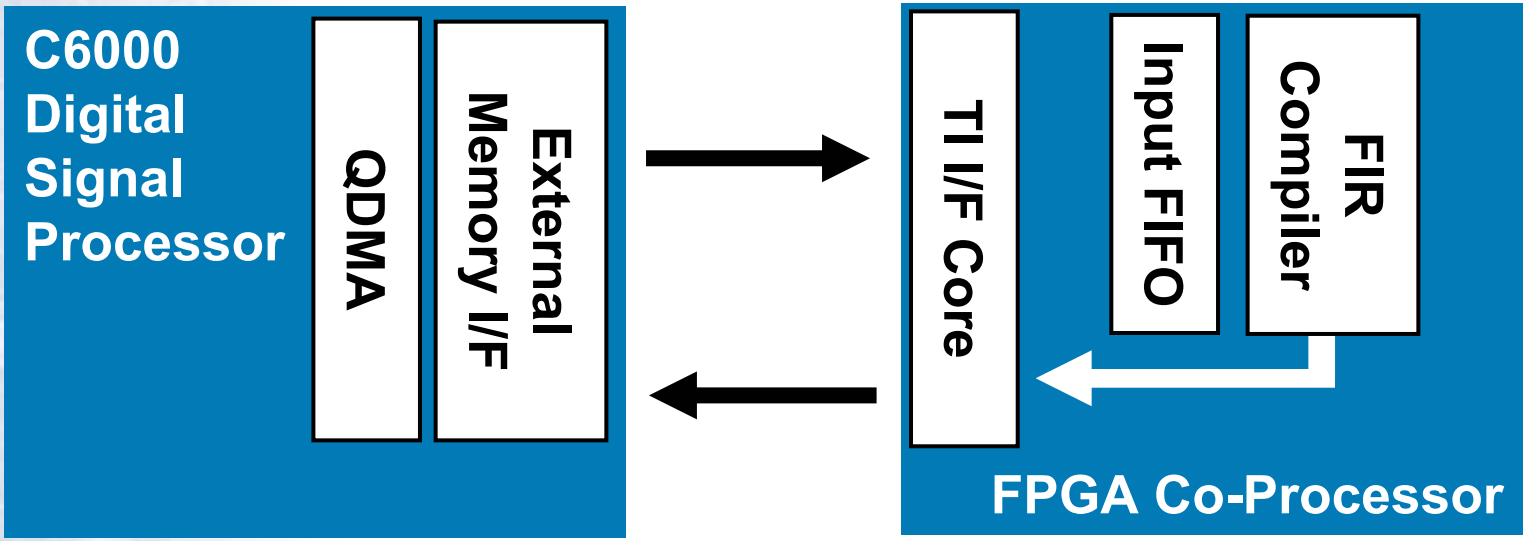
- FIR Parameters
  - 128-Tap
  - 16-Bit Data, 14-Bit Coefficients
- Four FIR Implementations for Comparison
  - TI C6711-Optimized TI DSPLib Function
  - TI C6416-Optimized TI DSPLib Function
  - Altera Eight-Cycle FIR Co-Processor
  - Altera One-Cycle FIR Co-Processor

TI Filtering Library (DSPLib)

- C-Callable Optimized Assembly Routines
- TI C67x DSPLib: FIR Filter (Radix 8)
  - Formula: Nh * Nr /2 + 13
    - Nh = Number of Coefficients
    - Nr = Number of Samples
  - ~1 Sample/ 64 Cycles (128 Tap Filter)
- TI C64x DSPLib: FIR Filter (Radix 8)
  - Formula: Nh * Nr/4 + 17
  - ~ 1 Sample/ 32 Cycles (128 Tap Filter)

Filter Co-Processor Design Example

- Current Implementation
  - 100 MHz, 32-Bit, Asynchronous EMIF on DSK
  - TI Writes 300 Samples to Co-Processor (Input Data)
  - Filter & Send Output to TI

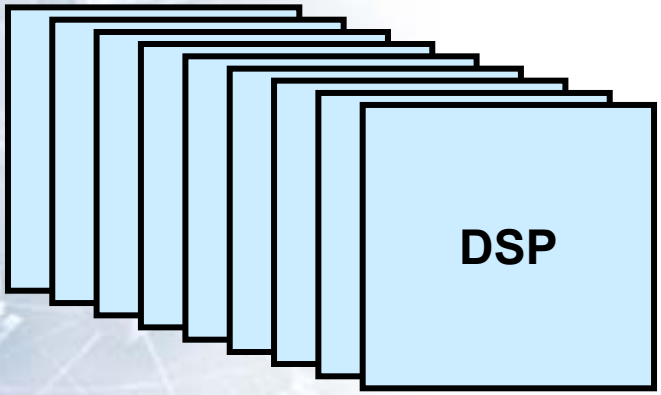


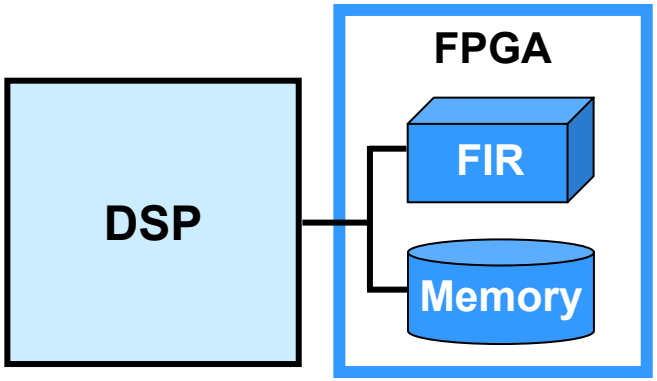
FIR Filter Example* – 16X Cost/Performance Improvement

Device	Solution	FIR Performance (MHz)	Device Cost****	Cost per FIR MHz
TI C6713-200	64-Cycles** at 200 MHz	3.125	$24.59	$7.87
TI C6416-600	32-Cycles** at 600 MHz	18.75	$160	$8.53
Altera EP1C3-8	7-Cycles*** at 197 MHz	28	$14	$0.50
Altera EP1C12-8	1-Cycle*** at 170 MHz	170	$84	$0.49

* FIR 128 Tap, 16-Bit Data, 14-Bit Coefficients
** DSPLib Optimized Assembly Libraries from Texas Instruments
*** Optimized MegaCore FIR Compiler from Altera
**** Pricing in Quantity of 100 at Arrow 6/25/03

14X Reduction in System Costs





Architecture	FIR Performance (MHz)	Total FIR Performance (MHz)	Device Costs	Total Cost
9 * TI C6416-600	9 * 18.75	167	9 * $160	$1,440
Altera EP1C12-8 + 1 TI C6713-200	170 + 3	173	$84 + $25	$110

Summary

- FPGA Co-Processors for DSP Offer Many Advantages
  - 10X Performance Boost
    - More Channels
    - More Complex Algorithms
    - Increased System Throughput
  - 10X Cost Reduction
    - Fewer Components
  - Complementary to DSP-Based Systems
    - Offloads Existing DSP
    - Integrates Into Existing DSP IDE
    - Evolution Not Revolution

Altera Code: DSP Solutions

- FPGAs
  - Stratix, Stratix GX, Cyclone
- Development Tools
  - DSP Builder, SOPC Builder
- Intellectual Property
  - FIR, FFT, Viterbi, Turbo, Reed Solomon, NCO
  - AMPP Third-Party Partners
- Development Kits
  - Altera
  - Third-Parties
- Design Services
  - ACAP Third-Party Partners
- Training