

A Flexible Chip Rate Processor for CDMA Rake Receiver



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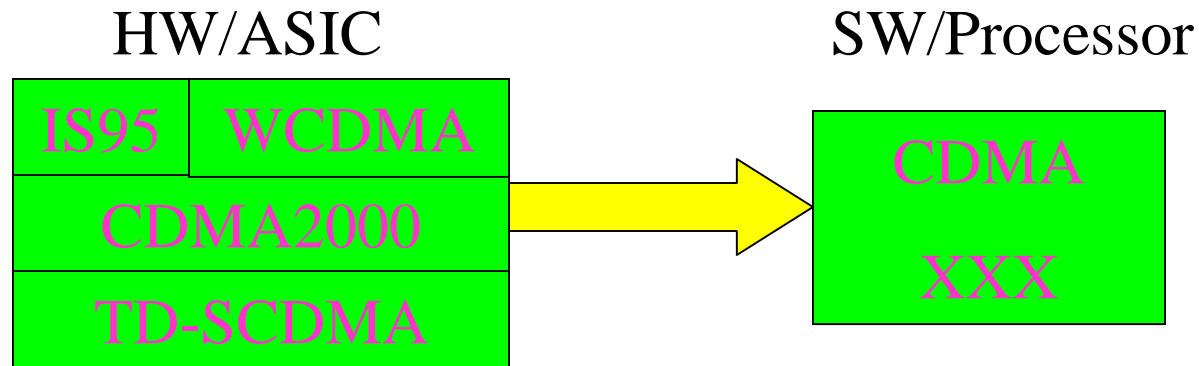


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Motivation: Multimode CDMA



- Various CDMA standards co-exist
 - IS95
 - CDMA2000
 - WCDMA
 - TD-SCDMA (China)

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Page 2



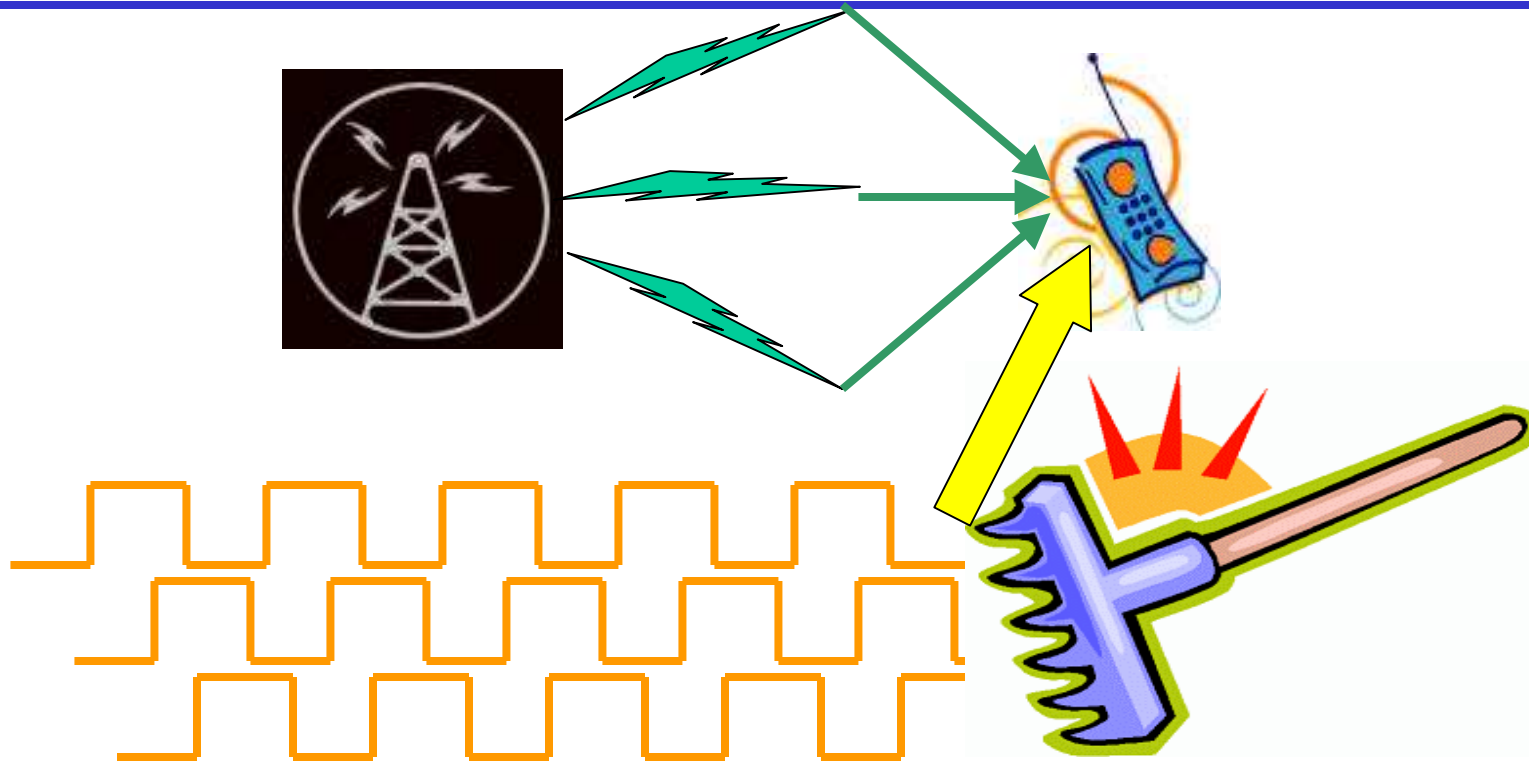
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Rake Receiver for CDMA



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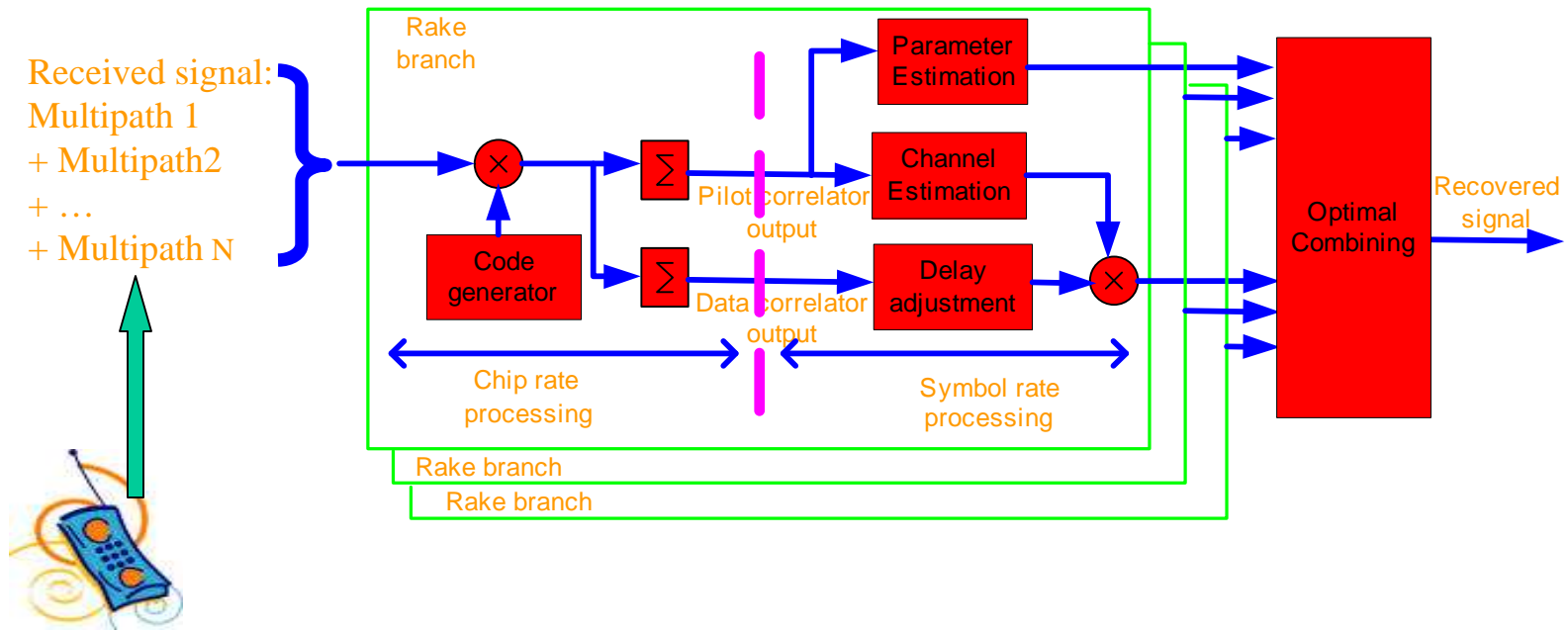
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November 17-19, 2003
Page 3



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Rake Receiver: Signal Processing



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Chip Rate Processing

- Chip rate processing performs:
 - Despreading codes generation (e.g., PN, Gold, Walsh, OVSF)
 - Appropriate input sample fetching
 - Correlation between input samples and generated codes
- Chip rate processing operations are:
 - High data rate
 - Relatively simple arithmetic
 - Short word-length
 - Traditionally implemented using ASIC

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Page 5

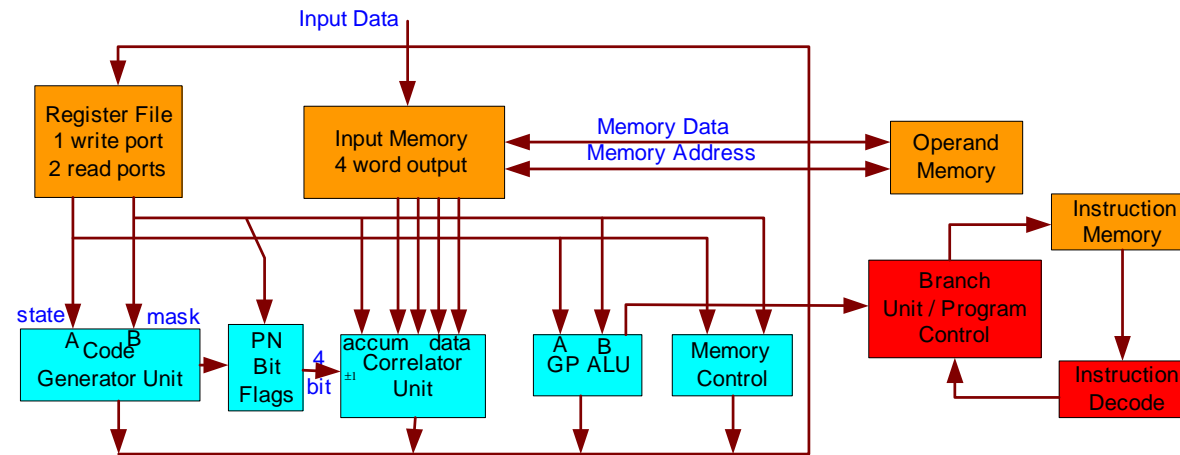
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Chip Rate Processor(CRP):Architecture



- Multiple processing units
- Flexible code generator (4 bits per cycle)
- Parallel correlator unit and flexible input queue
- Traditional processor architecture for SOFTWARE implementation

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Orlando, Florida
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Page 6

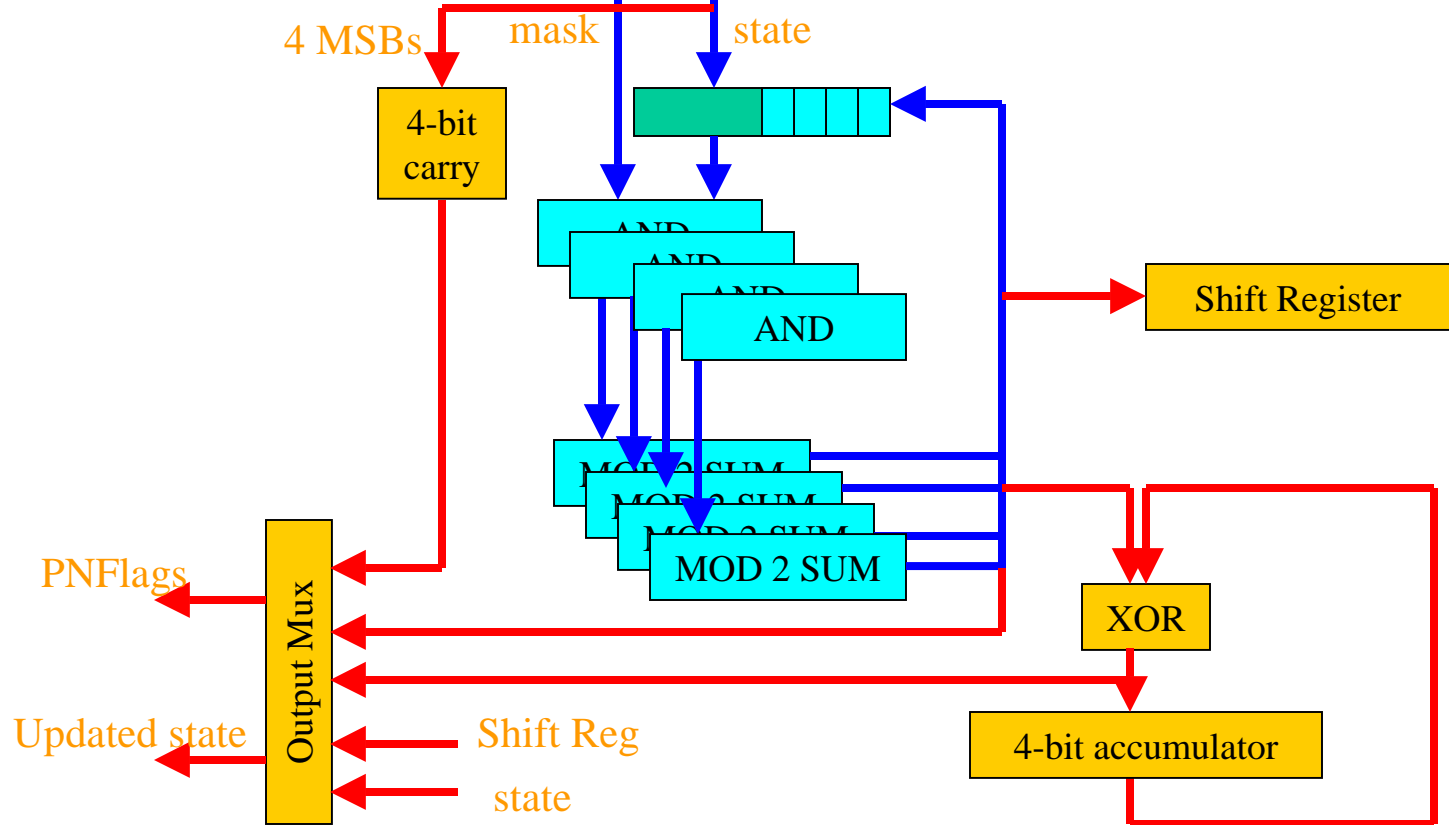
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Code Generator Unit



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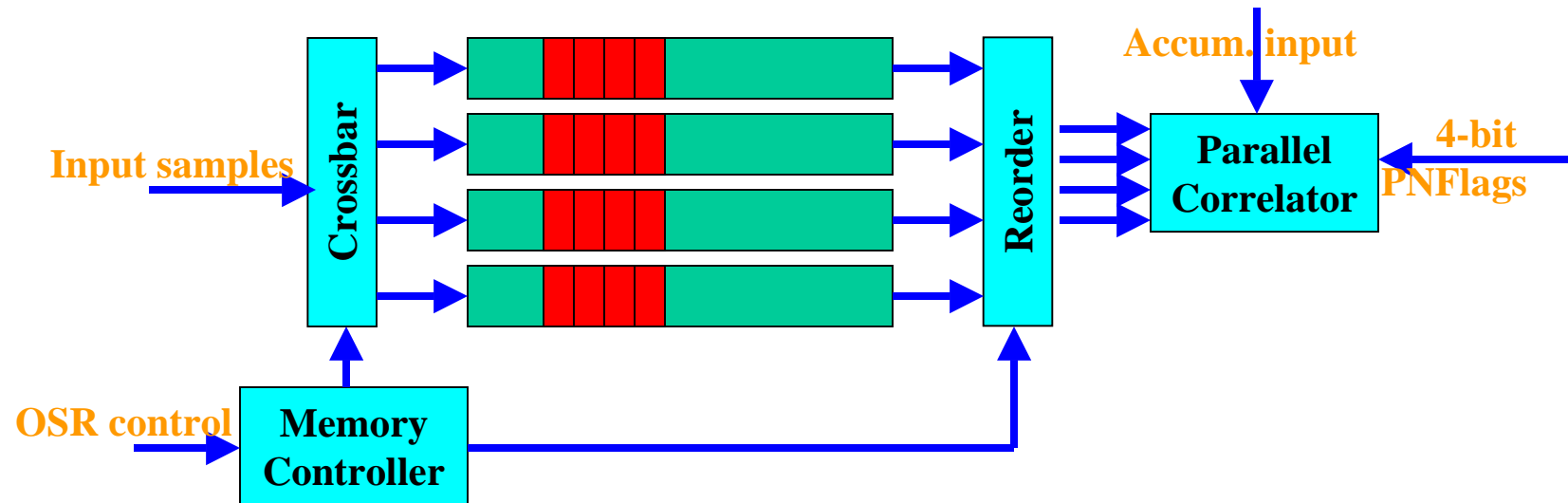
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November 17-19, 2003
Page 7



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Parallel Correlator & Flexible Queue



- Flexible Queue deposits/fetches samples based on OSR (example shows OSR = 4)
- Parallel correlator performs 4-chip correlation/cycle

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Orlando, Florida
November 17-19, 2003

Page 8

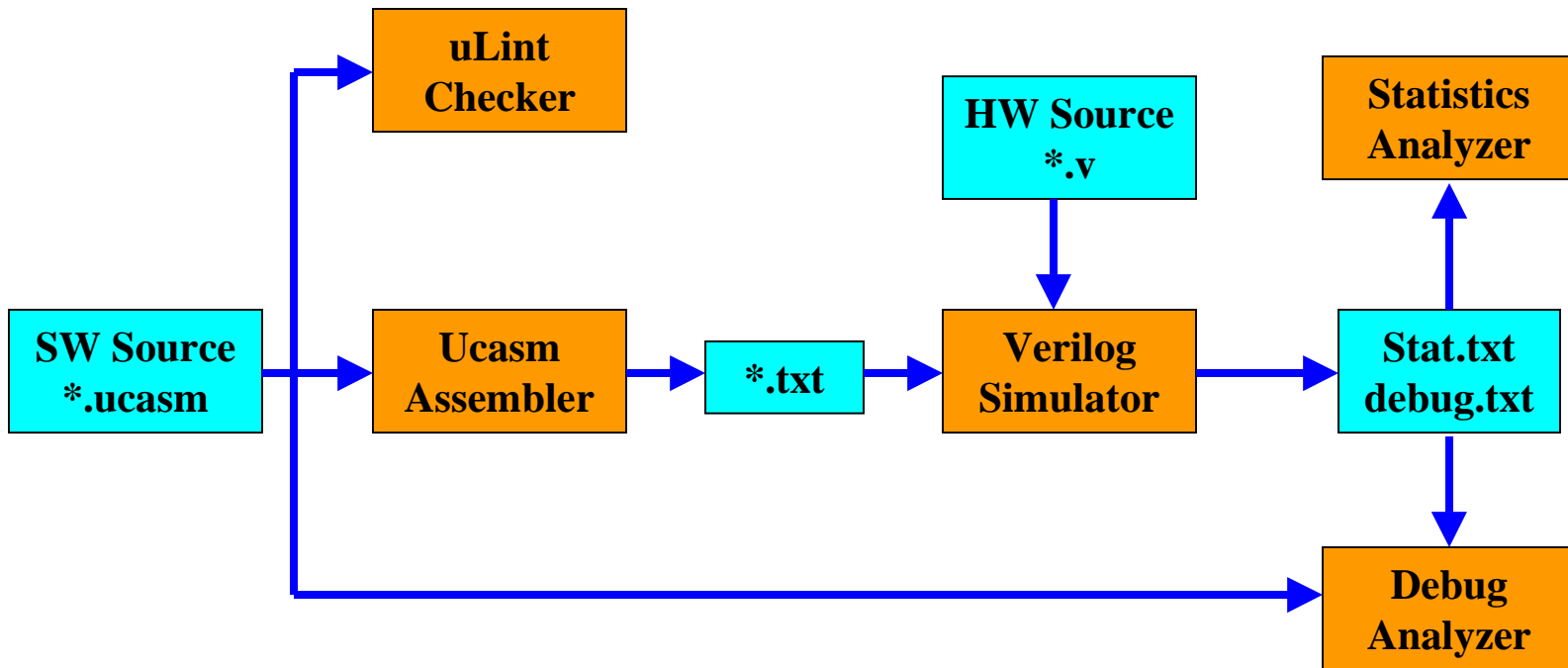
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Software Development Tools



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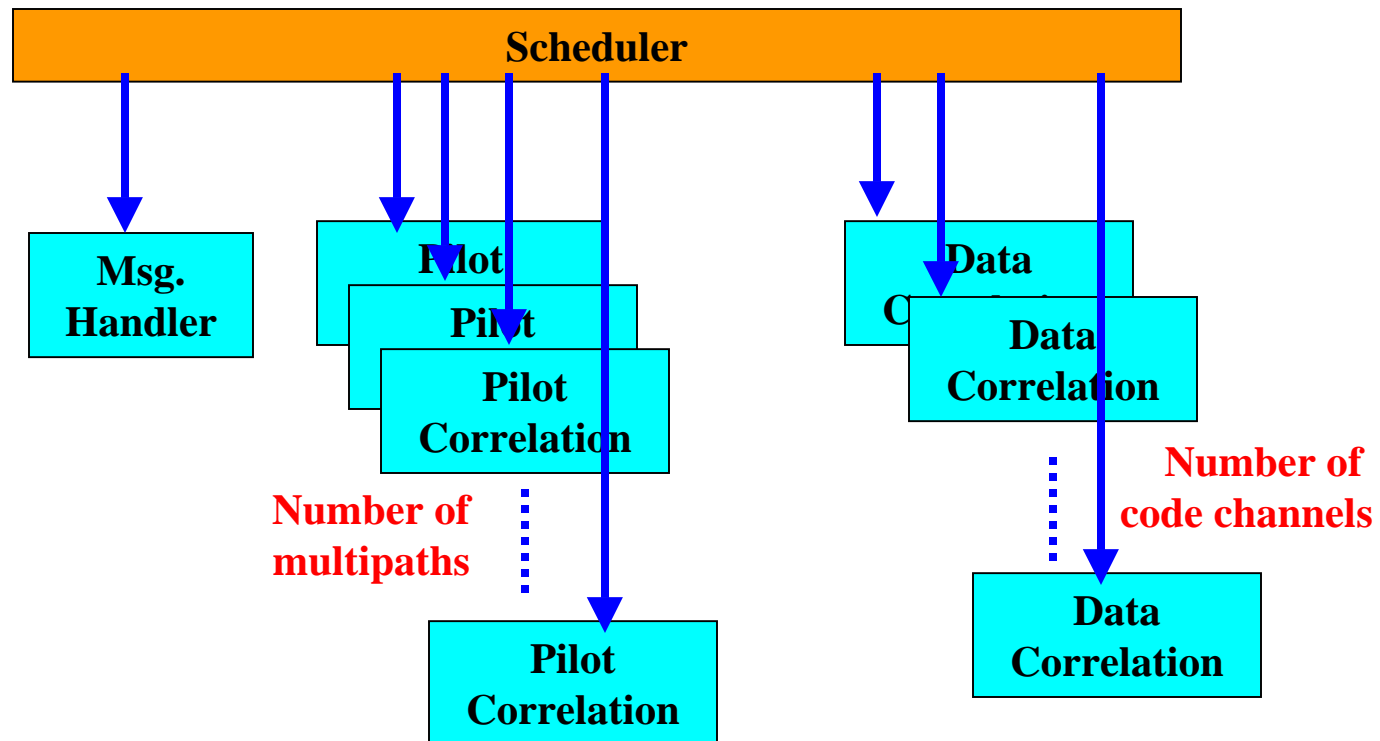
Orlando, Florida
November 17-19, 2003
Page 9



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Software Rake Receiver on CRP



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Basic Correlation Routines on CRP

Pilot Correlation

DoStart0 CorStart;
DoEnd0 CorEnd;
DoEn0 Corent;

CorStart:

MPNgen Pnmask, Pnstate, Pnstate;
McorAcc, A1, CorOn, CorOn;
McorAcc, A2, CorE, CorE;
McorAcc, A3, CorL, CorL;

CorEnd:

Data Correlation

DoStart0 CorStart;
DoEnd0 CorEnd;
DoEn0 Corent;

CorStart:

MPNgen Pnmask, Pnstate, Pnstate;
Mwalsh.c Row, Col, Temp;
Add Col, #4, Col;
McorAcc, A1, Cor1, Cor1;
McorAcc, A2, Cor2, Cor2;

.....

McorAcc, An, Corn, Corn;

CorEnd:

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November 17-19, 2003

Page 11

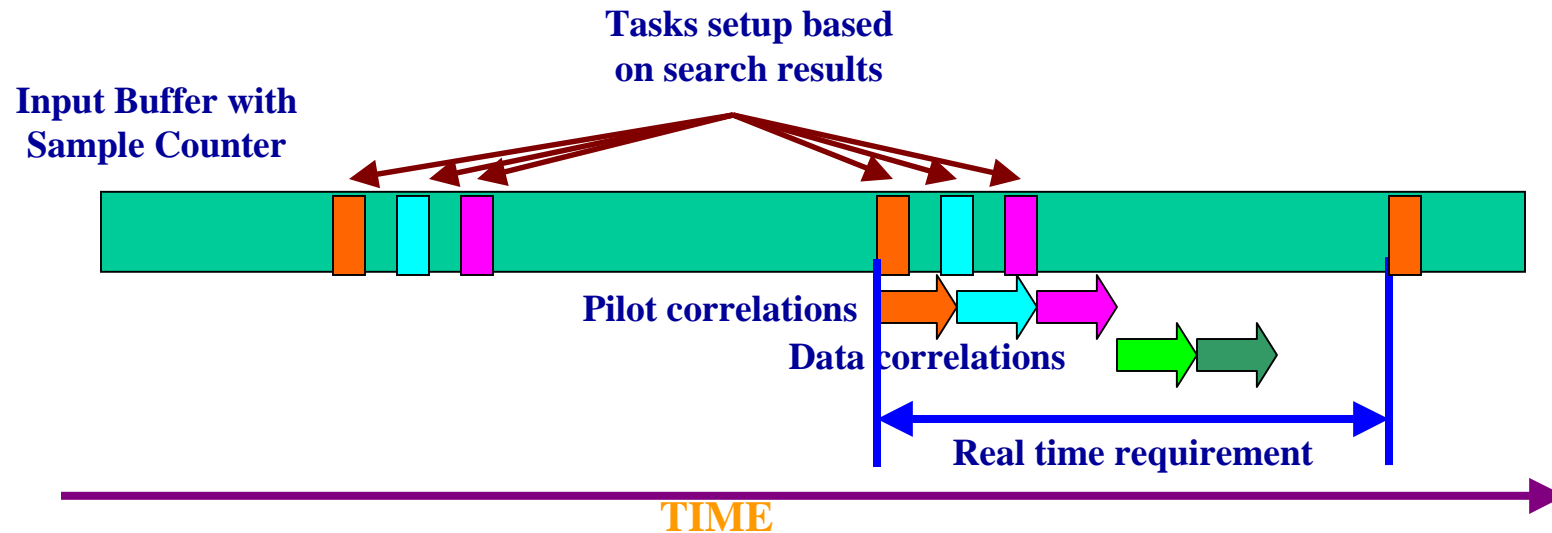
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Correlation Tasks Scheduling



- Tasks aware of when to execute based on time info.
- Batch processing meets real time requirement
- Data correlation waits for latest arriving multipath

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CRP Loading: an Example

Task Name	Clock Cycles	Number of Tasks	Equivalent Mcps	Processor Loading
Pilot Correlation	208	6	24	16%
Data Correlation (SF=64)	444	1	8.52	5.7%
Data Correlation (SF=32)	578	1	11.10	7.4%
Data Correlation (SF=16)	846	1	16.24	10.8%

- Chip rate = 1.2288 MHz, All tasks executed every 64 Chips, Processor clock = 150 MHz
- Most symbol rate processing included

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Conclusions

- A programmable chip rate processor
- Flexible code generator supporting various CDMA standards
- Flexible input queue designed to facilitate parallel correlation
- Software example for rake receiver implementation
- Suitability demonstrated as a software-defined replacement for dedicated ASIC

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