Practical Implementation of Commercial SDR RF Front Ends

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Abstract

All wireless communication systems have traditionally employed a Radio Frequency Front End (RF FE) located between the antenna and the baseband subsystem. The requirement for more cost-effective and reconfigurable RF FEs is one of the major needs of the wireless industry. The perspective of our discussion is that of commercial SDR practitioners, seeking economically viable solutions for the commercial wireless marketplace.

By the end of the Second World War, wireless communication systems had evolved to the point where they could be broken down into the following functions:

- Human Interface
- Local Control
- Prototcol Stack
- Low Speed Signal Processing
- High Speed Signal Processing
- RF FE
- Antenna

In these early systems, each function was implemented with discrete analog technology. This resulted in relatively large, expensive, high power consuming systems which were difficult to design, manufacture and manage/maintain in the field. The desire to lower cost size and power consumption while making devices easier to manage in the field has driven the technology evolution path we are still on today.

As digital technology entered the beginning of its period of rapid evolution, discrete analog components on complex printed circuit boards were gradually replaced. First discrete digital logic components were used to implement the Human Interface, Local Control, and Protocol Stack functions. With the appearance of the microprocessor, the discrete logic components were replaced with a microprocessor called a microcontroller and software. Then the Low Speed Signal Processing analog discrete components were replaced with digital logic components. Then special mathematical functionality (such as Multiply Accumulate, MAC) were added to microprocessors to create Digital Signal Processors (DSP's). Low speed signal processing functions were converted from discrete digital logic to DSP's and software.

Then the High Speed signal processing analog discrete components were replaced with digital logic components. The expectation was that the same process would continue and that the High Speed Signal Processing would be implemented by some kind of a microprocessor and software. However, a fundamental barrier was found.

Although DSP's could theoretically handle the speed of processing required for High Speed Signal Processing of 2nd Generation Air Interface Standards (AIS's), practical limitations created a barrier. The Nyquist theorem requires that a signal be sampled at more than twice its rate of change in order to preserve the data in the signal. This means that a 1.24 MHz signal must be sampled at approximately 3.25 MHz. In order to avoid quantization error, single samples are typically represented by 13

or more bits in Cellular systems. Minimum High Speed Signal Processing requires approximately 100 instructions per sample. This means that a DSP attempting to do High Speed Signal Processing for a 2nd Generation Cellular handset would have to operate at a clock speed in excess of 325 MHz. In practice, because of bus delays, the need to write to buffers, etc. it turns out to be in the GHz clock range. As DSP development progressed, it became clear that since power consumption varied directly with processor speed, it would be difficult to operate a DSP at these clock rates for battery powered applications.

Discrete digital component implementations avoided the power problem by implementing each of the 100 instructions in 100 discrete digital logic circuits arranged in a bucket brigade. In this way, each circuit can run at the clock rate of the sampled and quantized signal (such as 3.25 MHz), dramatically lowering power consumption.

As digital technology continued to develop another alternative appeared. Discrete digital logic components could be combined into a single chip called an Application Specific Integrated Circuit (ASIC). It achieved the cost, size and power consumption advantages inherent in integrated circuits, but it didn't have the flexibility inherent in software driven general purpose processors.
In the early 1990's, solutions to the High Speed Signal Processing requirements that offered software driven flexibility and the ability to change baseband subsystems to support different AIS's through software began to appear [Reference 1]. The appearance of these solutions in the company of market drivers led to the coining of the term Software Defined Radio (SDR). These solutions can be characterized as based on Reconfigurable Logic. Generally, they use software or software like code to configure digital logic to perform the High Speed Signal Processing at relatively low clock rates, thereby achieving the desired power consumption / heat dissipation while they are running, while being able to be reconfigured between runs to support different AIS's [Reference 1]. Recently, prototypes which run 1 G and some 2 G AIS's in standard processors have been demonstrated.

At the time of the introduction of Reconfigurable Logic and the coining of the term SDR, the dominant implementation architecture used for RF FE's was the Superheterodyne Architecture [Reference 3]. The Superheterodyne Architecture was patented in 1915. It was developed to overcome the problems inherent in the Direct Conversion or Homodyne Architecture (sometimes called Zero IF) developed in the 1890's.

The Superheterodyne Receiver uses a chain of amplifiers, frequency synthesizers, mixers, and filters to down convert, limit noise and select the desired channel. It uses two steps of mixing and filtering to achieve the desired result. The first step mixes the signal down to an Intermediate Frequency (IF) and the second step mixes the signal down to Baseband.

The Superheterodyne RF FE's were implemented with discrete analog components. Although there have been many years of work refining the

Superheterodyne Architecture, it by its very nature is not easily integrated with contemporary chip technology. The frequency synthesizers and filters required by the Superheterodyne Architecture require very narrow, very sharply defined band pass characteristics. That is they must pass the desired frequency and reject as much as possible all the undesired frequencies. This is sometimes described as filter quality or "Q". The steeper the filter wall, the higher its "Q". Superheterodyne Architectures require very high Q components.

These components can be built with arrays of resistors, capacitors and inductors (R, L, C). To achieve high Q, very precise values of R, L, and C are needed. Integrated circuit technology requires extremely large chip area to implement accurate R's, L's, and C's. .

What emerges is a practical limit. For a single mode and a single band for cellular applications Superheterodyne RF FE's for personal portable two way devices such as cell phones, generally have as many as 300 electronic (passive and active) parts.

As SDR High Speed Signal Processing technologies emerged from the laboratories and promised multi mode multi band systems, designers began to wonder how to avoide multiplying 300 part RF FE's to achieve multi mode multi band cabaility.
The United Sates Federal Government's Advanced Research Projects Administration (ARPA) contracted with a small Silicon Valley Company (enVia, Inc.) to among other things develop a prototype of a multi mode multi band RF FE that would support multiple modes and bands with maximum efficiency. This prototyping effort grew into a product family named the AN2/6.

A prototype system based on five test boards interconnected by coaxial cable was demonstrated in satisfaction of the ARPA contract in 1998. enVia continued development and in 1999 announced a family of single board RF FE's that was awarded the prize for being the most innovative product of 1999 by RF Development and Design Magazine [Reference 4].

The design objectives were to make the maximum possible reuse of hardware to reduce the part count, size, power consumption and cost to the minimum. . The product provided fast digital switching between bands (824-894MHz & 1850-1990MHz) and modes and was compliant with the AMPS, IS-95, IS-95+, IS 136, IS136+, and GSM mode standards. It processed the Rx signal from antenna to analog I/Q outputs and the Tx signal from analog I/Q input to antenna output. The module design, on FR4 PCB material featured a maximum vertical thickness of 10mm with a small 61x110mm-form factor. A 20% Reduction in size was achievable through the application of automated assembly processes.

The ARPA prototype successfully demonstrated that it was technically and economically feasible to build multimode Superheterodyne Multiband RF FE's that would support SDR digital sub systems. It showed that by innovative design methods and a focus on maximizing hardware reuse, Superheterodyne RF FE's with substantially lower parts counts, than with separate Superheterodyne RF FE's

for each mode and band, were achievable, leading to lower size, cost and power consumption.

The most fundamental lesson learned was that the Superheterodyne Architecture RF FE for cellular and similar applications was that it was on a long term cost / performance curve that was not likely to be changed. In fact, it appeared that the Superheterodyne RF FE's cost / performance curve might be reaching an asymptote.

If the cost performance curve for RF FE's for cellular and similar applications (highest volume market with the most competitive pricing) is plotted over the last twenty years, it can be seen to be declining at a 1% to 5% annual rate (see Figure 7) [Reference 6]. This compares with the Moore's Law curve for digital technology of doubling capability and halving price every eighteen months.

Some have attempted to achieve higher integration levels with exotic materials. Some of these materials have been and still are used for special components such as Power Amplifiers (PA's). In this case, the attempt was to increase integration levels by using them to implement other parts of the Superheterodyne Architecture. Examples of materials include:

- GaAs –Gallium /Arsenide
- SiGe – Silicon Germanium
- SoS – Silicon on Saphire
- SoI – Silicon on Insulator

These materials are able to increase speed and to increase the isolation of functions. These are very useful properties, however they do not address the fundamental limiting factor, the need for high Q. Furthermore, application of these materials and their associated processes, adds significant cost and risk.

The first alternative to the Superheterodyne Architecture that received wide spread industry attention was the Direct Conversion Architecture, sometimes called Homodyne, or Zero IF (ZIF). Direct Conversion eliminates one of the two stages of up/down conversion in the Superheterodyne Architecture. In so doing it can eliminate approximately one third of the parts used in a Superheterodyne Architecture.

At first, this sounds like a good deal. However, the Direct Conversion Architecture has fundamental noise performance problems that the Superheterodyne Architecture was created to overcome. It is true that for some AIS's these problems can be overcome, by using advanced DSP algorithms to eliminate the noise, but only at the price of additional power consumption by the DSP

It should also be pointed out that, like the Superheterodyne Architecture, the Direct Conversion Architecture lacks the capability to provide the flexibility previously obtained in the other subsystems (Baseband and Controller) through software driven architectures. Direct Conversion RF FE's have to be designed from the beginning for very specific modes and bands. Although they can be switched between bands and some modes, once built the bands and modes supported can not be changed.

As the limitations of integrated Direct Conversion Architectures became clear, attention once again returned to pure digital solutions. On the one hand, pure Digital Architecture solutions potentially

offered all the advantages of flexibility offered by software driven integrated hardware. On the other hand, this approach still seems to face insurmountable challenges. If the High Speed Signal Processing functions in the Baseband section created very difficult power consumptions / speed challenges; the frequency / speed / bandwidth requirements in the RF FE being several orders of magnitude higher move from very difficult to impossible.

Such a solution puts an analog to digital converter (ADC) at the antenna and does all down conversion and filtering in a digital signal processor (DSP). The ADC and DSP functions can be implemented in CMOS yielding the theoretical possibility of a 3, 2 or 1 chip RF FE solution with resulting decrease in cost and risk and the solution would be agile / flexible under software control. Unfortunately, the digital solution requires the ADC and the DSP to run at extremely high speeds thereby consuming extremely large amounts of power[1].

It is very difficult to operate an ADC at today's typical Cellular / PCS frequencies in the 2 GHz range. Low cost, low power ADC's for these frequencies are not generally commercially available today and show little likelihood of being available in the near future.

Even so, assuming that an ADC is available, a simplified Rx example solution with an incoming signal at 2GHz would sample the signal at 5 GHz and encode each sample in 16 bits. An optimistic estimate of the processing required in a single stream instruction set processor for the filtering and down conversion process would require 500 instructions per sample. Therefore the DSP would have to run at 2,500 GHz. The most optimistic estimate is that a full custom ASIC solution might be able to get the clock rate down to as low as 10 GHZ. Given that the receiver is on all the time, and that Chip power consumption is a direct function of clock speed, the power consumption for the full digital solution is so great that it is not practical for cell phones for as far into the future as we can see. In fact not only are there no commercially announced full digital solutions for handsets, there are none for Base Stations where power consumption is less constrained.

Some have tried to combine analog mixing and down conversion with digital down conversion and filtering. This architecture uses the first stage of a Superheterodyne Architecture solution (one stage of synthesis, mixing, and filtering) to bring the received signal down to IF. Then instead of the second analog stage (second stage of synthesis, mixing, and filtering) a digital down conversion and filtering stage is employed. By reducing the frequency of the signal, the speed at which the digital section must run is also reduced. In this way it is theoretically possible to avoid the noise burden the ZIF solution places on the Baseband section while eliminating the parts associated with the second down conversion stage. This approach can provide performance comparable to a Superheterodyne system.

Unfortunately, the power consumption in the digital section (A/D converter, digital down converter and digital filter) of this solution is still very large and the

digital parts can be expensive to manufacture thus negating the cost and power reduction goals. The power consumption comes directly from the speed of the signals being processed (still several orders of magnitude higher than Baseband). The cost of the digital chips comes from the size of the ASIC's (die area) required to implement the digital processing. Furthermore, some implementations seek to meet legacy Baseband interfaces by adding a digital to analog converter at the end of the digital chain so as to provide analog I & Q to the Baseband interface, further increasing the cost, size and power consumption of this solution approach.

The SDR RF FE alternatives discussed above define a solution space. On the upper left hand corner is the Superheterodyne Architecture. It provides good signal quality, but has relatively high power consumption and very high cost and size. Finally, it lacks the desired characteristic of the type of flexibility offered by software driven standard hardware architectures.

The upper right hand corner is the Direct Conversion Architecture. It provides lower cost and size in the RF FE, but the signal quality is degraded and large amounts of power must be used in digital filtering added in the Baseband. It also lacks the desired characteristic of the type of flexibility offered by software driven standard hardware architectures.

The lower left hand corner is the Pure Digital Architecture. It promises the desired characteristic of the type of flexibility offered by software driven standard hardware architectures. It is also theoretically very small in size and part count. However, while theoretically possible, its power consumption / processing speed requirements put it beyond practical reach.

The lower right hand corner is the Combination Analog Digital Architecture. It overcomes the Direct Conversion Architecture's signal quality problems while keeping its size lower than the Superheterodyne Architecture. However, its power consumption and cost are high.

What these architectures suggest is that there is a solution within this space (the sweet spot) which has the type of flexibility offered by software driven standard hardware architectures, while putting the RF FE on or near the Moore's Law curve for power consumption, size and cost. To find this solution will likely take a creative approach not widely pursued by the industry at this time.

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