

DEVELOPMENT OF SOFTWARE RADIO PROTOTYPE

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ABSTRACT

This paper is a report on a software defined radio prototype aimed at integrating various types of legacy radio equipment in public, civil and other fields. This prototype supports various types of analog and digital modulation, providing four full-duplex channels. The frequency coverage is 2-500MHz, and transmitting power output is +20dBm (100mW). Because of the low power output in this prototype, an external power amplifier has to be used. In order to cover 2-500MHz, two separate power amplifiers for HF and V/UHF are used. A single intermediate frequency (IF) of 70 MHz is used in common for radio frequency (RF) signals in the range of 2-500MHz. Under sampling analog to digital (A/D) conversion is employed, with the sampling frequency set to 40MHz. The prototype consists of a RF unit and a Signal processing/control unit, with a separate Human Machine Interface (HMI) terminal. Each RF and Signal processing/control unit consists of several modules. Various types of analog and digital modulation (waveform) software were developed for this prototype.

Testing confirmed that this prototype exhibits more than equivalent performance to traditional radio designs for basic analog and digital modulation modes. Also, radio relay operations for the analog modulation including Bridge mode were demonstrated.

1. INTRODUCTION

To realize both high flexibility and adaptability in the software radio [1],[2], it is important to develop both the hardware and software technologies that assure such performance. This prototype was developed to enable integration of various types of legacy radio equipment in a single re-configurable radio. During the development program, the architecture of the hardware platform such as functional allocation to units and modules, and definition of module interfaces, were considered. Evaluation tests were carried out for the functions, such as software download

and parameter control, and overall performance of the radio equipment. This paper reports on these topics.

2. BASIC DESIGN CONCEPTS

The following are considered for basic design concepts of this prototype development.

- Installation of a CPU in each main module, taking into account future flexibility.
- Allocation and partitioning of signal processing to FPGA and DSP.
- Provision of Bridge and Repeat radio relay functions.
- Accommodation of four full-duplex channels.
- Wide radio frequency coverage, 2 - 500MHz.
- Wideband signal processing using higher IF frequency.

3. SPECIFICATIONS OF PROTOTYPE

Based upon the above basic concepts, the specifications were fixed as shown in Table 1.

Table 1. Specifications of the prototype

RF range	2-500MHz
Waveform	SSB (USB•LSB),AM,FM BPSK, QPSK, 8PSK, 16QAM
Number of channels	Max.4 channels of full duplex
Radio relay	Repeat/Bridge
Frequency accuracy	< 0.1ppm
Rx IF frequency	70MHz (Double Conversion)
Tx IF frequency	25MHz (Triple Conversion)
Dynamic range	14bits (Quantize Bits)
Rx IF sampling frequency	40MHz (Under Sampling)
Tx IF sampling frequency	100MHz (4x Over Sampling)
Signal processing	FPGA: Quadrature MODEM DSP: Baseband MODEM
FPGA	XCV2000E x 3
DSP	TMS320C6701 x 4

CPU	Control module: Celeron Peripheral module : SH3
System bus (Sig./control Unit)	cPCI
System bus (RF Unit)	Original (cPCI Form Factor)
Operating System	Linux
HMI	Operates from web browser
Interface	Audio I/O, Serial I/O, Ethernet (100BASE-TX)

4. HARDWARE

This chapter describes the prototype system architecture, each unit and its internal modules.

4.1. Architecture

As shown in Figure 1, this prototype is composed of a RF unit, a Signal processing/control unit with a separate HMI terminal. Each unit consists of several 6U (Eurocard) compact PCI (cPCI) modules. As shown in Figure 2, the RF unit is accommodated in the upper part, and the Signal processing/control unit is in the lower part of a standard 19 inch rack.

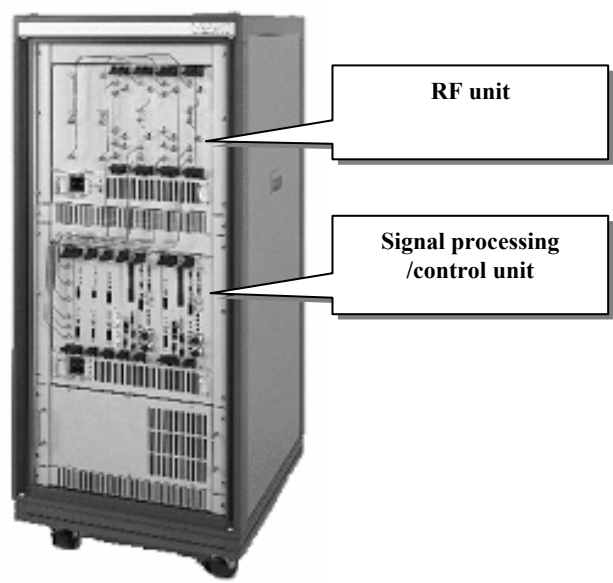


Figure 2. Prototype overview

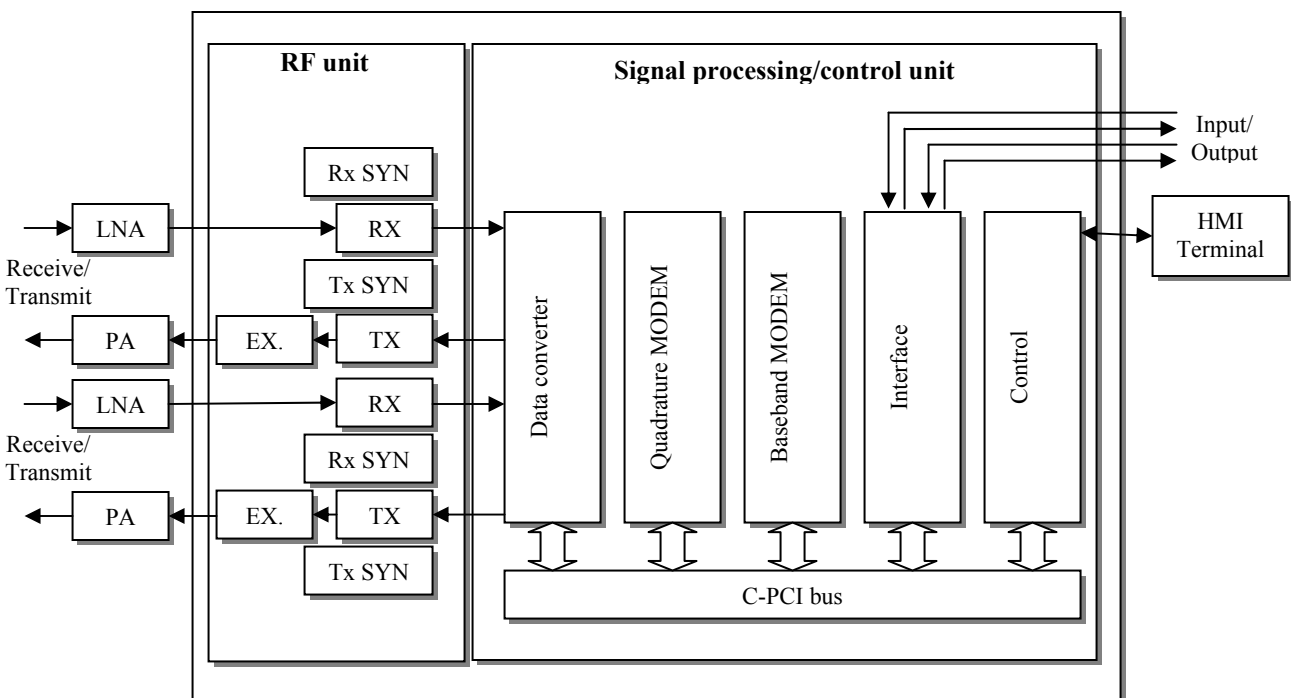


Figure 1. Block diagram of the prototype

4.2. RF unit

4.2.1. Receiver module

A 70MHz IF is selected, taking into account the following aspects of receiver configuration.

- Single IF to be used in common for the entire RF range of 2-500MHz.
- Convenient frequency to maintain an appropriate receiver spurious response
- Wide bandwidth of IF filter, 5MHz or more, to support a wideband signal processing.
- Restrictions due to sampling frequency of the A/D converter.

To suppress receiver spurious response, a double super heterodyne design, with a first IF frequency above 70MHz, is adopted for frequency conversion from RF (2-500MHz) to the 70MHz IF, taking into account lower receiving frequencies than the 70MHz IF.

4.2.2. Transmitter module

To suppress transmitter spurious emissions, triple frequency conversion, with a third IF higher than the transmitting frequency, is adopted for frequency conversion from first IF of 25MHz into RF signals of 2-500MHz.

4.2.3. Synthesizer module

To achieve independence between transmitter and receiver, an independent synthesizer is provided for each transmitter and receiver. The synthesizer realizes high C/N over the entire transmitter and receiver frequency ranges of 2-500MHz.

Table 2. Specifications of synthesizer module

Frequency step	100Hz for HF 12.5kHz for V/UHF
C/N	100dB/Hz (typical at 10kHz offset)
Output level	+10dBm
Lock up time	1.6msec (typical)

4.2.4. Exciter module

Transmitting power output of the Exciter module is +20dBm (100mW), providing flat power output within 2-500MHz. Because of the low power output in this prototype, an external power amplifier is employed. The power amplifier consists of two frequency bands, HF and V/UHF.

4.3. Signal processing/control unit

The Signal processing/control unit consists of the following modules: Data converter, Quadrature MODEM, Baseband

MODEM, Interface, and Control. Every module in the Signal processing/control unit is connected to each other by PCI bus, and provides a CPU in addition to the FPGA and DSP devices. These CPUs play a role of "adapter" defined in the SCA (Software Communication Architecture). In the design concept, FPGAs perform common signal processing for each modulation mode and simple cycle-intensive processing, while DSPs are allocated more complicated processing in baseband, taking into account high IF frequency. The configuration data of a FPGA can be downloaded through the adapter (CPU).

4.3.1. Data converter module

The data converter module performs: filtering of the receiving IF signal, A/D conversion of the receiving IF signal, D/A conversion of the transmitting IF signal, and filtering. In order to secure a sufficient dynamic range of the equipment, it is necessary to provide 14 bits or more for the number of quantization bits of the A/D converter. The practically usable maximum sampling frequency of the A/D converter that realizes 14bits of quantization was 40MHz at the beginning of development. Therefore, A/D conversion was realized by under sampling [3] with 40MHz sampling frequency that converts 70MHz IF signal into baseband. The transmitting IF signal was set to 25MHz, and D/A conversion was realized with 4x over sampling frequency of 100MHz, which converts digital IF into analog IF.

4.3.2. Quadrature modem module

The Quadrature MODEM uses FPGAs to process quadrature modulation/detection, sampling rate conversion, and filtering. Rate conversion is realized using the CIC (Cascaded Integrator and Comb) filter. Thereby, it can be set for a suitable baseband sampling rate corresponding to the modulation mode. The other processing such as analog modulation processing, mapping processing of digital modulation, channel equalization, etc., are performed in the baseband MODEM module.

4.3.3. Baseband modem module

The Baseband modem processes multiple channel modulation/demodulation process using four floating points DSP devices. The processing can be flexibly assigned to each of the four DSPs. The software for the DSP can be downloaded through the adapter (CPU), just as with the FPGA of the Quadrature MODEM. An individual DSP is assigned for each channel. Therefore, even if processing of either channel is under execution, a program can be downloaded to another channel.

4.3.4. Interface module

The Interface module provides analog I/O and digital I/O port interfaces allowing various types of legacy radio to be replaced with this software radio equipment. In addition,

the data input/output through the Ethernet interface of the Control module are also possible for digital modulation.

4.3.5. Control module

The Control module that provides the main control function of this prototype occupies the cPCI system slot. This module employs a commercially available (COTS) PC/AT compatible CPU board .

5. SOFTWARE

Waveform software for various modes of analog and digital modulation were developed. Each waveform is realized by a DSP program. Independent programs are used for modulation and demodulation for each modulation mode, allowing independent waveforms to be downloaded to each transmitter and receiver of multiple channels in this prototype. Switching time for modulation mode switching should be kept to a minimum. While program download to a DSP can be made quickly, configuration data download to a FPGA needs a significant long duration. Therefore, download to a FPGA for modulation mode switching should be avoided in practice. To achieve this goal, functions allocated to the FPGA processing in the Quadrature MODEM should be common to multiple modulation modes. Using I/Q signals for the interface between the Quadrature and Baseband MODEM (including analog modulations), this resulted in; realization of common processing in the Quadrature MODEM for the modulation modes in our target, and elimination of download to a FPGA for the modulation mode switching.

6. HMI CONTROL

The HMI terminal, connected to the Control unit through the Ethernet, is implemented using an Internet (www) browser for control of the software radio. A COTS PC is utilized for the HMI terminal. The HTTP server function is performed in the Control module. Downloading of application software from the HMI terminal into the Control unit is performed by FTP via the Ethernet. The downloaded application software is saved at a storage device of the control unit, and is transmitted to each peripheral module via the cPCI bus by the control module.

An example screen shot of this operation is shown in Figure 3. The present frequency, the waveform, the state of input/output media, the transmitting state, and the state of radio relay, etc. are displayed graphically.

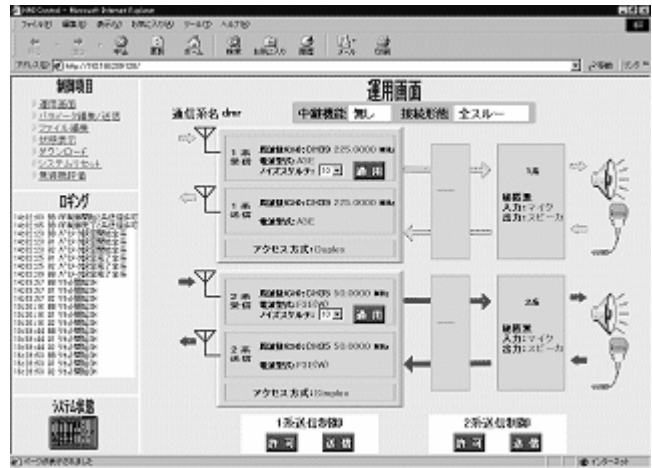


Figure 3. Operation view

The parameter setting screen is shown in Figure 4. The parameters setting for such as frequency, waveform and input/output media, are made on this screen. In addition, a download management screen, a maintenance screen, etc. are provided.

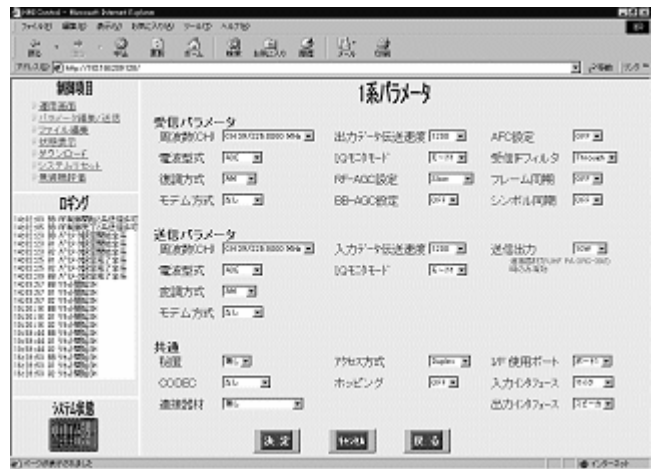


Figure 4. Parameter setting view

7. PERFORMANCE EVALUATION

7.1. Analog Modulation

Satisfactory performance was obtained for each analog modulation as shown in Table 3; Evaluation results. For example, in SSB, carrier suppression and undesired sideband are not generated theoretically in digital signal processing, while it is a predominant feature in many legacy radio designs. However, since the PA is not included in this measurement, it is necessary to take into consideration undesired sideband of SSB etc., which may be generated due to non-linearity of the PA.

Table 3. Evaluation Results

SSB	Tx	Carrier suppression	< -70dB
		Undesired sideband	< -70dB
		SINAD	36.0dB
AM	Rx	SINAD	34.0dB
	Tx	SINAD	48.0dB
FM	Tx	Maximum modulation depth	100•
		SINAD	30.5dB
	Rx	SINAD	51.0dB

7.2. Digital Modulation

The receiver BER performances over BPSK, QPSK, and 16QAM at static environment are shown in Fig. 5.

For the digital modulation, channel equalizer software (bi-directional decision feedback type) was incorporated anticipating operation in multi-path fading environments.

The BER performance of 16QAM in the multi-path fading environment is shown in Fig. 6. The channel equalizer operates appropriately in a multi-path fading environment of between 0.5 - 3.0 ms delay time in two ray model. The constellation of 16QAM after equalization processing is shown in Figure 7.

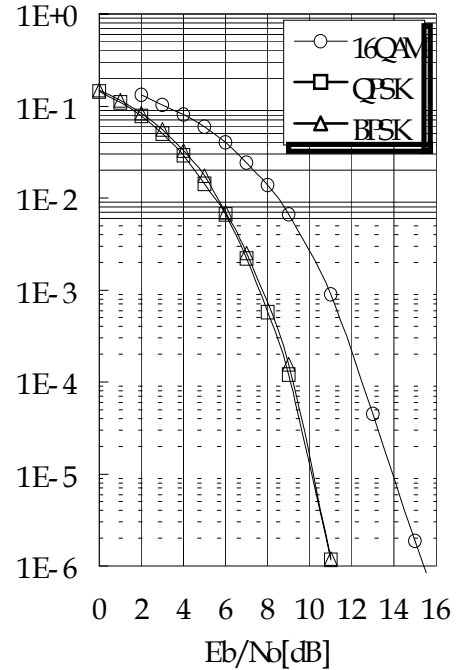


Figure 5. Receiver BER performance of digital modulation at static environment

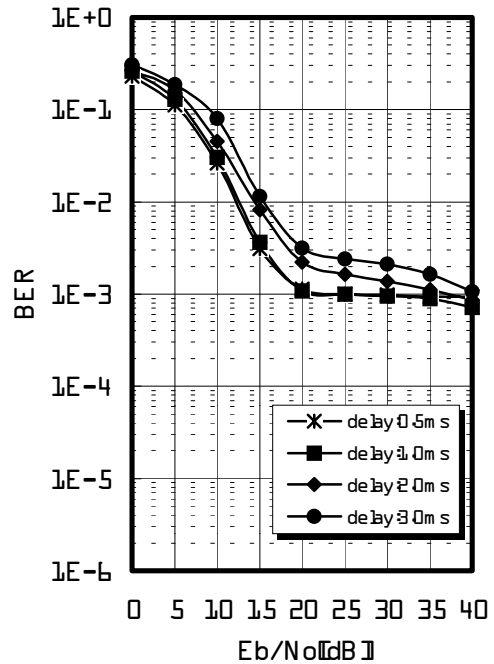


Figure 6. Receiver BER performance for 16QAM at multi-path fading environments

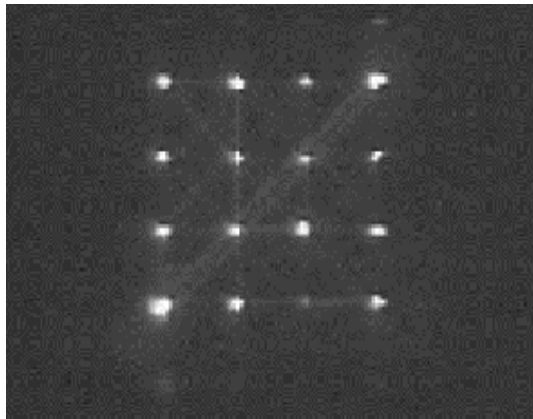


Figure 7. The constellation of 16QAM after equalization

7.3. Radio relay function

Since this prototype has multiple full duplex channels, various types of radio relay functions can easily be realized. Besides the conventional repeater mode, the bridge relay, which employs different modulation mode before and after relay, was also implemented. Concept of the bridge relay is shown in Fig. 8. Satisfactory operation was confirmed for both repeater and bridge relay in various analog modulation modes.

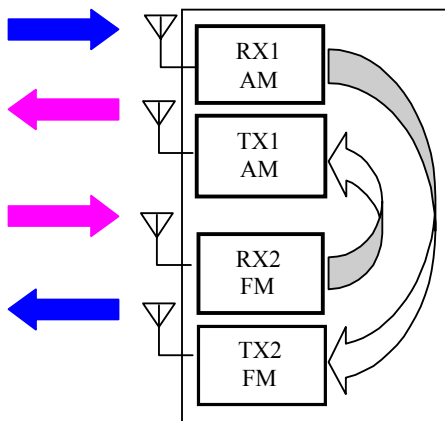


Figure 8. Concept of the bridge relay

7.4 Overview

In analog modulations, better performance was achieved using digital signal processing than by using conventional analog processing, in accordance with theoretical design estimates. In particular, much better performances was obtained over the legacy radio in modulation accuracy and transmitting noise characteristics. As for receiver demodulation, it shows that adoption of an under sampling technique for receiving signal A/D conversion can result in,

satisfactory performance in the SINAD (noise and distortion) characteristics by using a suitable anti-aliasing filter and a high accuracy clock oscillator. Satisfactory operation of the channel equalization for receiving digitally modulated signals was also confirmed.

8. CONCLUSION

A prototype was developed with the goal of replacing and integrating various types of legacy radio equipment from the public, civil and other sectors. To achieve this goal, design of a practical hardware platform appropriate for software radio implementation is an important issue. Design aspects such as composition of units and modules, and module interface were considered. Functionality, such as software download and parameter control, and overall performance of the radio equipment were evaluated in this research. In the analog modulations, better performances were achieved using digital signal processing than with the legacy radio's analog methods. During demodulation, processing range of the digital signal processing was expanded by using a higher sampling frequency for under sampling A/D conversion. Adopting under sampling techniques to the received signal A/D conversion, satisfactory performance is obtained by using a suitable anti-aliasing filter and a high accuracy clock oscillator, etc. Also, appropriate radio relay operations including Bridge mode were confirmed for the analog modulation system.

This prototype was developed to explore and evaluate a design approach of for multi-band, multi-mode SDR hardware platform realization. However, our target is commercial use of software radio systems based on a new SDR architecture called the Software Communications Architecture (SCA) being adopted as a commercial software standard. At present, a new prototype is being developed. This new prototype will use an upgraded hardware platform and adopts the SCA.

9. REFERENCES

- [1] J.Mitola, "The Software Radio Architecture", IEEE Communications Magazine, Vol.33, No.5, pp.26-38, May. 1995.
- [2] J.Mitola, "Software Radio Architecture: A Mathematical Perspective", IEEE J.Sel.Areas Commun., Vol.17, No.4, pp.514-538, April. 1999.
- [3] R. G. Vaughan, N.L.Scott and D.R.White, "The Theory of Bandpass Sampling", IEEE Trans. Signal Proc., Vol.39, No.9, pp.1973-1984, Sept. 1991.