ALOE Framework and Tools

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SDR Execution Environment

SDR Application 2 (Waveform 2)

SDR Application $N$ (Waveform $N$)

Flexible Low Overhead

Pipelined Execution +
Online Mapping

Simplified Scheduling
Flexible Multiprocessing

ALOE
Outline

1. ALOE Framework
2. Computing Resource Management
3. ALOE Tools
4. Waveform Development
5. Summary
1.1 Lightweight Framework

- How to design a low-overhead framework?

- Language: Standard C
- Memory: Static (or custom pool)
- Scheduling: Static, non-preemptive
1.2 ALOE Layers

Abstract Application Layer

Real Application Layer

ALOE Layer

Hardware Layer

ALOE VIRTUAL PLATFORM

PE: Processing Element
1.3 ALOE Architecture

1.4 ALOE Time Management

- **Time slots** synchronized to ADC/DAC
- Relaxed **synchronization**
- Cooperative, static **scheduling**
- Deterministic **latency**

![Diagram of ALOE Time Management]

- ADC
- Rate Conv.
- Processor 1
- Processor 2
- Internal Link
- External Link
- Mapped modules:
  - Module mapped to processor 1
  - Module mapped to processor 2
  - ALOE daemons

2. Computing Resource Management

Management Algorithm

Mapping Algorithm

Cost Function

SDR Platform Modeling

SDR Application Modeling

Platform Models (Computing resources)

Application Models (Computing requirements)
2.1 SDR Platform Modeling

- Processing resources and requirements
- Inter-processor bandwidth resources and requirements

**Example: SDR Platform Model**

\[ C = (C_1, C_2, C_3) \text{ MOPTS} \]
\[ B = \begin{pmatrix} B & B \\ B & \infty & B \\ B & B & \infty \end{pmatrix} \text{ MBPTS} \]

- Abstraction layers provide computing resources & requirements in above units
- Availability of software modules for each processor type

**ABSTRACT**

- MOPTS: Million operations per time slot
- MBPTS: Mega-bits per time slot
2.2 Waveform: UMTS Downlink Receiver

- DDS Sampling Rate
  - DDS: 130 MOPS
  - DDS Sampling Rate: 492 MOPS
- Matched Filter
  - Matched Filter: 2450 MOPS
- 46 MOPS Interpolator
- 120 MOPS Frequency Adjust
- 160 MOPS 4-Finger RAKE MRC
- DPCH
- Physical Channel De-Mapping
- 2nd Deinter-leaving
- Physical Channel Desegmentation
- 10 MOPS

- Chip Sync
  - Sync1
  - Sync2
  - Sync3
  - Sync4
- 15.36 MOPS
- 1 MOPS Ray Search
- 92 MOPS Channel Estimation
- 7.68 Mbps

- Sampling Rate Adjust
  - Ray Search: 3.84 MHz
  - Freq Adjust: 65 MHz
  - Freq Adjust: 61.44 MHz
  - Sync4: 4·4000 MOPS
- Sync1
- Sync2
- Sync3

- 4·4000 MOPS
- 105 MOPS
- 10 MOPS

- Turbo Decoding
- Rate Matching
- 1st Deinter-leaving
- Radio Frame Desegmentation
- Physical Channel Desegmentation

- TrBk Concat./CodeBk Deseg.
- CRC
- 0.2 MOPS

- 0.384 Mbps

- TrBk Concat./CodeBk Deseg.
- CRC
- 0.2 MOPS

- 1.15 Mbps

- 342 MOPS Turbo Decoding
- 141 MOPS Rate Matching
- 116 MOPS 1st Deinter-leaving
- 62.9 MOPS Radio Frame Desegmentation

- 15.36 MOPS
- 7.68 Mbps

- 10 MOPS

- 15.36 MHz
- 3.84 MHz

- 3.84 MHz
- 7.68 Mbps
### 2.3 SDR Application Modeling

![Diagram of SDR Application Modeling]

**Function model:**
\[ c = (0.076, 0.289, 0.289, 1.44, 1.44, 2.35, 2.35, \ldots) \text{ MOPTS} \]

**Dataflow model:**
\[
\begin{bmatrix}
0 & 0.612 & 0.612 & 0 & 0 & 0 & 0 & \ldots \\
0 & 0 & 0 & 0.578 & 0 & 0 & 0 & \ldots \\
0 & 0 & 0 & 0 & 0.578 & 0 & 0 & \ldots \\
0 & 0 & 0 & 0 & 0 & 0.145 & \ldots & \text{MBPTS}
\end{bmatrix}
\]

**Stage model:**
\[ s = (1, 2, 2, 3, 3, 4, 4, 4, 4, 5, 6, 6, 7, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17) \]
2.4 The $t_w$-mapping & Cost Function

- Dynamic programming
- Parameter $w$ controls algorithm complexity
- Cost function independent
  - control different resources
  - define different optimization goals

Two-term cost function:

$$\text{Cost} = \frac{\text{processing requirement}}{\text{available processing power}} + \frac{\text{bandwidth requirement}}{\text{available bandwidth}}$$

- balance processing load
- minimize data flows


2.4 The $t_w$-mapping & Cost Function

$\{P_1, f_i\}$ represents the mapping of waveform component $f_i$ to processor $P_1$. 
2.4 The $t_w$-mapping & Cost Function

Path costs

Decision

$w = 1$

$P_1$ 0.5 $P_1$ 0.5

$P_2$ 0.6 $P_2$ 0.6

$f_1$ $f_2$ $f_3$ $f_4$

$f_1$, $f_2$, $f_4$ $\rightarrow$ $P_1$

$f_3$ $\rightarrow$ $P_2$

3. ALOE Tools

- Development and Debugging Tools
  - ALOE lab sessions
  - Source code templates
  - Automatic code generation tools (Simulink Target)
  - Graphical user interface
3.1 Graphical User Interface (I)

- Execution control
- Execution time statistics
- Parameter time evolution

Loaded modules
Schedule
Module Output
Parameter modification
3.1 Graphical User Interface (II)
4. Waveform Development

- LTE-128 points.
- 1 MHz
- 3 bit-streams
4.1 Processing Platforms

DAC/ADC

P1

P2

P3

P4

P5

P6

P7

P8

P9

P10

P11

P12

RF

PCIe

GbE

i7 Quad-Core, 2.6 GHz
ADC/DAC board: Innovative Integration X5-400
Sampling Rate: 61.44 MHz
Time-slot: 2 ms. E2E-latency: 40 ms.
4.2 Signal Captures

DA output (time and frequency domain)

Sync module output: Correlation with Zhou sequence

DDC output
5. Summary

ALOE Project

- Open source framework for SDR
- Non-commercial research version
- Tested:
  - GPPs under Linux (x86 and ARM7)
  - DSPs under RTOS-BIOS (TMS C64xx)
  - UMTS bit-level, LTE (1 MHz)

- Documentation and downloads at http://flexnets.upc.edu/